

# A 9-Bit 80-MS/s CMOS Pipelined Folding A/D Converter with an Offset Canceling Technique

Seung-Chul Lee, Young-Deuk Jeon, and Jong-Kee Kwon

*ABSTRACT*—A 9-bit 80-MS/s CMOS pipelined folding analog-to-digital converter employing offset-canceled preamplifiers and a subranging scheme is proposed to extend the resolution of a folding architecture. A fully differential dc-decoupled structure achieves high linearity in circuit design. The measured differential nonlinearity and integral nonlinearity of the prototype are  $\pm 0.6$  LSB and  $\pm 1.6$  LSB, respectively.

*Keywords*—Analog-to-digital converter (ADC), folding.

## I. Introduction

Folding analog-to-digital converters (ADCs) based on a flash structure inherit advantages in high-speed and low-voltage operation compared to the ADCs based on a multiplying digital-to-analog converter which requires high dc-gain amplifiers in closed-loop configuration for residue signal processing. However, the resolution of the folding architecture is limited by the offset voltage and the poor linearity of open-loop amplifiers [1], [2]. Although the averaging technique is useful in reducing the linearity degradation caused by the random offset voltage, it is less efficient when the offset voltage has any tendency. Moreover, the odd number of the folding factor impedes the extension of the ADC resolution in the cascade folding architecture. Odd interpolation between the pipelined stages can be considered, but it complicates digital error correction and deteriorates the linearity [3].

In this letter, we present an offset canceling technique used at the output node of the first stage pre-amplifier to alleviate the static performance limitation as well as a subrange scheme for

least significant bits to simplify decoding circuits and make the resolution extension flexible in folding ADCs.

## II. Proposed Pipelined Folding ADC Design

The pipelined folding architecture employing track-and-hold circuits (T/Hs) between the every folding stage was reported in [3]. By substituting the T/Hs for sample-and-hold circuits (S/Hs), as shown in Fig. 1, we can improve the static and dynamic performance of the folding ADC. Because the S/Hs always reset the previously sampled data, the worst-case settling time is shorter than the T/Hs and the signal-to-noise-and-distortion ratio (SNDR) of the ADC is less dependent on the input signal frequency. Furthermore, with the S/Hs, each stage adopts a dc-decoupled structure and deals solely with the difference between the input signal and the reference signal, so that larger input and output signal ranges with a flexible common mode level are achieved.

Before the folding stages, the offset-canceled preamplifiers alleviate the limitation on the linearity imposed by the folder offset. For the averaging technique, the six dummy preamplifiers,  $A_1$  to  $A_3$  and  $A_{20}$  to  $A_{22}$ , are added at the top and bottom reference resistors to minimize the signal distortion of the preamplifiers placed around both edges. The 4-bit sub-ADC with 16 comparators extracts the most significant bits from the preamplifier outputs,  $V_{A4}$  to  $V_{A19}$ . At the same time, the outputs of the preamplifiers are interpolated and transferred to the first folding stage. The cascade of two  $3\times$  folding stages and  $2\times$  resistive interpolation per stage effectively implements  $9\times$  folding with  $4\times$  interpolation. The three intermediate bits and one additional bit for error correction are obtained from the output of the second folding stage with a 3-bit sub ADC. At the last stage, the subranging block is employed to extend the

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Seung-Chul Lee (phone: + 82 42 860 6277, email: schlee@etri.re.kr), Young-Deuk Jeon (email: ydjeon@etri.re.kr), and Jong-Kee Kwon (email: jkkwon@etri.re.kr) are with IT Convergence & Components Laboratory, ETRI, Daejeon, Korea.

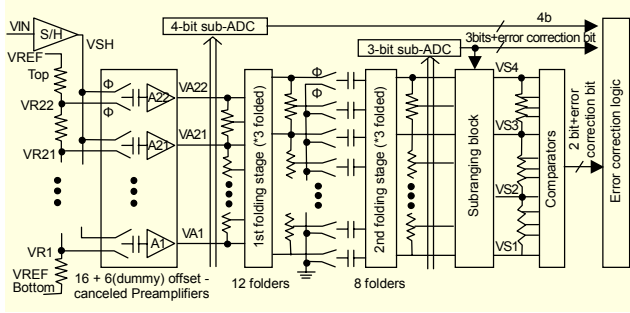


Fig. 1. Proposed pipelined folding A/D converter.

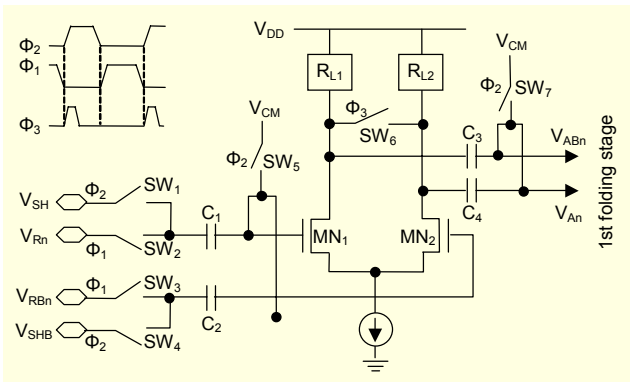


Fig. 2. Proposed preamplifier with offset canceling.

resolution of the pipelined folding architecture without odd interpolation between the pipeline stages. By repeatedly adding the sub-ranging block, additional bit extension is achievable in the architectural aspect.

As shown in Fig. 2, the proposed preamplifier with the input and output stages separated from other stages by capacitors makes circuit design more flexible and enables the employment of the offset canceling technique. When the  $\phi_2$  is high, the differential signals from the front-stage S/H, namely,  $V_{SH}$  and  $V_{SHB}$ , are sampled at the  $C_1$  and  $C_2$  capacitors, respectively. The other side of the capacitors is connected to the common mode voltage  $V_{CM}$  (around  $0.6 \cdot V_{DD}$ ), and the offset voltage of the preamplifier is stored at the  $C_3$  and  $C_4$  capacitors. The  $SW_6$  resets the output stage for the finite period  $\phi_3$ , reducing the reset time. During the amplifying phase  $\phi_1$ , the  $n$ -th reference voltages from the resistor ladder,  $V_{Rn}$  and  $V_{RBn}$ , are applied to the capacitors  $C_1$  and  $C_2$ . Only the voltage difference between the input and the reference voltage is amplified, so the outputs without the preamplifier offset are transferred to the first folding stage.

The gain of the preamplifier is set to about six to guarantee a level of accuracy greater than 9 bits for a  $1-V_{P-P}$  input considering folder offsets in the order of 10 mV. A higher gain could further decrease the effect of the folder offset but would degrade the linearity of the preamplifier output. The output nodes of the adjacent preamplifiers are connected through the

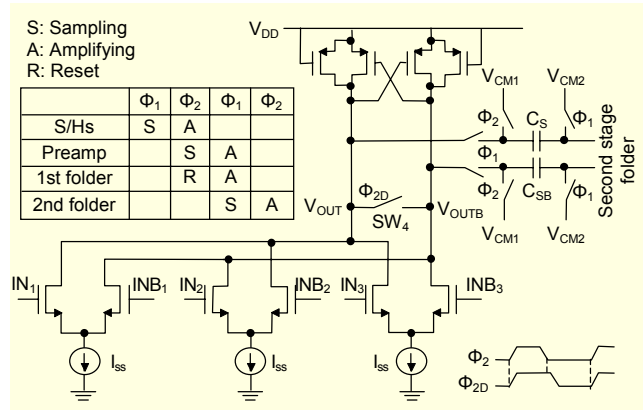


Fig. 3. First stage folder.

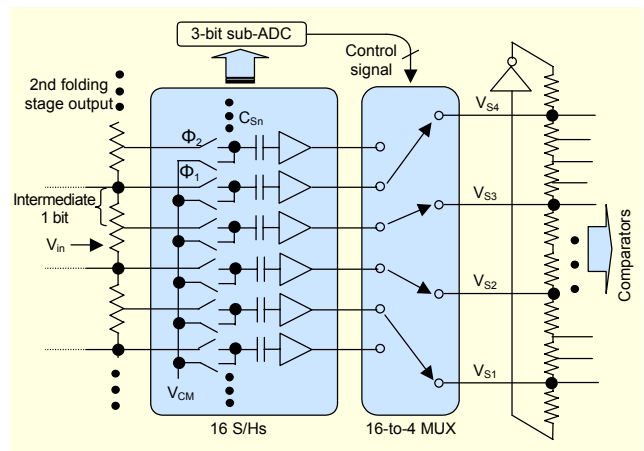


Fig. 4. Diagram of a sub-ranging block.

average resistors reducing the non-linearity resulting from the gain mismatch between the preamplifiers. However, a small error correction factor, relatively large average resistors ( $600 \Omega$ ) compared to the load resistors (about  $2 \text{ k}\Omega$ ), and a large preamplifier gain (which is not suitable for averaging technique) [4], are employed to clarify the effect of the proposed offset canceling technique. In this case, the improvement in differential nonlinearity enhanced by the averaging technique is only around 1 bit.

The first stage folder, shown in Fig. 3, adopts a conventional cross-coupled PMOS load. The folder folds and amplifies the signals from the preamplifiers by a gain of two during the  $\phi_1$ . The output signals are stored at the sampling capacitor,  $C_S$ . While the folder is in the reset period, switch  $SW_4$  has a slightly longer reset time ( $\phi_{2D}$ ) than the other switches, thereby avoiding backward flows due to the switch transition from the next stage S/H and facilitating the output signal to settle more rapidly. The second stage folder has the same structure as the first stage folder except for reverse clock phases.

The sub-ranging block, which determines the least significant bits, consists of S/Hs and the multiplexer, as shown in Fig. 4. The

outputs of the second folding stage are interpolated with resistors and stored at the sampling capacitors of the S/Hs during the  $\phi_2$  phase. At the same time, the signals are digitized by the 3-bit sub-ADC with 8 comparators directly connected to the second folding stage output. During the  $\phi_1$  phase, the sampled signals are applied to the subranging amplifiers, whose output connection to the resistor array is determined by the sub-ADC output through the multiplexer. The first and fourth output nodes of the subranging block,  $V_{S1}$  and  $V_{S4}$ , are connected through the resistors crossing the differential outputs of the amplifiers, which makes the condition of the output nodes similar to that of the other second and third output nodes,  $V_{S2}$  and  $V_{S3}$ . This method is adopted for every averaging resistor array in the proposed ADC.

In the pipelined folding architecture, the error correction scheme is more complex than that of the conventional ADCs with residue amplifiers because the fine comparator output does not reflect the coarse comparator error. Figure 5 shows the simplified multi-stage flash-type error correction of the proposed scheme. It compares the error correction bit from the previous stage sub-ADC with the parity of the next stage sub-ADC. When the two values are same, the error correction logic subtracts 1 from the output of the next stage sub-ADC. No operation is performed if the values are different.

### III. Implementation and Measurement

The proposed ADC is implemented in a 0.18- $\mu\text{m}$  n-well CMOS process with an active area of 2.2 mm<sup>2</sup> (=1.6 mm $\times$ 1.4 mm), as shown in Fig. 6. The power consumption, including an on-chip reference driver circuit, is 115 mW at 80 MS/s from a 1.8 V supply. About one-third of the total power is dissipated by the pre-amplifiers. The measured differential nonlinearity and integral nonlinearity are  $\pm 0.6$  LSB and  $\pm 1.6$  LSB, respectively, as shown in Fig. 7. The resolution of the proposed ADC is better than the recently published results using the

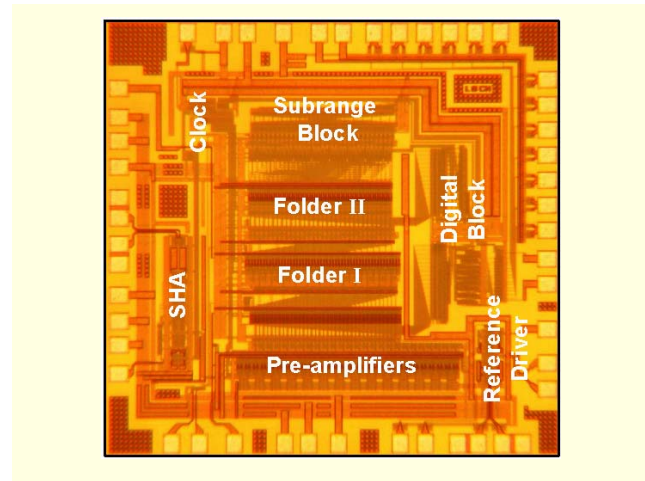


Fig. 6. Die photograph of the proposed A/D converter.

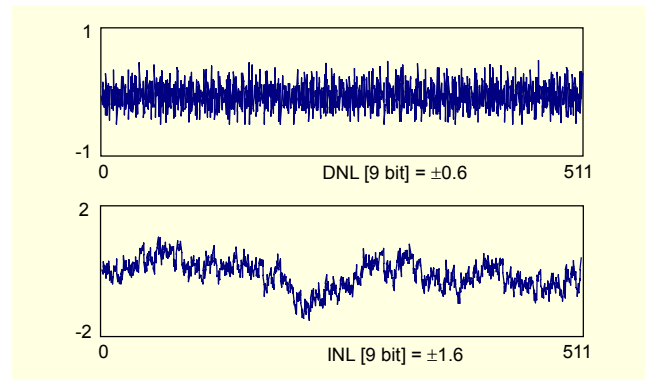


Fig. 7. Measured static performance.

averaging technique [1], [2] by about 1 bit, despite its relatively small error correction factor. If the ADC employed a higher error correction factor suitable for averaging techniques, it could achieve a higher linearity up to 10 bits. An SNDR of around 50 dB has been achieved for low output frequencies. The measured SNDR is 49 dB for 8 MHz input at 80 MS/s.

MSB' (corrected value)	Under		0				1					
MSB (sub-ADC output)	0		1				2					
(MSB+1)' (corrected value)	1		0				1					
MLSB' (corrected value)	2	3	0	1	2	3	0	1	2	3		
MLSB+1 (sub-ADC output)	1		0				1					
MLSB (sub-ADC output)	3	0	1	2	3	0	1	2	3			
LSB+1 (sub-ADC output)	0	1	0	1	0	1	0	1	0	1		
LSB (sub-ADC output)	0	1	2	3	0	1	2	3	0	1	2	3
MLSB correction	<ul style="list-style-type: none"> <li>• If MLSB is even and LSB+1 is 0, then subtract 1 from MLSB.</li> <li>• If MLSB is even and LSB+1 is 1, then no correction is performed.</li> <li>• If MLSB is odd and LSB+1 is 0, then no correction is performed.</li> <li>• If MLSB is odd and LSB+1 is 1, then subtract 1 from MLSB.</li> </ul>											
MSB correction	<ul style="list-style-type: none"> <li>• If MSB is even and (MSB+1)' is 0, then subtract 1 from MSB.</li> <li>• If MSB is even and (MSB+1)' is 1, then no correction is performed.</li> <li>• If MSB is odd and (MSB+1)' is 0, then no correction is performed.</li> <li>• If MSB is odd and (MSB+1)' is 1, then subtract 1 from MSB.</li> </ul>											

Fig. 5. Error correction scheme.

### References

- [1] K. Makigawa, K. Ono, T. Ohkawa, K. Matsuura, and M. Segami, "A 7-Bit 800-Msps 120-mW Folding and Interpolation ADC Using a Mixed-Averaging Scheme," *Proc. Symp. VLSI Circuits*, 2006, pp. 138-139.
- [2] G. Geelen and E. Paulus, "An 8-b 600-MS/s 200-mW CMOS Folding A/D Converter Using an Amplifier Preset Technique," *IEEE ISSCC Dig. Tech. Papers*, Feb. 2004, pp. 254-255.
- [3] M.J. Choe, B.S. Song, and K. Bacrania, "A 13-b 40-Msample/s CMOS Pipelined Folding ADC with Background Offset Trimming," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, Dec. 2000, pp. 1781-1790.
- [4] K. Kattmann and J. Barrow, "A Technique for Reducing Differential Non-linearity Error in Flash A/D Converter," *IEEE ISSCC Dig. Tech. Papers*, Feb. 1991, pp. 170-171.