A New Automatic Compensation Network for System-on-Chip Transceivers

Jee-Youl Ryu and Seok-Ho Noh

This paper proposes a new automatic compensation network (ACN) for a system-on-chip (SoC) transceiver. We built a 5 GHz low noise amplifier (LNA) with an on-chip ACN using 0.18 μm SiGe technology. This network is extremely useful for today's radio frequency (RF) integrated circuit devices in a complete RF transceiver environment. The network comprises an RF design-for-testability (DFT) circuit, capacitor mirror banks, and a digital signal processor. The RF DFT circuit consists of a test amplifier and RF peak detectors. The RF DFT circuit helps the network to provide DC output voltages, which makes the compensation network automatic. The proposed technique utilizes output DC voltage measurements and these measured values are translated into the LNA specifications such as input impedance, gain, and noise figure using the developed mathematical equations. The ACN automatically adjusts the performance of the 5 GHz LNA with the processor in the SoC transceiver when the LNA goes out of the normal range of operation. The ACN compensates abnormal operation due to unusual thermal variation or unusual process variation. The ACN is simple, inexpensive and suitable for a complete RF transceiver environment.

Keywords: System-on-chip, automatic compensation network, low noise amplifier.

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I. Introduction

Wireless communication using radio frequency integrated circuit (RFIC) devices has been a rapidly expanding field, and considerable research continues in that area [1]-[10]. Today's electronics industry is actively trying to incorporate all of the RF, intermediate frequency (IF), and baseband functions into the fewest possible ICs to reduce system size and cost, and to improve overall system performance. However, the lack of a suitable test technique and the need to reduce test costs for this system-on-chip (SoC) trend still remain major obstacles to making wireless systems affordable. The cost of production testing is particularly problematic. A majority of these testing costs are related to the performance testing of RF components [1], [2].

Faults occurring in RFICs are commonly classified into catastrophic faults (hard faults) caused by, for example, spot defects and parametric faults (soft faults). Parametric faults results from random fluctuations inherent in the variation of the manufacturing process including mask misalignment and line width variation, or defect-related sensitivity to environmental parameters such as power supply and temperature [1]-[4]. The designers and engineers of RF and mixed-signal tests are primarily concerned with parametric faults. This is because these faults are hard to distinguish from acceptable variations and lead to a significant performance loss which violates the circuit's specification [2]. Since the parametric variation simulations and tests for RF circuits are more complicated and time-consuming than those for analog and digital circuits, it is a crucial issue in RF testing. In particular, once chips are fabricated and packaged, simple comparison or sophisticated compensation techniques need to be applied to adjust the performance of chips with process variations or thermal

variations. Unfortunately, if the internally adjusting performance loss resulting from these variations in the SoC environment cannot be overcome, the SoC approach will be dismissed as impracticable due to chip production and test costs. Despite the considerable research which is underway to solve these problems [1]-[10], the IC industry is seeking a more suitable technique.

In this paper, a new low-cost alternative for RF SoC testing to adjust parametric variations is proposed. The alternative utilizes an automatic compensation network (ACN) for a 5 GHz low-noise amplifier (LNA) as a typical RF front-end chip. The network comprises an RF design-for-testability (DFT) circuit, capacitor mirror banks (CMBs), and a digital signal processor (DSP). The RF DFT circuit helps the network to provide DC output voltages, which makes the compensation network automatic.

II. Automatic Compensation Network Configuration

Figure 1 shows the SoC-based receiver configuration with an automatic ACN for the LNA. In the ACN, the processor automatically adjusts and compensates the performance of the 5 GHz LNA when it goes out of the normal range of operation due to unusual thermal variation or unusual process variation.

The RF DFT hardware consists of a test amplifier (TA), a band-gap reference, and two RF peak detectors (PD1 and PD2) as shown in Fig. 2. This additional hardware occupies a very small area on the SoC, and it helps to measure LNA performance without expensive external equipment. Two RF peak detectors are used to provide DC output voltages (V_{T1} and V_{T2}).

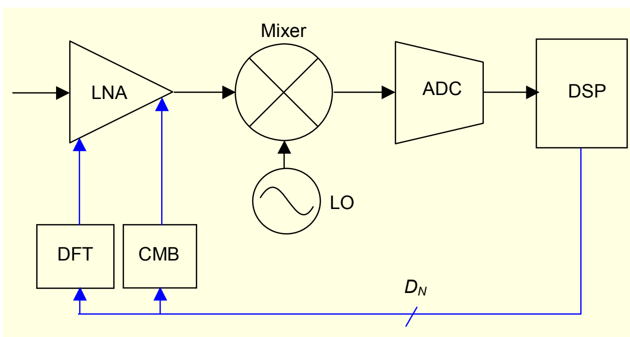

Fig. 1. SoC-based receiver configuration with an ACN for the LNA.

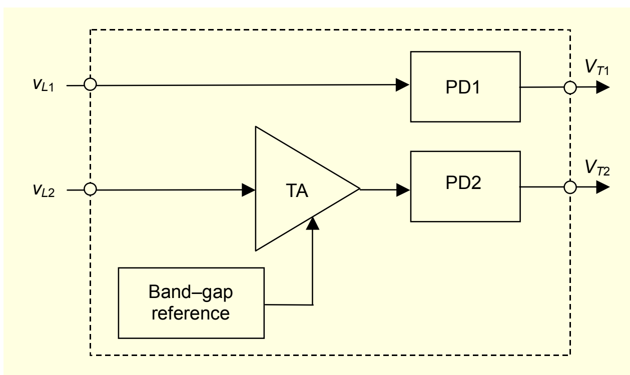

Fig. 2. RF DFT hardware.

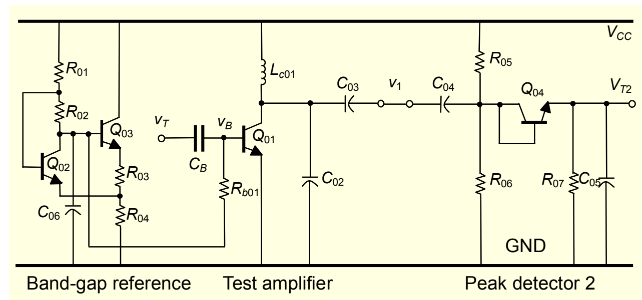

Fig. 3. Schematic diagram of an RF DFT.

The proposed DFT circuit is shown in Fig. 3. It is designed using 0.18 μm SiGe technology and consists of TA and PD2 circuit stages. The PD1 circuit is also a part of the DFT circuit, and it has the same topology as the PD2 circuit as shown in Fig. 3. The test amplifier is designed with the input and output impedances of 50 ohms. The gain of the test amplifier is designed to be 3 to increase the output voltage level. The RF peak-detectors are used to convert RF signal to DC voltage. The bias stage utilizes a band-gap reference circuit for a low-supply voltage and low-power dissipation. The inductor L_{c01} is used to match input and output impedances. The bias resistors R_{05} and R_{06} shown in Fig. 3 are used to keep transistor Q_{04} in the active region so that the transistor acts as a rectifier. The diode connections have the advantage of keeping the base-collector junction at zero bias. The smallest amount of minority-charge storage when there is a forward-biased condition will be highly beneficial to the rectification of RF signals [11]. To reduce the output-ripple voltage, large values were chosen for R_{07} and C_{05}. For details concerning high-frequency small-signal analysis of the DFT circuit, refer to [12].

Figure 4 shows the design of the proposed CMB. It has N-bit capacitor banks to accurately compensate LNA performance. Taking this approach, we have designed an 8-bit CMB considering chip area overhead. Each capacitor bank is controlled using digital signals ($D_8 \cdots D_2 D_1$) from the digital signal processor (DSP) hardware. The input data streams of ($D_8 \cdots D_2 D_1$) = (0⋯01) for (1/8) C_b and (1⋯11) for C_b are used to compensate LNA performance. The C_b is under fault-free value. It was designed with LNA on a single chip using 0.18 μm SiGe technology to demonstrate this idea. It is powered by 1.8 V supply voltage. It was designed to have separate power supplies for the RF and digital sections of the chip to isolate the

RF circuitry from the switching noise introduced by the digital supplies. The chip is divided into RF and digital sections with different substrate grounds to attenuate noise coupling from one area of a chip to another. The distributed gate resistance of the MOS devices contributes to the thermal noise [13]. To minimize this resistance, the transistors M_1 to M_8 were laid out as a parallel combination of many narrower devices. The transconductances of the transistors were minimized to reduce the input-referred noise voltage related to the thermal noise. These transistors, like MOS switches, are designed to operate in the deep triode region so that they exhibit no DC shift between the input and output voltages [14]. The resistors, R_{D1} to R_{S8} were used to control a DC-bias voltage of MOS switches. For details of DC and high frequency small-signal analysis of the CMB, refer to the appendix.

To verify the performance of our proposed ACN, a two-stage LNA was designed. It was designed for a 5 GHz IEEE 802.11a wireless LAN application. Figure 5 shows the schematic of the 5 GHz LNA, which is powered by a 1 V supply. The bias stage utilizes a band-gap reference circuit for a low supply voltage and low-power dissipation. It controls base currents for the first and second stages. The complete design consists of four HBTs, five inductors, five capacitors, and six resistors, all on a single chip. For details of the LNA, refer to [12].

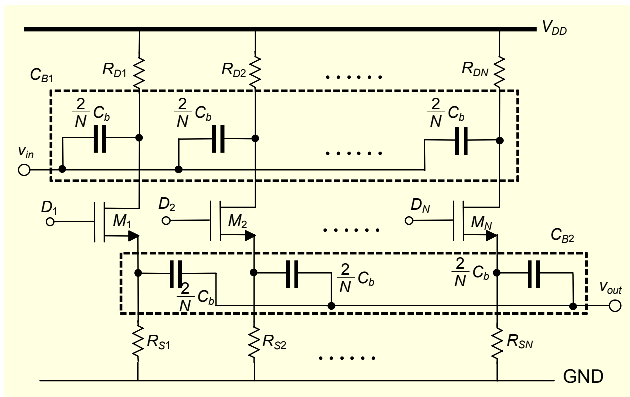

Fig. 4. N-bit CMB.

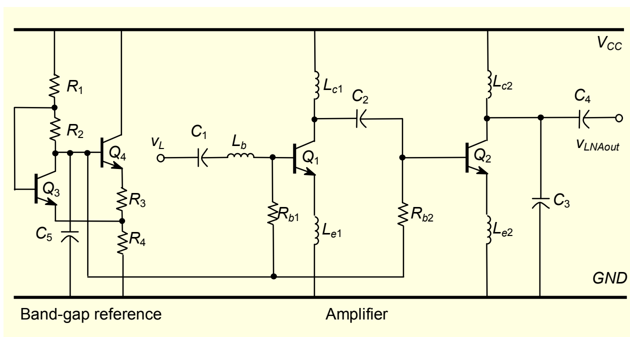

Fig. 5. Schematic diagram of the LNA.

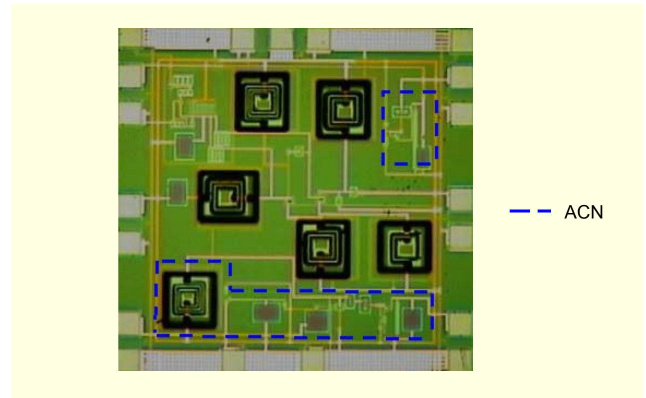

Fig. 6. Chip micrograph of the LNA with ACN.

Figure 6 shows a chip micrograph of the LNA with ACN. The ACN is the space within the dotted lines. The physical chip area is approximately 1.5 mm×1.5 mm.

III. Test Set-up and Approach

1. Test Set-up

Figure 7 shows the test set-up used to realize our idea which was shown in Fig. 1. Our proposed ACN provides DC outputs so that all of the measurements can be done by an on-chip data converter within the SoC, making the test set-up automatic.

It contains an LNA, a DFT circuit, and CMBs, all on a single chip. The test structure can be automatically configured by the external data acquisition hardware. The complete test-bed contains an RF source (v_{in}) with source resistance (R_s), RF relays (S1, S2, and S3), load impedance (Z_L), and a data converter board. The measurement set-up contains very low-loss RF relays and input transmission matching the LNA and DFT circuits. The positions of the relays were controlled to measure the output DC voltages V_{T1} and V_{T2} through the DFT circuit. These relays were controlled by a DeMux chip on an external board.

Figure 8 shows the procedure of our three-step process to compensate LNA performance. The first step is to measure the

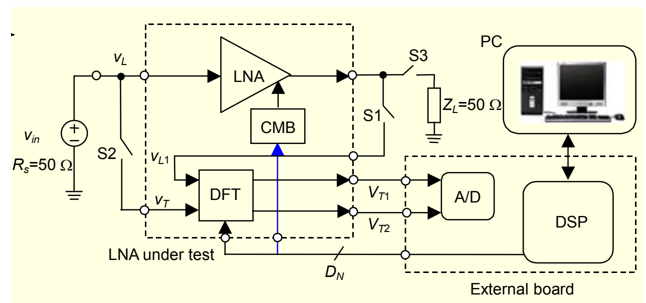

Fig. 7. Measurement set-up of the ACN for an RF LNA.

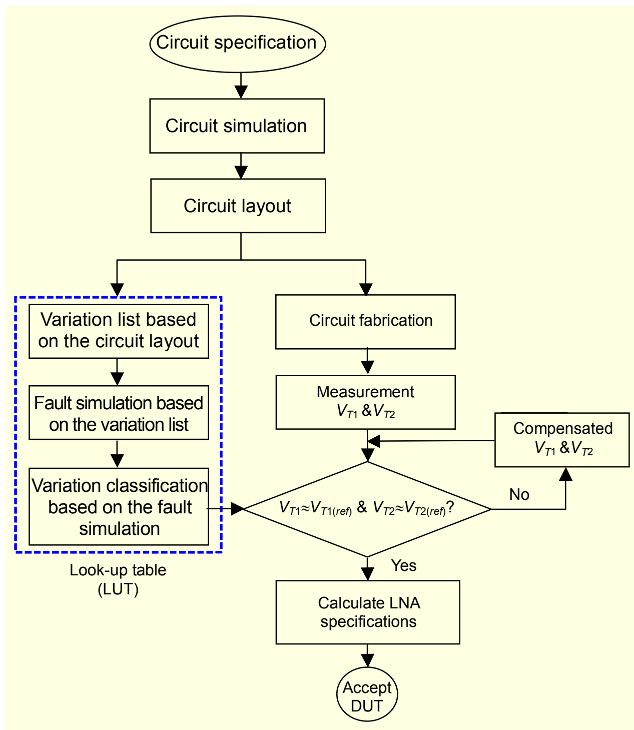

Fig. 8. Procedure of the ACN for specific LNA performance.

simple DC outputs V_{T1} and V_{T2} using the proposed DFT hardware. The second step is to compare the measured DC outputs V_{T1} and V_{T2} with reference values $V_{T1(ref)}$ and $V_{T2(ref)}$, which may be found in a look-up table. Finally, the automatic compensation step is applied to adjust LNA performance when the LNA has process variations or thermal variations. If the measured V_{T1} and V_{T2} values are more than ±2% of the reference values $V_{T1(ref)}$ and $V_{T2(ref)}$, they are automatically compensated. Specific LNA specifications are compensated, such as input impedance, gain, and noise figure.

2. Theoretical Approach

Since the parametric variation tests for RF circuits are more complicated and time-consuming than those of analog and digital circuits, it is a crucial issue in RF testing. Our proposed technique utilizes an on-chip DFT circuit to measure important LNA specifications without major external testing equipment. Our new RF DFT circuit provides DC output voltages, making the overall test set-up simple, inexpensive, and automatic. These DC output voltages are converted to units of decibels and ohms using the equations we developed for the LNA specifications. In this paper, we consider measurements of input impedance, gain, and noise figure of the LNA. We consider fault-free and faulty cases and present mathematical expressions which we developed to translate the output DC measurements to actual LNA parameters.

A. *Input Impedance*

Figure 9 shows the equivalent circuit for the inputs of the LNA and test amplifier. In the figure, $Z_{in(LNA)}$ and $Z_{in(TA)}$ represent the input impedances of the LNA and test amplifier, respectively. These impedances have resistance and reactance parts. The input impedance measurement is performed with the switches S2 and S3 in closed position and the switch S1 in open position as shown in Fig. 7. The aim of the overall test technique is to find any deviations between the source impedance (R_s) and the input impedances ($Z_{in(LNA)}$ and $Z_{in(TA)}$). For example, the test amplifier of Fig. 9 checks changes in the input impedance of the LNA for any mismatch with the source resistance. Figure 9 shows the DC voltage at the output of the RF DFT circuit in the case of a mismatch due to a defect or a process variation.

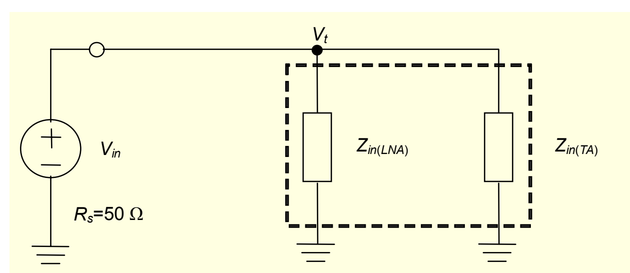

Fig. 9. Equivalent circuit for the inputs of the LNA and test amplifier.

We consider a fault-free LNA with a perfectly matched input impedance of 50 ohms. The theoretical value for the voltage across the input impedances of the LNA and test amplifier is expressed as $V_t = \left| Z_{in(LNA)} / (2Z_{in(LNA)} + R_s) \right| V_{in}$. Voltage is represented in terms of the LNA impedance ($Z_{in\,(LNA)}$) when we assume the matched 50 ohm impedance for the test amplifier. The test amplifier is designed with the input and output matching impedances of 50 ohms, respectively. The gain of the test amplifier (G_{TA}) is set to 3 to increase the output voltage level. The DFT circuit monitors the DC voltage V_{T2} as shown in Fig. 7. Using the measured V_{T2} voltage, a new expression to calculate the fault-free LNA impedance, $Z_{in\,(LNA)}$ is obtained:

$$\left| Z_{in(LNA)} \right| = f(V_{T2}) = R_s \frac{K_1}{1 - \left(1 + \dfrac{R_s}{\left| Z_{in(TA)} \right|} \right) K_1}, \qquad (1)$$

where $K_1 = G_{02} / G_{TA}$, G_{02} is the voltage gain expressed as $G_{02} = (V_{T2} - V_{02}) / V_{in}$, and V_{02} is the offset voltage for the peak-detector circuit, PD2.

Under a faulty condition, the LNA can have parametric faults such as unusual thermal variations and unusual process

variations [1]-[4]. In this case, there is a certain variation in the input impedance magnitude of the LNA because of change in its input matching condition. This condition provides a new value in V_{T2}, which is the output DC voltage for the faulty LNA. The input impedance of the LNA under a faulty condition can be expressed as

$$\overline{|Z_{in(LNA)}|} = f(\overline{V_{T2}}) = R_s \frac{\overline{K_1}}{1-\left(1+\frac{R_s}{|Z_{in(TA)}|}\right)\overline{K_1}}, \quad (2)$$

where $\overline{K_1} = \overline{G_{02}}/G_{TA}$, and G_{02} is the voltage gain expressed as $\overline{G_{02}} = (\overline{V_{T2}} - V_{02})/V_{in}$ under a faulty condition. The bar represents the defective parameters under faulty conditions.

B. Voltage Gain

The voltage gain measurement is performed with the switch S1 in the closed position and the switches S2 and S3 in the open position as shown in Fig. 7. The voltage gain measurement is based on monitoring the DC voltage of the first peak detector, PD1. The DFT circuit monitors the DC voltage V_{T1} as shown in Fig. 7. Using the measured V_{T1} and V_{T2} voltages, a new expression to calculate the fault-free LNA gain, G_{LNA}, is used:

$$G_{LNA} = f(V_{T1}, V_{T2}) = \left(1+\frac{R_s}{|Z_{in(LNA)}|}\right)G_{01}, \quad (3)$$

where G_{01} is the voltage gain expressed as $G_{01} = (V_{T1} - V_{01})/V_{in}$, and V_{01} is the offset voltage for the peak detector circuit, PD1.

Under a faulty condition, the DFT circuit provides a new value in V_{T1}, which is the output DC voltage for the faulty LNA. The voltage gain of the LNA under a faulty condition can be expressed as

$$\overline{G_{LNA}} = f(\overline{V_{T1}}, \overline{V_{T2}}) = \left(1+\frac{R_s}{\overline{|Z_{in(LNA)}|}}\right)\overline{G_{01}}, \quad (4)$$

where $\overline{G_{01}}$ represents the voltage gain expressed as $\overline{G_{01}} = (\overline{V_{T1}} - V_{01})/V_{in}$ under a faulty case.

C. Noise Figure

The conventional formula for the noise figure is given in [12] as

$$NF = 1 + \frac{N_2}{G \cdot N_1}, \quad (5)$$

where G is the amplifier power gain, N_1 is the LNA source resistance noise power, and N_2 is the inherent output noise. Using (5), noise figure equations based on the proposed RF DFT structure are developed.

If there is no detectable defect and the device performance is within the specifications of the input impedance and voltage gain measurements, the noise figure obtained by the DFT circuit can be expressed using the noise figure anticipated by the LNA specification. The approximate expression for the fault-free noise figure based on the RF DFT structure is determined as

$$NF = f(V_{T1}, V_{T2}) = 1 + \left\{\frac{|Z_{in(LNA)}|}{R_s + |Z_{in(LNA)}|}\right\}^2 \cdot \frac{G_0}{G_{01}^2}(NF_0 - 1), \quad (6)$$

where G_0 and NF_0 are power gain and the noise figure anticipated by the LNA specification, respectively.

Under the case of a fault, the noise figure can be expressed as

$$\overline{NF} = f(\overline{V_{T1}}, \overline{V_{T2}}) = 1 + \left\{\frac{\overline{|Z_{in(LNA)}|}}{R_s + \overline{|Z_{in(LNA)}|}}\right\}^2 \cdot \frac{G_0}{\overline{G_{01}^2}}(NF_0 - 1). \quad (7)$$

IV. Results

Parametric fault testing of the LNA involves expensive measurement equipment. Our RF DFT circuit provides DC voltages (V_{T1} and V_{T2}), which can be used to find LNA specifications through the mathematical expressions shown in previous section. We were able to adjust the CMB with the LNA circuits by providing a combination of digital codes to the capacitor banks. Using the signal processor, the ACN automatically adjusts the performance of the 5 GHz LNA when it goes out of the normal range of operation. To demonstrate this idea, we considered variations of LNA gains and noise figures due to process variations, thermal variations, and coupled variations. As process variations, we identified the most sensitive inductor component L_{c1} shown in Fig. 5 that contributed to varying LNA voltage gains. As thermal variations, we considered temperature variations of -20°C to 70°C that contributed to varying LNA noise figures. We also identified coupled variations including both process variations and thermal variations. In each of these three cases, our results verify that the proposed ACN automatically adjusts and compensates the LNA performance.

Table 1 lists $V_{T1(ref)}$ and $V_{T2(ref)}$ measured at the output of the DFT circuit as a frequency function of the LNA. The measurement results show the average values for 10 cases.

Table 1. $V_{T1(ref)}$ and $V_{T2(ref)}$ measured by the DFT circuit.

Frequency (GHz)	$V_{T1(ref)}$ (mV)		$V_{T2(ref)}$ (mV)	
	Simulation	Measurement	Simulation	Measurement
4.50	400	343.8	166.20	205.3
4.75	421	335.7	160.30	218.2
5.00	448	304.8	171.40	213.4
5.25	445	274.9	180.00	205.4
5.50	432	253.0	189.00	182.3
5.75	418	232.0	191.05	168.1
6.00	406	219.1	192.02	160.2

Acceptable variations of less than ±2% for fault-free values from Monte Carlo simulations were considered. The DC voltages $V_{T1(ref)}$ and $V_{T2(ref)}$ were measured after 40 nanoseconds settling time of the peak detectors PD1 and PD2 to ensure steady-state DC value. The output RC time constant of the peak detector contributed to the settling time constant. These results were used to obtain the magnitudes of the input impedances, voltage gains, and noise figures of the LNA as shown in (1), (3), and (6). As can be expected from the simulation results, $V_{T1(ref)}$ had the highest value at the operating frequency of 5 GHz. Since $V_{T1(ref)}$ is proportional to the LNA gain, it showed the highest value at this frequency. When the frequency increased, $V_{T2(ref)}$ also increased. As shown in Table 1, the measured experimental results are similar to the simulation results in this regard. However, the measurement result showed the maximum values at a lower frequency than the simulation. This frequency shift may be a result of parasitic effects at high frequencies.

1. Process Variations and Compensations

Figure 10 shows the gain variation and its compensation results for a +20% process variation of the most sensitive component (L_{c1}) as shown in Fig. 5. Defect-free values are obtained using the results of Table 1 and (3). Variation values are plotted using (4). The gain compensation shown in this figure was performed at the operation frequency of 5.25 GHz. We identified a variation of 1.04 dB (11.32%) in the LNA gain from the +20% process variation. To compensate a 1 dB LNA gain, the input data stream of $(D_8 \cdots D_2 D_1) = (0 \cdots 01)$ providing $C_B = (1/8)C_b$ was applied. The C_b is the same value for the fault-free case. As can be seen from Fig. 10, our ACN can compensate the gain of LNA due to the process variation at 5.25 GHz.

We investigated the noise figure compensation from the LNA gain compensation using the input data stream of $(D_8 \cdots D_2 D_1) = (0 \cdots 01)$ for $(1/8)C_b$. Figure 11 depicts the noise figure variation and its compensation results for the L_{c1}+20% process variation. Defect-free values were also obtained using the results of Table 1 and (6). Variation values are obtained using (7). The noise figure compensation shown in this figure was performed at the operation frequency of 5.25 GHz. The L_{c1}+20% process variation showed a small variation in the LNA noise figure as shown in Fig. 11. We identified a variation of 0.022 dB (0.5%) in the LNA noise figure from the +20% process variation. As shown in Fig. 11, our ACN can compensate the noise figure of the LNA due to the process variation at 5.25 GHz. The impedance matching network at the LNA input has a significant effect on the noise figure performance [15], [16]. The significant improvement in the noise figure shown in Fig. 11 reveals that the input impedance matching which resulted

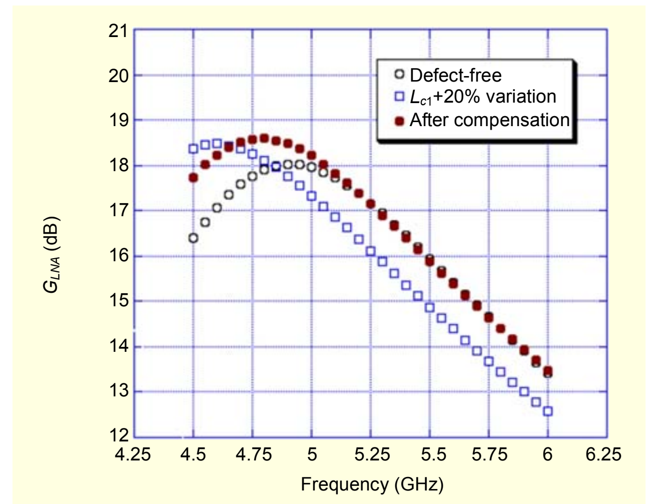

Fig. 10. LNA gain compensation for L_{c1}+20% process variation.

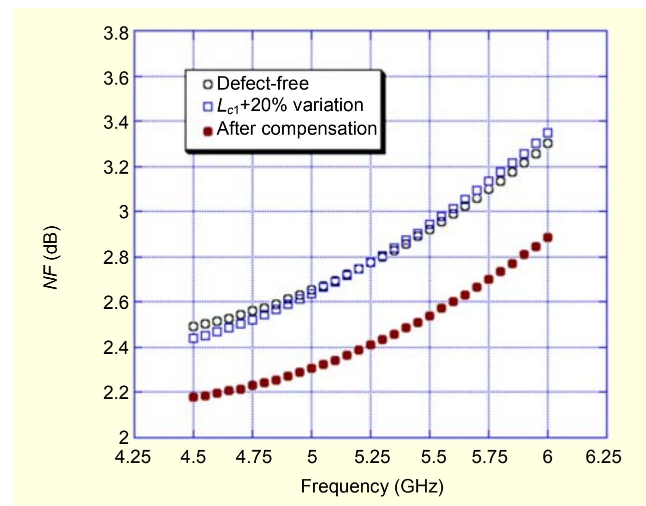

Fig. 11. LNA noise figure compensation for L_{c1}+20% process variation.

from the adjustment of C_b after compensation is optimized. The noise figure can be minimized by choosing the optimum base capacitor, C_b [15], [16].

2. Thermal Variations and Compensations

Figure 12 shows the gain variation and its compensation results for the +40°C thermal variation. The gain compensation shown in this figure was done at the operation frequency of 5.25 GHz. Defect-free values were also obtained using results of Table 1 and (3), and variation values were plotted using (4). We identified a variation of 0.372 dB (4.19%) in the LNA gain from the +40°C thermal variation. The +40°C thermal variation showed a small variation in the LNA gain as shown in Fig. 12. To compensate this LNA gain variation, the input data stream of $(D_8 \cdots D_2 D_1) = (0 \cdots 01)$ providing $C_B = (1/8)C_b$ was applied. As can be seen from Fig. 12, our ACN can compensate the gain of the LNA due to the thermal variation at 5.25 GHz.

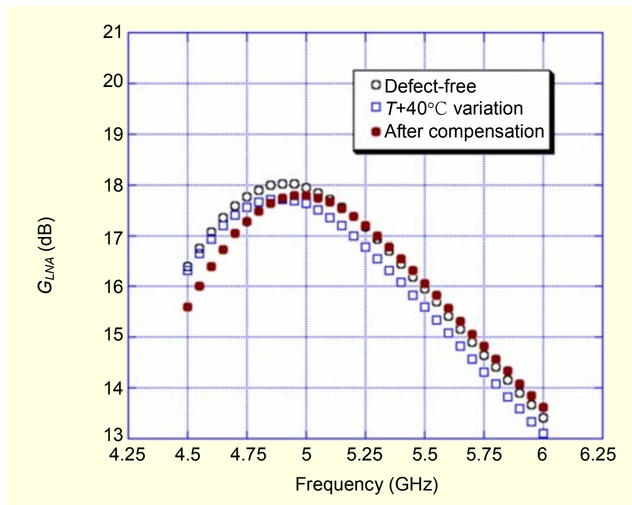

Fig. 12. LNA gain compensation for T+40°C thermal variation.

Figure 13 shows the noise figure variation and its compensation results for the +40°C thermal variation. The noise figure compensation shown in this figure was done at the operation frequency of 5.25 GHz. We identified a variation of 0.357 dB (8.55%) in the LNA noise figure from the +40°C thermal variation. To compensate this LNA noise figure variation, we provided the input data stream of $(D_8 \cdots D_2 D_1) = (0 \cdots 01)$ for $(1/8)C_b$. As can be expected, the +40°C thermal variation showed a large variation in the LNA noise figure asshown in Fig. 13. The proposed ACN can compensate the noise figure of the LNA due to the thermal variation at 5.25 GHz. This significant improvement in the noise figure shown in Fig. 13 reveals that the input impedance matching after C_b compensation is optimized. The noise figure can be minimized by choosing the optimum base capacitor, C_b [15], [16].

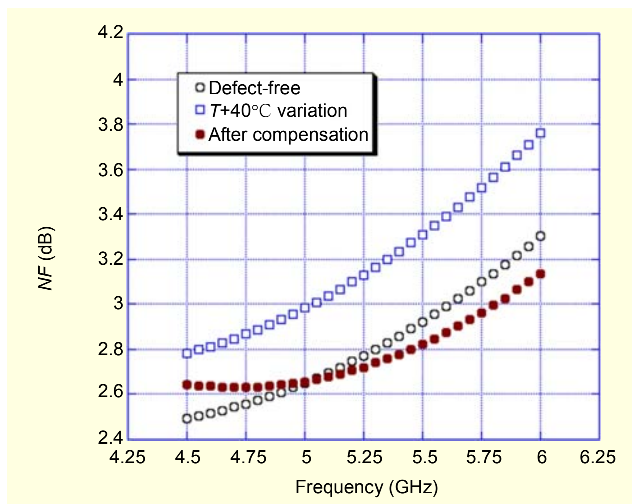

Fig. 13. LNA noise figure compensation for T+40°C thermal variation.

3. Coupled Variations and Compensations

Figure 14 shows the gain variation and its compensation results for the L_{c1}+10% process and +40°C thermal variations. The gain compensation shown in this figure was done at the operation frequency of 5.25 GHz. We identified a variation of 0.843 dB (9.25%) in the LNA gain from the L_{c1}+10% process and +40°C thermal variations. These variations showed large variation in the LNA gain as shown in Fig. 14. To compensate this LNA gain variation, the ACN provided the input data stream of $(D_8 \cdots D_2 D_1) = (0 \cdots 01)$ for $(1/8)C_b$. As shown in Fig. 14, the proposed ACN can compensate the gain of the LNA due to the process and thermal variations at 5.25 GHz.

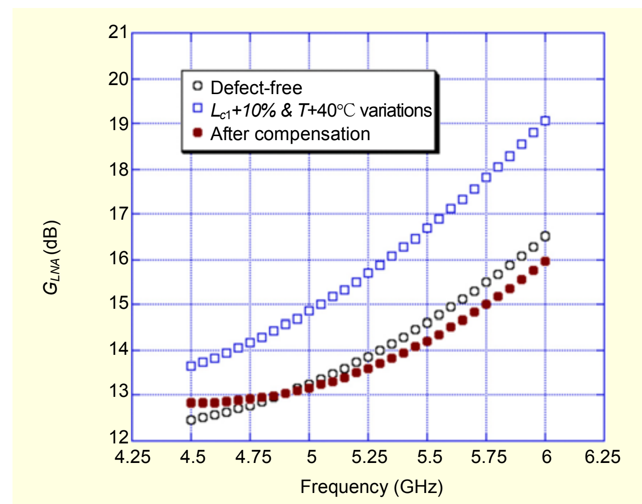

Fig. 14. LNA gain compensation for coupled variations.

Table 2. Comparison of variation and their compensations.

Variations			Compensations			
Components	ΔG_{LNA} (dB)	ΔNF (dB)	Data codes	C_B	ΔG_{LNA} (dB)	ΔNF (dB)
L_{c1}+10%	-0.450	0.003	(00000011)	0.250C_b	0.440	-0.367
L_{c1}+20%	-1.040	0.022	(00000001)	0.125C_b	1.010	-0.370
T+10°C	-0.103	0.108	(00111111)	0.750C_b	0.146	-0.141
T+20°C	-0.188	0.191	(00001111)	0.500C_b	0.283	-0.275
T+30°C	-0.277	0.274	(00000011)	0.250C_b	0.403	-0.393
T+40°C	-0.372	0.357	(00000001)	0.125C_b	0.412	-0.409
L_{c1}+10% & T+10°C	-0.560	0.113	(00001111)	0.500C_b	0.305	-0.272
L_{c1}+10% & T+20°C	-0.649	0.197	(00000011)	0.250C_b	0.443	-0.368
L_{c1}+10% & T+30°C	-0.744	0.281	(00000011)	0.250C_b	0.445	-0.396
L_{c1}+10% & T+40°C	-0.843	0.366	(00000001)	0.125C_b	0.517	-0.420
L_{c1}+20% & T+10°C	-1.150	0.134	(00000001)	0.125C_b	0.548	-0.388

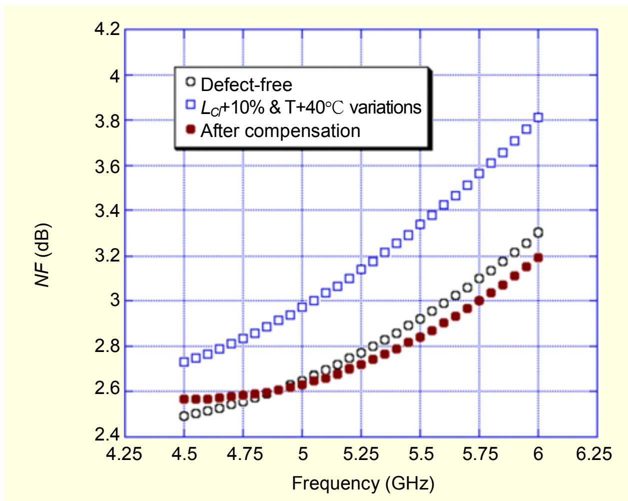

Fig. 15. LNA NF compensation for coupled variations.

Figure 15 shows the noise figure variation and its compensation results for the L_{c1}+10% process and +40°C thermal variations. The gain compensation shown in this figure was done at the operation frequency of 5.25 GHz. We identified a variation of 0.366 dB (8.77%) in the LNA noise figure from the L_{c1}+10% process and +40°C thermal variations. These variations showed a large variation in the LNA noise figure as shown in Fig. 15. To compensate this LNA noise figure variation, the compensation network adjusted the input data stream of $(D_8 \cdots D_2 D_1) = (0 \cdots 01)$ for $(1/8)C_b$. As shown in Fig. 15, the presented ACN can compensate the noise figure of the LNA due to the process and thermal variations at 5.25 GHz. This significant improvement in the noise figure shown in Fig. 15 reveals that the input impedance matching after C_b compensation is optimized.

Table 2 summarizes the noise figure and gain variations and their compensation results for process, thermal and coupled variations. Data codes used for compensation are listed. As can be seen in this table, the proposed ACN showed good compensation results for the variations of the LNA gains and noise figures.

V. Conclusion

This paper presented a new ACN for the LNA .We proved that our ACN can help to compensate LNA with parametric variations. Utilizing our new ACN, we measured input impedance, gain and noise figure, and it automatically adjusted performance of 5 GHz LNA when the LNA went out of the normal range of operation. The new ACN provided successful measurement results of LNA chips. The RF LNA is provided with complete testing by utilizing a novel ACN architecture and mathematical equations. We believe that this new capability will provide industry with a low-cost technique to test RFIC chips.

Appendix

Consider the DC model shown in Fig. A1 to explain the DC bias condition of the 1-bit CMB.

When digital input D_1 shown in Fig. A1(a) is in the logic-high state with 1.8 volts, the MOS switch is closed since it is designed with $V_{DS1} << 2(V_{GS1} - V_{TH1})$ to operate in the deep triode region. On the other hand, when the D_1 is in the logic-low state with 0 volt, the MOS switch is open. In this circuit,

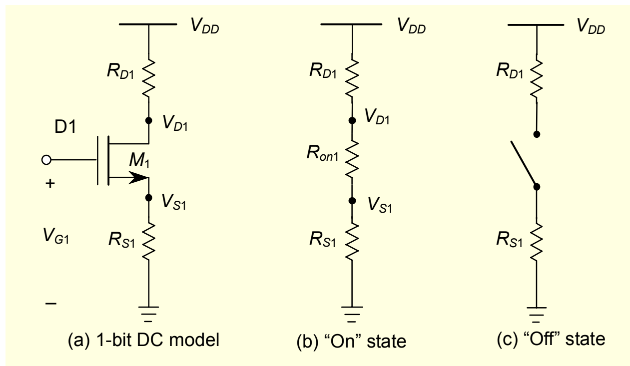

Fig. A1. DC model for 1-bit CMB.

the *on* resistance of the MOS switch expressed in (A1) is designed with approximately 2 ohms. The other DC parameters are described in (A2) to (A5).

$$\frac{V_{DS1(on)}}{I_{DS1(on)}} = R_{on1} = \frac{1}{\mu_n C_{ox}\frac{W}{L}(V_{GS1} - V_{TH1})} \tag{A1}$$

$$V_{S1} = V_{G1} - V_{GS1} = 1.8 - 0.7 = 1.1(V) \tag{A2}$$

$$I_{D1(on)} = 0.05(mA) \tag{A3}$$

$$R_{S1} = \frac{V_{G1} - V_{GS1}}{I_{D1(on)}} = \frac{1.1\ (V)}{0.05\ (mA)} = 22\ (k\Omega) \tag{A4}$$

$$R_{D1} = \frac{V_{DD} - V_{D1}}{I_{D1(on)}} = \frac{V_{DD} - V_{DS1(on)} - V_{S1}}{I_{D1(on)}} = \frac{0.6(V)}{0.05(mA)} = 12\ (\text{k}\Omega) \tag{A5}$$

When $(D_8 \cdots D_2 D_1)$ = $(0 \cdots 01)$, Fig. 4 in section II can be modeled as Fig. A2.

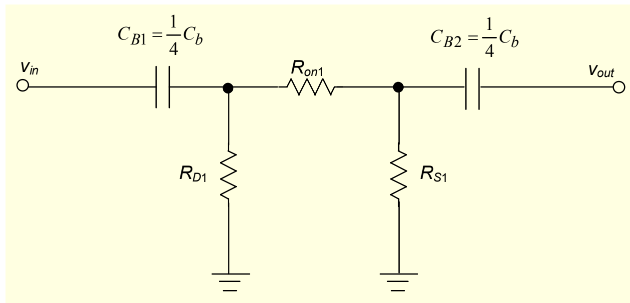

Fig. A2. Small-signal model for 1-bit CMB.

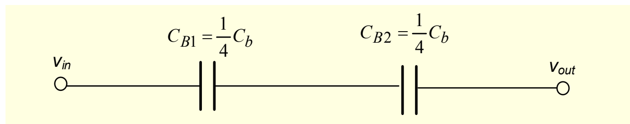

Fig. A3. Equivalent model for Fig. A2.

Since $R_{on1} << \left|(\omega(2/N)C_b)^{-1}\right| << R_{D1}$ and $R_{on1} << \left|(\omega(2/N)C_b)^{-1}\right| << R_{S1}$, we obtain the equivalent model shown in Fig. A3.

From Fig. A3, we obtain

$$C_B = \frac{C_{B1}C_{B2}}{C_{B1} + C_{B2}} = \frac{1}{8}C_b. \tag{A6}$$

When $(D_8 \cdots D_2 D_1) = (1 \cdots 11)$, C_B is expressed as

$$C_B = \left(\frac{1}{8}\right) \times (8C_b) = C_b\,. \tag{A7}$$

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