Low-Power-Adaptive MC-CDMA Receiver Architecture

Mohd. Hasan, Tughrul Arslan, and John S. Thompson

This paper proposes a novel concept of adjusting the hardware size in a multi-carrier code division multiple access (MC-CDMA) receiver in real time as per the channel parameters such as delay spread, signal-to-noise ratio, transmission rate, and Doppler frequency. The fast Fourier transform (FFT) or inverse FFT (IFFT) size in orthogonal frequency division multiplexing (OFDM)/MC-CDMA transceivers varies from 1024 points to 16 points. Two low-power reconfigurable radix-4 256-point FFT processor architectures are proposed that can also be dynamically configured as 64-point and 16-point as per the channel parameters to prove the concept. By tailoring the clock of the higher FFT stages for longer FFTs and switching to shorter FFTs from longer FFTs, significant power saving is achieved. In addition, two 256 sub-carrier MC-CDMA receiver architectures are proposed which can also be configured for 64 sub-carriers in real time to prove the feasibility of the concept over the whole receiver.

Keywords: MC-CDMA, FFT, architecture, VLSI design.

I. Introduction

The crucial design issues for future wireless transceivers are the challenging and contradictory requirements of high performance, low power, and flexibility. The application requirements for wireless systems are quite diverse in terms of changing data rates and bit error rates along with changing bandwidths and other channel parameters like the delay spread. It is essential for wireless transceivers to be adapted to operation rather than being designed for the worst-case channel conditions.

The two blocks consuming the most power in a multi-carrier code division multiple access (MC-CDMA) or orthogonal frequency division multiplexing (OFDM) receiver are the fast Fourier transform (FFT) and the Viterbi decoder [1]. The low-power architectures for these two important blocks have already been investigated [2]-[4]. It is possible to reduce the power consumption further by dynamically reducing the complexity of the receiver architecture in real time as per the changing channel requirements like the delay spread, signal-to-noise ratio (SNR), bandwidth, bit error rate and so on. In [5], the authors have achieved power saving in a Viterbi decoder by dynamically varying its architecture according to real-time changes in system characteristics.

This paper proposes altering the FFT size or inverse FFT (IFFT) size in real time as per the channel delay spread instead of using a fixed large FFT-based transceiver designed for the worst-case delay spread. The FFT/IFFT size in MC-CDMA changes from 16-point to 1024-point [6] depending upon the delay spread, transmission rate, and Doppler frequency. The power saving is significant as it uses the most appropriate FFT/IFFT size instead of a fixed large FFT/IFFT for the worst-case channel conditions. This is achieved by monitoring the channel parameters in real time.

The hardware overhead logic for monitoring the channel parameters is insignificant because this logic has to operate at a

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much lower frequency [5]. Moreover, this logic helps in saving power not only in the FFT but also in other blocks of the receiver like the combiner, the Viterbi decoder and the IFFT block of the transmitter [5].

Two reconfigurable 256-point FFT/IFFT processor architectures are proposed that can also be configured as 64-point or 16-point by disabling the clocks of the higher stages in real time. The two architectures differ only in the extent of clock gating applied to their disabled modules. The power saving for shorter FFTs/IFFTs also depends on the architecture. This concept of dynamic adjustment of hardware size according to changes in the channel parameters in real time is extended to the combiner block of the MC-CDMA receiver. Two reconfigurable 256 sub-carrier MC-CDMA receiver architectures are proposed that can also be configured for 64 sub-carriers to prove the feasibility of the concept over the whole receiver.

II. MC-CDMA

The MC-CDMA receiver [6], a combination of OFDM and CDMA, has a lot of potential in future mobile wireless systems; therefore, power consumption is an important issue. In MC-CDMA, the coded user signal is transmitted on multiple sub-carriers. If the processing gain is equal to the number of sub-carriers, this system modulates all the sub-carriers with the same coded bit, but with a phase shift on each sub-carrier determined by the spreading code. This multi-carrier modulation can also be implemented using an IFFT. If the k-th chip of the spreading code for user u is defined as $c(k,u) \in \{-1,+1\}$, then the transmitted baseband signal for the m-th coded data symbol $b(m)$ is

$$x(n) = \sum_{k=0}^{N-1} \exp(j2\pi kn/N)c(k,u)b(m). \quad (1)$$

The baseband signal is then cyclically extended by more than the channel delay spread to remove inter-symbol interference (ISI). The resulting symbol is then passed through the digital-to-analog converter (DAC) prior to up-conversion through the high-frequency RF carrier. The block diagram of an MC-CDMA transmitter is shown in Fig. 1. By using a guard interval, the receiver selects the portion of the signal that is free from ISI. This

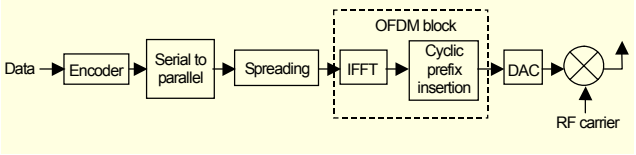

Fig. 1. MC-CDMA transmitter.

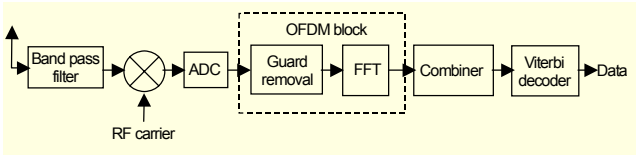

Fig. 2. MC-CDMA receiver.

is then processed by the FFT block to demodulate the sub-carriers.

The channel effect of a multipath channel $h(n)$ at the output of the FFT is narrowband for each sub-carrier, H(k); therefore equalization and de-spreading can be incorporated into a single combining operation to estimate the transmitted data bit. If the output of the FFT block at frequency bin k is defined as $Y(k)$, then the combining operation can be represented by

$$\hat{x}(n) = \text{sign}\{\sum_{k=0}^{N-1} R\{c(k,u)A(k)Y(k)\}\}. \quad (2)$$

The entire receiver structure is shown in Fig. 2. The combiner block is implemented by setting $A(k)$ by (3) for the minimum mean square error (MMSE) solution, where λ is a parameter dependent upon the signal-to-noise level and the number of users.

$$A(k) = H^*(k)/(|H(k)|^2 + \lambda) \quad (3)$$

The sign bit of the value obtained after accumulation of the real part of the product of the equalizer coefficients $A(k)$, the FFT output $Y(k)$, and the corresponding CDMA chip $c(k,u)$ over the code length of 64 in (2), is a measure of the received data estimate.

The equalizer coefficients $A(k)$ are obtained by inserting pilot bits in the transmitted bitstream. An MC-CDMA receiver contains three main system blocks: an FFT block to demodulate

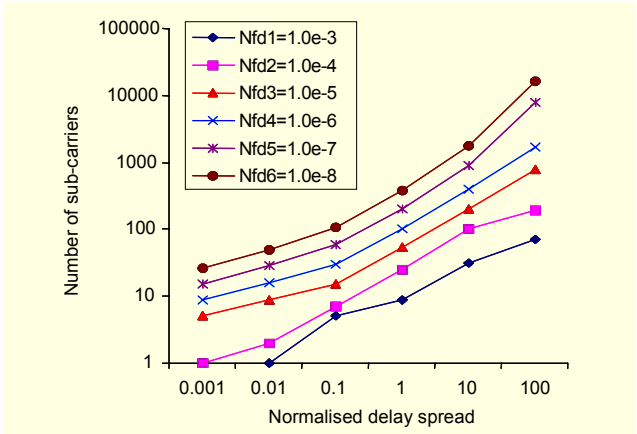

Fig. 3. Optimum number of sub-carriers as a function of normalized delay spread and maximum Doppler frequency.

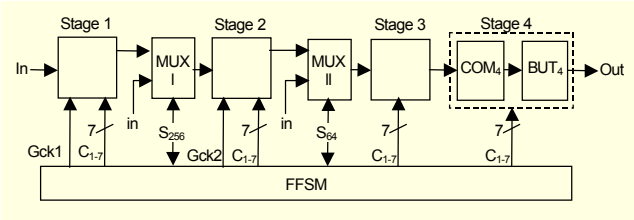

Fig. 4. Architecture of 256-point radix-4 reconfigurable pipelined FFT processor.

the OFDM signals, a combiner block for despreading and equalization, and a Viterbi decoder for decoding the convolutional codes.

III. Variation of FFT Size with Channel Parameters

In a basic OFDM system, a guard interval is inserted in every symbol to overcome the effect of ISI. The guard interval needs to be longer than the delay spread of the channel. The OFDM symbol duration is chosen to be about five times longer than the guard interval for transmission efficiency [1]. The number of sub-carriers (FFT size) is determined by the following:

(OFDM symbol duration-guard interval) × bandwidth.

The number of sub-carriers in MC-CDMA depends upon the delay spread (τ), the maximum Doppler frequency (fd), and the transmission rate (R) [6]. Figure 3 shows the variation of the optimum number of sub-carriers as a function of the normalized value of delay spread (τ×(R×P)), where P is the processing gain for different values of the normalized maximum Doppler frequency Nfd (fd/(R×P)) [6]. It is clear from Fig. 3, that for the intermediate range of τ, fd, and R, the optimum number of sub-carriers varies from 16 to 1024. Only in extreme cases, the optimum number of sub-carriers goes beyond this range.

It is clear that in both MC-CDMA and basic OFDM, the number of sub-carriers depends on the delay spread. The indoor delay spread is measured in the range from 30 ns to 370 ns depending on the building size [1]. The outdoor delay spread is much longer; therefore, it is desirable to design a reconfigurable FFT processor the size of which can be tailored to the channel parameters. The idea is to design the receiver for the maximum number of sub-carriers and then disable unused blocks by clock gating for smaller sizes depending on the delay spread. This approach of hardware size adjustment on the basis of changes in channel parameters in real time is also extended to the combiner block of the receiver. Two 256 sub-carrier MC-CDMA receiver architectures are proposed to study the effect of dynamic adjustment of hardware on the power saving of the whole receiver. This concept can also be extended to the Viterbi decoder to save even more power. Switching to the appropriate FFT size is done automatically by the receiver after reading the channel parameters in real time.

The reconfigurable FFT/IFFT processor is based on Guoan and Jones' radix-4 pipelined architecture [7]. It is better than other pipelined architectures in terms of computational efficiency and hardware savings in complex multipliers, adders, and data stores. It consumes less power due to its lower hardware requirement compared to other radix-4 pipelined architectures [8].

IV. Reconfigurable FFT Processor Architectures

A reconfigurable radix-4 256-point pipelined FFT/IFFT processor architecture is comprised of four radix-4 stages as shown in Fig. 4. Reconfigurability is achieved by inserting two multiplexers, namely MUX I and MUX II, between the higher stages to directly route the input data to stage 2 or stage 3 depending on the required FFT size. The FFT processor can act as a 64-point processor by feeding the input data directly to stage 2 and clocking down the first stage. This is accomplished by selecting the input data rather than the output of stage 1 by the external select input, S_{64}, of MUX I. Moreover, the gated clock input (G_{ck1}) to stage 1 is also disabled by the FFT finite state machine (FFSM).

Similarly, it can act as a 16-point processor by controlling the select input, S_{16}, of MUX II to feed the input data directly into stage 3 and disable stages 1 and 2 with the help of gated clocks G_{ck1} and G_{ck2}. The basic stage of the FFT processor is comprised of a commutator, a butterfly, and a complex multiplier as shown in Fig. 5. The last stage contains just the

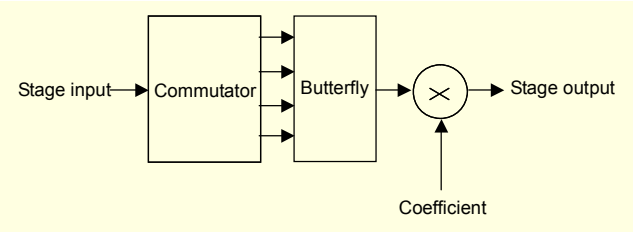

Fig. 5. General stage of a radix-4 FFT processor.

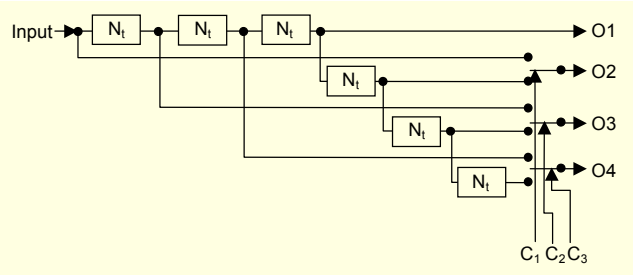

Fig. 6. Radix-4 commutator.

commutator (C5) and the butterfly (B5).

The commutator, shown in Fig. 6 [7], is based on six N_t length FIFOs and three multiplexers. The FIFO block within the commutator structure is realized by using a dual-port RAM to save power consumption. The FIFO size N_t equals $4^{(4-t)}$, where t is the stage number for a 256-point FFT.

The FFSM is responsible for generating all the control signals for all the FFT stages. It is a combination of four different finite state machines (FSMs) with one FSM per stage. Each FSM generates seven control signals, $C_{1\text{-}7}$, for its stage. The MUX I and MUX II select lines are activated by the external inputs S_{256} and S_{64}, respectively, according to the FFT size.

Two different reconfigurable FFT/IFFT processor architectures are proposed depending upon the extent of clock gating. In the first architecture, RFFT-I, clock gating is applied to all the blocks of the commutator including the dual-port RAM-based FIFOs for stages 1 and 2 of the FFT processor. The second FFT processor architecture, namely RFFT-II, is obtained by limiting clock gating to the registers and FSMs of stages 1 and 2 only. This selective clock gating reduces the power overhead of the reconfigurable FFT over the fixed FFT of the same size. The selective clock gating approach reduces power saving in switching from longer to shorter FFTs. This reduction in power saving is due to the power consumed in the dual-port RAM-based FIFOs in the disabled stages. It is important to note that the basic FFT and IFFT architectures are identical.

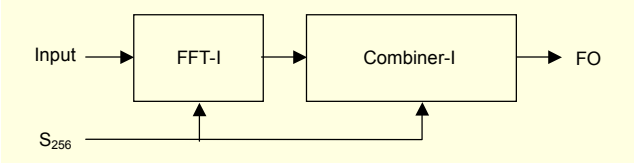

Fig. 7. Receiver-I.

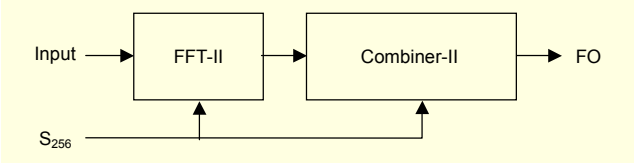

Fig. 8. Receiver-II.

V. Reconfigurable MC-CDMA Receiver Architectures

This paper also presents two 256 sub-carrier MC-CDMA receiver architectures namely receiver-I and receiver-II to prove the applicability of the concept of power saving through dynamic adjustment of hardware for the whole receiver. The difference between the two architectures again lies in the extent of clock gating within their FFT and combiner modules. Clock gating is applied to most of the unused blocks including the dual-port RAMs of the FFT and the combiner in receiver-I, whereas it is selectively applied to only the registers and FSM of receiver-II. The block diagrams of receiver-I and receiver-II are shown in Figs. 7 and 8, respectively. Receiver-I is comprised of a 256-point reconfigurable FFT (FFT-I) and a reconfigurable combiner (combiner-I) with a partitioned equalizer memory that can be partly disabled for a 64 sub-carrier receiver. The reconfigurable FFT-I processor consists of an ordering block (ORD) to restore the digit reversed FFT output to normal order for onward processing. The clock gating in FFT-I is applied to all the blocks of stage 1. It is important to note that the external select input, S_{256}, is used to disable the blocks of both receivers.

Receiver-II is comprised of a 256-point reconfigurable FFT processor, FFT-II, and a reconfigurable combiner, combiner-II, with clock gating limited to intermediate registers and FSMs. The selective application of the gated clock reduces the power overhead of the reconfigurable receiver as compared to the fixed receiver. However, it also brings down the power saving in switching from 256 to 64 sub-carriers. The next subsection discusses the reconfigurable FFT processor architectures, namely FFT-I and FFT-II.

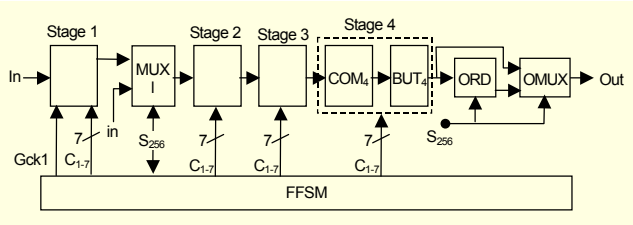

Fig. 9. 256/64 point reconfigurable FFT processor architecture employed in an MC-CDMA receiver.

1. 256-Point Reconfigurable FFT Processor Architecture

The architectures of the reconfigurable FFT processors FFT-I and FFT-II are tailored to the requirements of the reconfigurable MC-CDMA receiver. Since the reconfigurable MC-CDMA receiver assumed here supports only 256 and 64 sub-carriers, only 256-point and 64-point FFT sizes are needed. Moreover, the combiner of the 256 sub-carrier MC-CDMA receiver needs the FFT outputs in normal order. This means that the FFT processors require an additional ordering stage to convert the digit reversed FFT output order to normal order. The architecture of the reconfigurable FFT processor employed in an MC-CDMA receiver is shown in Fig. 9. Both FFT-I and FFT-II have the same basic architecture. Again, the difference lies in the extent of the clock gating. The architecture of FFT-I is similar to RFFT-I in which clock gating is applied to all of the unused modules of the stage 1 commutator including its dual-port RAM. The architecture of FFT-II is similar to RFFT-II,

with clock gating confined to the registers and FSM of stage 1.

An ordering block, shown in Fig. 10, is also needed in the reconfigurable FFT processor to restore the FFT output to normal order to carry out the combining operation for a 256 sub-carrier receiver. The ordering block is comprised of two RAMs, namely RAM0 and RAM1, each having 256 locations to store the 256 words of the FFT. The two RAMs are needed for uninterrupted operation of the pipelined receiver. The first RAM stores the digit reversed output of the FFT, whereas the second RAM sends the previous block of the FFT output in normal order to the combiner for further processing. The roles of the two RAMs are reversed after each 256 clock cycles for real time processing. The address pointer to the RAM which stores the FFT output is generated by a ROM based on the actual location of the digit reversed data, whereas the address pointer to the RAM outputting data to the combiner is generated by a counter. Two multiplexers, namely MUXA0 and MUXA1, are used to select the appropriate address for RAM0 and RAM1, respectively. A multiplexer (MUXD) is used to select the RAM output. An FSM controls the ordering operation by flipping between the RAMs for reading and writing operations. It controls the selected lines of the multiplexers and also has a counter for generating the address. This ordering block is partially disabled in the case of a 64 sub-carrier receiver by keeping its input fixed with the help of a multiplexer IMUX and also by disabling the clock of its FSM in both FFT-I and FFT-II architectures. This is possible because the order of the 64 outputs of the FFT is immaterial for the combiner in the 64 sub-carrier receiver assumed here. The output multiplexer (OMUX) selects either the output of the ORD block or the digit reversed FFT output depending upon the number of sub-carriers. The ORD block is by-passed for the 64 sub-carrier system using the OMUX.

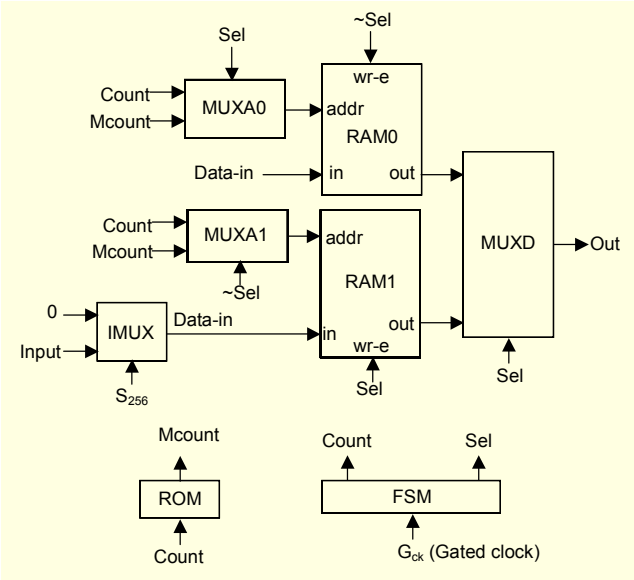

Fig. 10. Architecture for ordering stage of FFT processor.

2. Reconfigurable Combiner Architecture

The reconfigurable combiner can handle both 256 and 64 sub-carriers. The combiner block performs both despreading and equalization of the FFT outputs to recover the transmitted signal. It carries out equalization by first estimating the channel transfer function with the help of some known symbols called pilot symbols. The transmitted data is then recovered by dividing the real part of the received signal by the estimated channel transfer function.

An MC-CDMA data frame is comprised of pilot and data symbols as shown in Figs. 11 and 12 for 64 and 256 sub-carriers, respectively. The known pilot symbols help in estimating the channel transfer function. This transfer function is assumed to remain fixed between the two pilot symbols. A slowly fading channel with a CDMA code length of 64 is assumed. The data is divided into blocks of 32 symbols with the first symbol in each block being used as a pilot for channel estimation. The equalizer coefficients corresponding to all the sub-carriers are computed in the estimation phase. These coefficients are stored in the memory and are used in the data demodulation phase. The equalizer coefficients are assumed to be fixed during the data demodulation phase.

The reconfigurable combiner architecture is shown in Fig. 13. It is comprised of the modules described in the following subsections.

A. Despreading Module

This module is used to multiply the input (FFT outputs) by

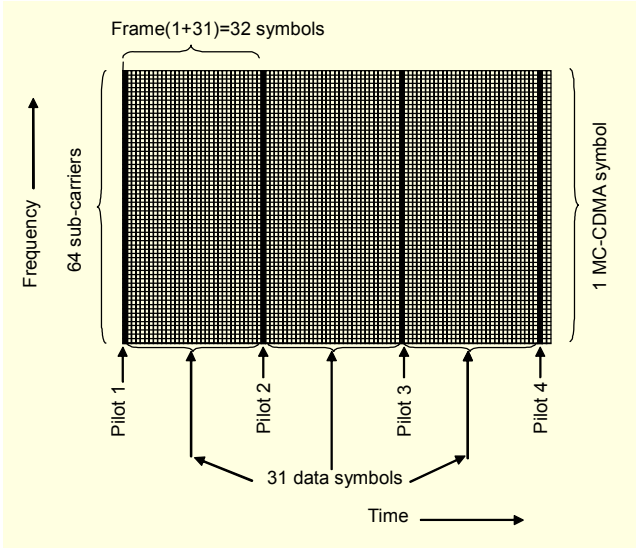

Fig. 11. MC-CDMA frame for 64 sub-carriers.

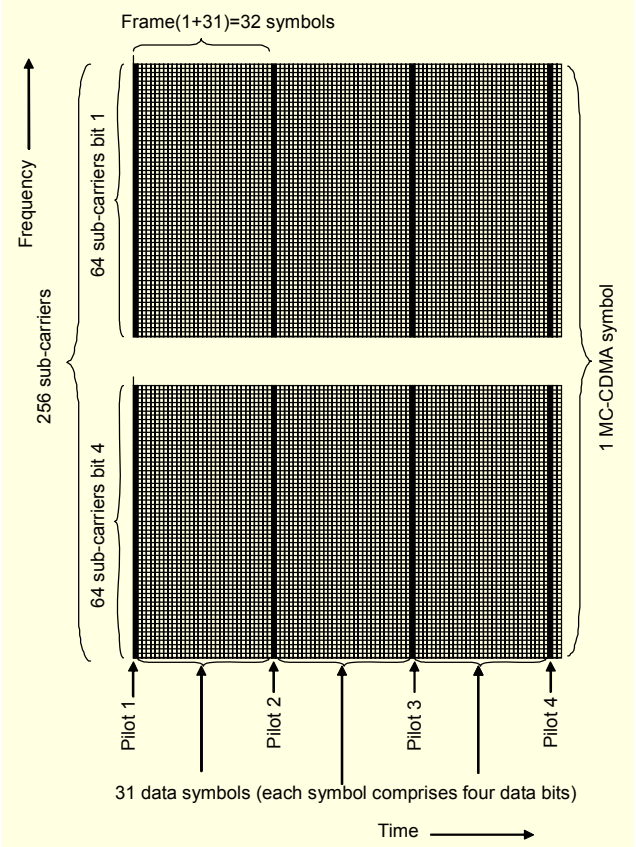

Fig. 12. MC-CDMA frame for 256 sub-carriers.

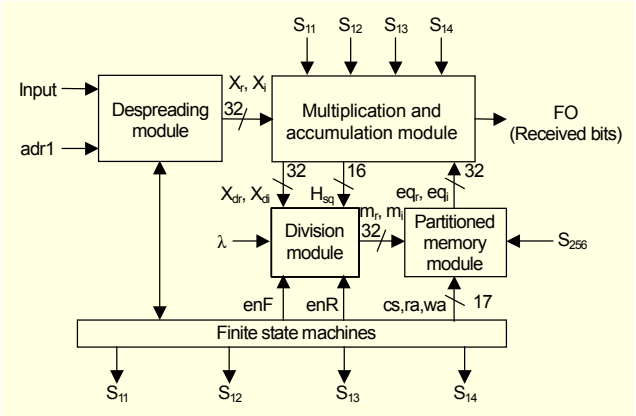

Fig. 13. Reconfigurable combiner architecture.

either +1 or -1, depending on the corresponding chip value. This is done by selectively complementing the input for a chip value of -1 and letting it through for +1. This task can be performed easily by a set of XOR gates with one of their inputs connected to the chip value. The chip values are stored in a 64-bit ROM.

B. Multiplication and Accumulation Module

This module is comprised of two multipliers which are used both in the channel estimation phase and the data demodulation

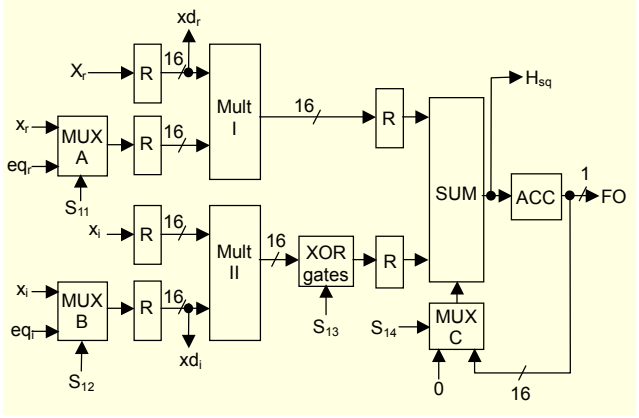

Fig. 14. Multiplication and accumulation module.

phase to reduce power consumption as shown in Fig. 14. In the channel estimation phase, the multipliers Mult. I and Mult. II are fed with the same input, x_r and x_i, respectively, to compute the square of the channel transfer function, H_{sq} ($|H(k)|^2$). This is accomplished by controlling the select inputs, S_{11} and S_{12}, of MUX A and MUX B with the help of an FSM. The control input S_{13} is set to 0 in the estimation phase so that the summation of the two multiplier outputs is performed by the summer (SUM). A summer-based accumulator is used instead of a programmable adder/subtractor to reduce the power consumption. The select input S_{14} in the estimation phase always selects 0 to sum the two multiplier outputs because no accumulation is needed in the channel estimation phase. The output H_{sq} from this module is used for computation of the equalizer coefficients $A(k)$ given in (3). The registers are used at the input of the multipliers to reduce the input switching activity and hence the power consumption. Moreover, registers between the summer and the multiplier are used to reduce the length of the critical path, thereby leading to low power consumption due to less buffering and glitching.

C. Division Module

The division module is used to compute the real and imaginary parts of the equalizer coefficients m_r and m_i, respectively, by using the input pilot symbol and H_{sq} input from the accumulation module. This is shown in Fig. 15 and is required by (3). The real part of the equalizer coefficient m_r is obtained by dividing the real part of the pilot symbol with the summation of H_{sq} and the factor λ. The imaginary part of the equalizer coefficient is obtained by dividing the complement of the imaginary part of the pilot symbol with the previous divisor. The negation of the imaginary part is done to obtain the equalizer coefficient tending towards the reciprocal of the channel transfer function. This is required to remove the channel effects later, and is carried out by multiplying the incoming data block with the equalizer coefficients. The two-

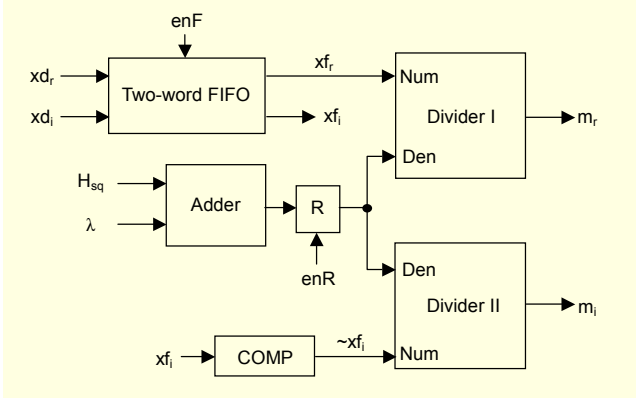

Fig. 15. Division module.

word FIFO block and the register (R) are enabled only during the channel estimation phase by enF and enR signals. This helps to reduce the power consumption by reducing the switching activity at the divider inputs and inside the FIFO block. The FIFO is needed to synchronize the numerator and the denominator of the divisor. A 1's complementer block (COMP) is also needed to generate the complement of the imaginary part of the FIFO output. The division module does not consume much power because it is active only during the short channel estimation phases. Hence, the design is based on two dividers, namely divider I and divider II with N denoting the numerator and D denoting the denominator.

D. Memory Module

The memory module is used to store the equalizer coefficients. The memory size required in a 256/64 sub-carrier system is 256-words. The dual-port RAM is used because of the need for simultaneous read and write operations due to slight overlap of the channel estimation and demodulation phases in the receiver. The unused 192 words of the dual-port RAM are disabled through clock gating in switching from 256 to 64 sub-carriers thereby saving power in the combiner-I architecture.

E. Finite State Machines

The finite state machine module of the reconfigurable combiner is shown in Fig. 16. It consists of two FSMs and a multiplexer. The FSMs, namely FSM_{256} and FSM_{64}, are needed to realize a reconfigurable combiner that can handle both 256 and 64 sub-carriers, respectively. A multiplexer, MUX23, is used to select the appropriate FSM depending on the number of sub-carriers as per the S_{256} control signal. The control signals S_{11}, S_{12}, S_{13}, and S_{14} control the blocks in the multiplication and accumulation module, whereas enabling signals enF and enR control the selective enabling of blocks in

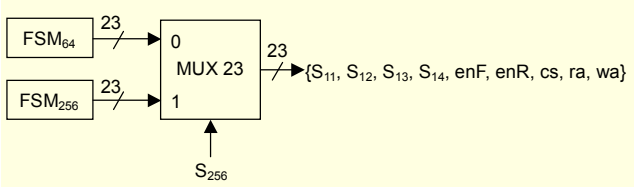

Fig. 16. Finite state machine for reconfigurable combiner.

the division module. The read address (*ra*) and the write address (*wa*) are also generated for the dual-port RAM. The estimation phase for 256 sub-carriers continues for 256 clock cycles, whereas the data demodulation phase lasts for 7936 clock cycles. The accumulator of the multiplication and accumulation module has to be cleared after every 64 accumulations for both 64 and 256 sub-carriers to recover the received bits. The estimation phase for 64 sub-carriers lasts only for 64 clock cycles and the demodulation phase lasts for 1984 clock cycles.

It is clear that power saving occurs both in the FFT and the combiner in switching from 256 to 64 sub-carriers. The first FFT stage can be disabled partially or fully to significantly reduce its power consumption because this stage is not required in a 64 sub-carrier receiver. Similarly, the ordering stage can be partially disabled by keeping its inputs fixed for 64 sub-carriers. Moreover, the 192 words RAM and/or FSM_{256} can also be disabled in the combiner for a 64 sub-carrier receiver, thereby saving power over a fixed receiver.

Two reconfigurable combiner architectures, namely, combiner-I and combiner-II, are proposed for receiver-I and receiver-II, respectively. The 192 words of the dual-port RAM and FSM_{256} are disabled by clock gating for 64 sub-carriers in combiner-I, whereas only FSM_{256} is disabled through clock gating for combiner-II. This means that combiner-II employs limited clock gating, unlike combiner-I.

VI. Results

The reconfigurable 256 sub-carrier MC-CDMA receiver cores, namely, receiver-I and receiver-II; the fixed 256 sub-carrier MC-CDMA receiver; the reconfigurable FFT processor cores, namely RFFT-I and RFFT-II; and the fixed 256-point FFT processor with a word length of 16-bits were designed at the register transfer level (RTL) using Verilog hardware description language. The cores were synthesized using SYNOPSYS DesignCompiler with UMC 0.18 μ standard cell CMOS library. The layouts of the cores were generated using Envisa Silicon Ensemble. This was followed by extracting RC information and then performing RC back-annotated post-layout gate-level netlist simulations for 4000 uniformly distributed random input data samples for all FFT lengths using

the Verilog-XL™ simulator. The resulting switching activity of the circuit nets was then used by the SYNOPSYS DesignPower to compute the power consumption for different FFT sizes. All the simulations were carried out at a clock frequency of 25 MHz and at the supply voltage of 1.8 V. The input data was obtained by modeling the transmitter and receiver in MATLAB for 32 users with a signal-to-noise ratio equal to 40 dB. The results are listed in Tables 1 to 4.

Table 1 lists the power saving for reconfigurable FFTs RFFT-I and RFFT-II as compared to a fixed 256-point FFT. The power overhead is 26% for a 256-point RFFT-I as compared to a fixed 256-point FFT. This power overhead is primarily due to the clock gating of the dual-port RAMs in the commutator. This extensive clock gating in RFFT-I results in power saving of 55% and 85% in switching to 64-point or 16-point FFTs, respectively, as compared to a fixed 256-point FFT processor. The RFFT-I architecture is more suitable for channel conditions where the FFT size required is generally less than the maximum size of 256 points.

Table 1. Power saving between the fixed and the reconfigurable FFT processor architectures.

FFT type	FFT size	Power (mW)	Power saving (%)
Fixed	256	123.01	-
RFFT-I	256	154.62	-26
	64	55.03	55
	16	18.69	85
RFFT-II	256	124.31	-1
	64	91.48	26
	16	70.44	43

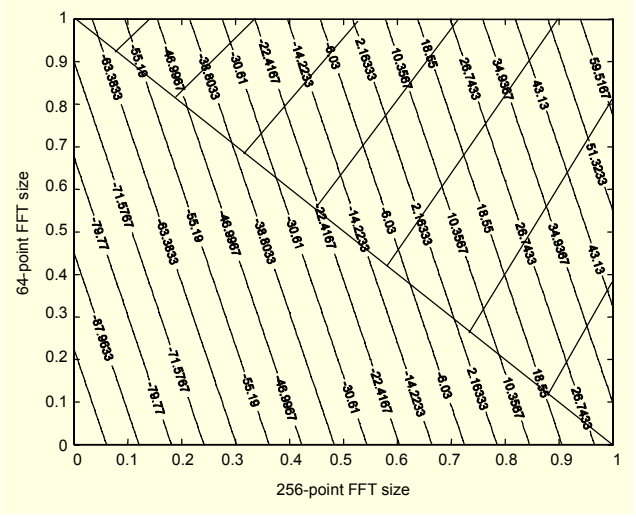

Fig. 17. Power saving for the respective fractional time durations of the corresponding FFT sizes for RFFT-I architecture. The lower un-hatched triangle is only valid because the combined time fractions must be less than or equal to 1 (100%).

The second reconfigurable 256-point FFT architecture, RFFT-II, introduces a power overhead of just 1% as compared to a fixed 256-point FFT processor due to selective clock gating. The clock gating in RFFT-II is limited to the inter-stage registers and FSMs of the commutators. This means that the power overhead in gating the large dual-port RAMs is absent. This limited clock gating yields only 26% and 43% power saving in switching to 64-point or 16-point FFTs, respectively. The RFFT-II architecture is more suitable for channel conditions where the probability of the maximum FFT size (256) is high.

Figures 17 and 18 give the power saving comparison of RFFT-I and RFFT-II architectures as a function of percentage time durations of the various FFT sizes. Only the lower un-hatched triangles in Figs. 17 and 18 are valid because the sum of two FFT size percentages can never exceed 100%. It is clear from these figures that the power overhead of RFFT-I exists for a higher percentage of the maximum FFT size (greater than 75% for 256-point FFT size), whereas this percentage is close to 95% for RFFT-II. It is also evident from the figures that RFFT-II is better than RFFT-I in terms of power saving, provided the probability of the maximum FFT size is more than around 62%. The power saving is around 88% for RFFT-I architecture for 12% duration of a 256-point FFT, 0% of 64-point, and 88% of 16-point, as compared to only 45% power saving for RFFT-II for the same combination. Any of these architectures can be chosen depending on the FFT sizes required over a period of time as per the application.

It is evident from Table 2 that stage 1 of the FFT processor

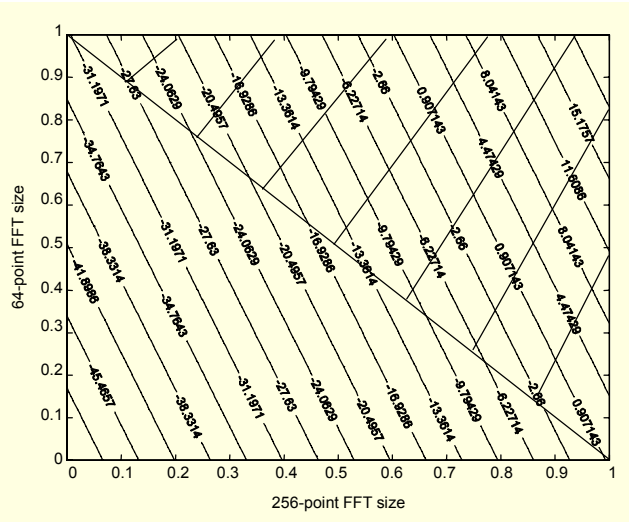

Fig. 18. Power saving for the respective fractional time durations of the corresponding FFT sizes for RFFT-II architecture.

Table 2. Power consumed by the major blocks of the fixed and reconfigurable 256-point FFT processor.

FFT stage	Major blocks in each stage	Fixed FFT power (mW)	RFFT-I power (mW)	RFFT-II power (mW)
Stage1	COM_1	62.90	93.38	63.45
	BUT_1	0.94	0.92	0.94
	MULT	6.11	6.11	6.11
Stage 2	COM_2	18.79	28.05	19.01
	BUT_2	0.91	0.89	0.94
	$MULT_2$	6.15	6.14	6.13
Stage3	COM_3	5.71	5.78	5.79
	BUT_3	0.94	0.98	0.97
	MULT	6.19	6.17	6.17
Stage4	COM_4	1.31	1.30	1.31
	BUT_4	1.50	1.44	1.51
MUX-I	-	-	0.1	0.12
MUX-II	-	-	0.05	0.05

Table 3. Power comparison between the fixed and the reconfigurable receiver.

Receiver type	Receiver size in sub-carriers	Power (mW)	Power saving (%)
Fixed	-	243.66	
Receiver-I	256	285.85	-16
	64	129.45	+47
Receiver-II	256	244.79	-0.5
	64	196.60	+19

Table 4. Power consumed by the major blocks of the fixed and reconfigurable receiver.

Major blocks of receiver	Fixed receiver 256 (mW)	Receiver-I		Receiver-II	
		256 (mW)	64 (mW)	256 (mW)	64 (mW)
FFT	173.78	198.75	92.61	175.04	128.21
Combiner	38.43	53.15	16.95	38.56	36.31

contributes most to the power consumption, followed by stages 2 and 3, and then, the last stage. The power consumed by the stage 1 commutator is the maximum for RFFT-I because clock gating is applied to all the modules of its commutator. The stage 1 commutator power overhead is negligible for RFFT-II as compared to RFFT-I with respect to the fixed FFT because clock gating in RFFT-II is limited to the FSM of its commutator. The same power consumption trend continues for stage 2. Stages 3 and 4 consume identical power for all the architectures due to the absence of clock gating in these stages. The additional logic for reconfiguration in the form of multiplexers MUX-I and MUX-II does not consume much power.

Table 3 lists the power consumed by the fixed and the reconfigurable receiver architectures. Receiver-I, in the 256 sub-carrier mode, consumes maximum power just like RFFT-I as compared to both receiver-II and the fixed receiver. This is because of extensive clock gating in both the FFT processor and the combiner. The power overhead of receiver-I is 16% as compared to only 0.5% for receiver-II. The power overhead of receiver-II is much lower compared to that of receiver-I because the clock gating is limited to only the registers and FSMs of the FFT and the combiner. The power saved by going down to 64 sub-carriers is 47% in receiver-I because the power saving occurs in the commutator, the equalizer RAM, and the ordering block. The power saving is only 19% for receiver-II due to limited power reduction in the commutator and the ordering block, in addition to the small power saving in the combiner due to the disabling of its FSM only.

Table 4 lists the power consumed by the major blocks of the receiver. It is clear that the FFT block consumes most of the power in a MC-CDMA receiver. The power consumed by the FFTs in the receiver goes up considerably after the inclusion of the ordering block ORD.

VII. Conclusion

This paper has presented a novel concept of real-time adjustment of MC-CDMA receiver hardware according to the channel requirements. Two 256 sub-carrier reconfigurable MC-CDMA receiver architectures have been presented which can also be configured for 64 sub-carriers in real time. These architectures can be easily modified to support any other combination of sub-carriers. The power saved by going down to a smaller number of sub-carriers has been clearly established. In addition, two reconfigurable 256-point FFT/IFFT architectures are presented that can also be configured for 64 or 16-points to save power. The power saving occurs both in the transmitter and the receiver due to the presence of an IFFT block in the transmitter. This concept of hardware size adjustment on the basis of changing channel parameters can be extended to other receiver blocks like the Viterbi decoder to save even more power. We envisage designing a fully reconfigurable transceiver for MC-CDMA on the basis of the above concepts.

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