Low-Voltage Current-Sensing CMOS Interface Circuit for Piezo-Resistive Pressure Sensor

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A new low-voltage CMOS interface circuit with digital output for piezo-resistive transducer is proposed. An input current sensing configuration is used to detect change in piezo-resistance due to applied pressure and to allow low-voltage circuit operation. A simple 1-bit first-order delta-sigma modulator is used to produce an output digital bitstream. The proposed interface circuit is realized in a 0.35 μm CMOS technology and draws less than 200 μA from a single 1.5 V power supply voltage. Simulation results show that the circuit can achieve an equivalent output resolution of 9.67 bits with less than 0.23% non-linearity error.

Keywords: CMOS amplifier, current amplifier, resistive readout, interface circuit current sensing, Wheatstone bridge, piezo-resistive sensor.

I. Introduction

Recent advances in CMOS processing and micromachining technologies have allowed various types of microsensor to be integrated with signal processing circuitry in a single chip [1]-[3]. The so-called "smart sensor" is increasingly employed in many applications. A smart sensor basically integrates an on-chip sensor, a front-end readout amplifier, an analog-to-digital converter, and a digital microcontroller in a single chip. With the continuing downsizing of submicron CMOS technology and reduction of power supply voltage, a single-chip smart sensor would require all circuitry to operate under low power supply voltage. Therefore, there is a need for a low-voltage interface circuit, which serves as a bridge between the on-chip sensor and the backend digital processor.

The aim of this work is to realize a low-voltage interface circuit for a CMOS piezo-resistive pressure sensor. The sensor resistance is changed when a pressure variation is applied. The resistance change is traditionally measured by using the Wheatstone bridge circuit, the sensitivity of which depends on the excitation voltage or current. For high bridge sensitivity, high excitation voltage or current is needed, which prevents low-voltage and low-power operation.

In this paper, a new low-power low-voltage interface circuit with digital output is proposed. A current-sensing topology is used to detect the sensor resistance variation and allows low-voltage circuit implementation. The paper is organized as follows. In section II, the circuit configurations for resistive readout, including the traditional Wheatstone bridge, the current-mode Wheatstone bridge, and the proposed low-voltage current-sensing configuration, are described. Sections III and IV describe the architecture and the implementation of the proposed interface circuit, respectively. Simulation results

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and conclusions are given in sections V and VI, respectively.

II. Input Configurations for Resistive Readout

1. Voltage-Sensing Configurations

A. Voltage-Driven Wheatstone Bridge

Traditionally, the voltage-driven Wheatstone bridge configuration is used for the precise measurement of small resistance changes. It is comprised of four resistors connected in a quadrilateral form and an excitation voltage connected across one diagonal of the bridge. The output voltage of the bridge is measured differentially between the voltage divider outputs connected across the other diagonal. The deviation of one or more resistors in the bridge from a nominal value is measured as an indication of change in the measured physical variable, and the output voltage across the bridge indicates the resistance change.

The bridge can have one, two, or four piezo-resistors, whose values are deviated with the applied physical variable, as shown in Fig. 1. Typically, in sensor applications, the nominal values of four resistors are chosen to be equal. The differential output voltage and the end-point linearity error of the bridges in Fig. 1 are summarized in Table 1, where V_{EX} is the excitation voltage to the bridge. The linearity error is calculated as the maximum error in percentage full scale from a straight line that connects the origin and the end point at full scale. Table 1 shows that inherent linearity between the piezo-resistance variation and the output voltage variation can be obtained with the all-element and two-element varying configurations in Fig. 1(a) and Fig. 1(b), respectively. However, linearity error is not critical because it can easily be compensated by using software in digital systems [4]. More importantly, to reduce offset and increase the sensitivity of the sensor, the bridge should have accurate resistance matching among piezo-resistors and equal absolute resistance variation with pressure. These requirements are difficult to achieve in the all-element and two-element varying bridges, not to mention the drawbacks in terms of larger area and cost. The previously mentioned difficulty can be alleviated by using a single piezo-resistor as shown in Fig. 1(d).

One drawback of voltage-driven Wheatstone bridges is that the bridge sensitivity ($S = V_o/(\Delta R/R_0)$ is proportional to V_{EX} and inversely proportional to the baseline resistance of the piezo-resistors. Therefore, to obtain high sensitivity, large V_{EX} and small piezo-resistance are preferred, which prevent low-voltage operation and lead to considerable power consumption of the bridge.

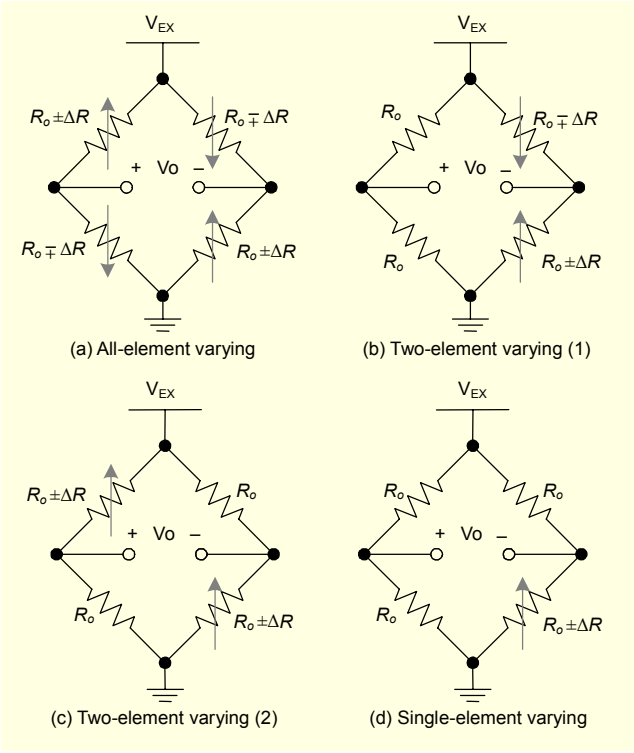

Fig. 1. Voltage-driven Wheatstone bridge configurations.

Table 1. Summary of input configurations for resistive readout.

Input configuration	Output voltage or current	Linearity error (%/%)
Fig. 1(a)	$V_o = V_{EX}\left(\frac{\Delta R}{R_o}\right)$	0
Fig. 1(b)	$V_o = \frac{V_{EX}}{2}\left(\frac{\Delta R}{R_o}\right)$	0
Fig. 1(c)	$V_o = \left(\frac{\Delta R}{2R_o + \Delta R}\right)V_{EX} \approx \frac{1}{2}\left(\frac{\Delta R}{R_o}\right)V_{EX}$	0.5
Fig. 1(d)	$V_o = \frac{1}{2}\left(\frac{\Delta R}{2R_o + \Delta R}\right)V_{EX} \approx \frac{1}{4}\left(\frac{\Delta R}{R_o}\right)V_{EX}$	0.5
Fig. 2(a)	$V_o = (\Delta R)I_{EX}$	0
Fig. 2(b)&(c)	$V_o = \left(\frac{\Delta R}{2}\right)I_{EX}$	0
Fig. 2(d)	$V_o = \frac{R_0}{4}\left(\frac{\Delta R}{R_o + \frac{\Delta R}{4}}\right)I_{EX} \approx \frac{\Delta R}{4}I_{EX}$	0.25
Fig. 3(a)&(b)	$\Delta I = I_1 - I_2 = (\Delta R / R_o)I_{EX}$	0
Fig. 4(a)	$\Delta I = \frac{(V_{EX} - V_{CM})}{R_o}\cdot\frac{(\Delta R / R_0)}{(1 + \Delta R / R_0)} \approx \frac{(V_{EX} - V_{CM})}{R_o}\cdot(\Delta R / R_0)$	1
Fig. 4(b)	$\Delta I = \frac{2(V_{EX} - V_{CM})}{R_o}\cdot\frac{(\Delta R / R_0)}{[1 - (\Delta R / R_0)^2]} \approx \frac{2(V_{EX} - V_{CM})}{R_o}\cdot(\Delta R / R_0)$	0.01

B. Current-Driven Wheatstone Bridge

The Wheatstone bridges can also be driven by a constant current source, as shown in Fig. 2. All current-driven bridges are inherently linear, except for the single-element varying configuration in Fig. 2(d). The sensitivity of current-driven bridges is proportional to the excitation current, I_{EX}. Therefore, a large I_{EX} is required to obtain high sensitivity, which increases the power consumption of the bridge.

2. Current-Sensing Configurations

A. AZKA Cell: A Current-Mode Wheatstone Bridge

As an alternative to the traditional voltage-mode Wheatstone bridge, a current-mode Wheatstone bridge has been proposed based on the circuit dualilty concept [6]. A current-mode dual network for the all-element varying Wheatstone bridge is shown in Fig. 3(a). It is straightforward to show that the current difference, $\Delta I = I_1 - I_2$, is linearly proportional to the change in resistance, ΔR, as shown in Table 1. Due to the circuit duality, the currrent-mode Wheatstone bridge inherits all characteristics and behavior of its voltage-mode counterpart in the current domain, such as sensitivity, linearity, stability, and so on. The input sensitivity is proportional to the constant excitation current value, I_{EX}. Unfortunately, it is not easy to measure ΔI practically; thus, the circuit in Fig. 3(a) is seldom used.

A practical current-mode Wheatstone bridge, shown in Fig. 3(b), has been proposed in [6] and is called the AZKA cell. The circuit uses two resistor elements driven by a constant excitation current. One end of both resistors is tied together, while the other end is forced to be equipotential, that is, $V_1 = V_2$, by a differential current or transimpedance instrumentation amplifier, which can be implemented by a number of

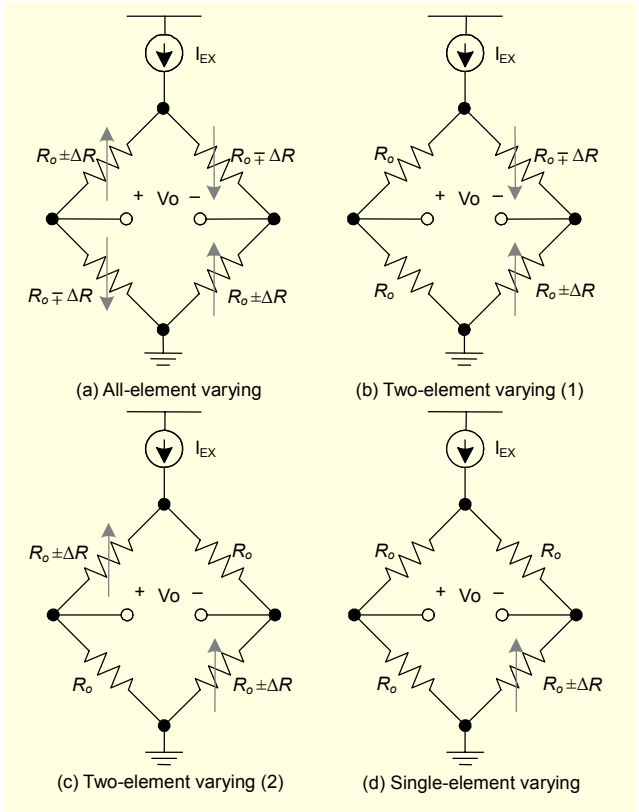

Fig. 2. Current-driven Wheatstone bridge configurations.

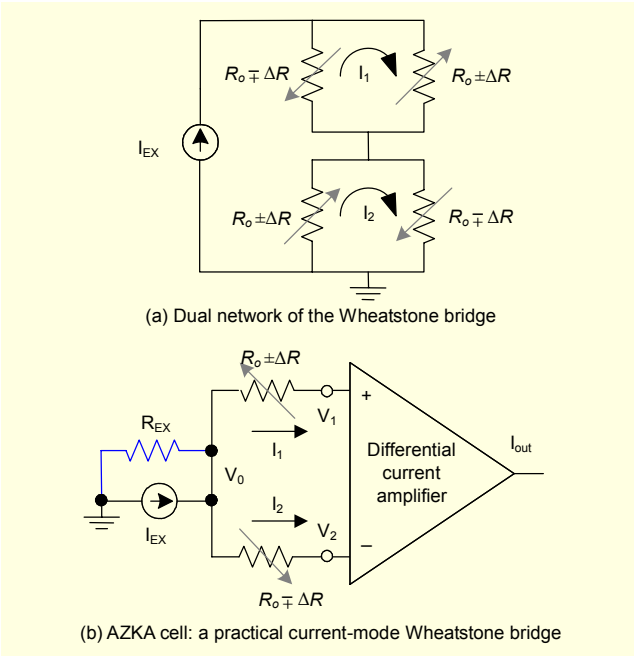

Fig. 3. Current-mode Wheatstone bridge configurations.

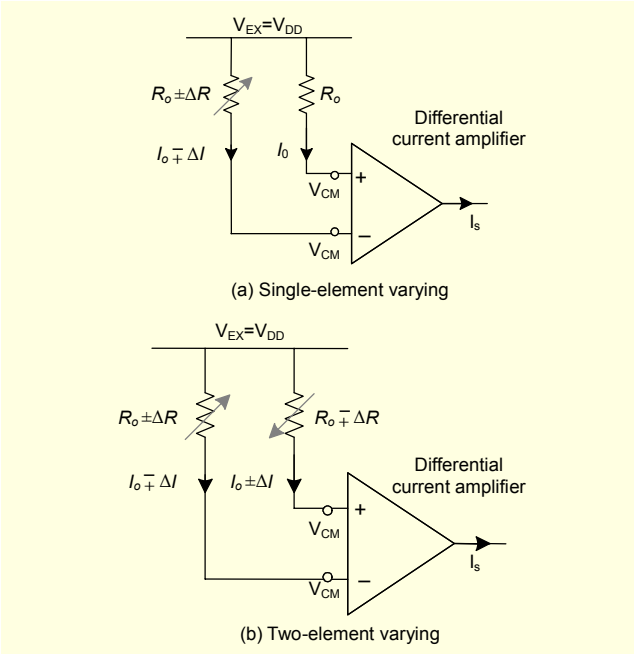

Fig. 4. Proposed low-voltage current-sensing configuration.

circuitarrangements with operational amplifiers, second-generation current conveyors (CCII), or operational floating current conveyors (OFCC) [6], [7]. It can be shown that the circuit in Fig. 3(b) exhibits the same properties and behavior as those of Fig. 3(a), while using only two resistors.

B. Proposed Low-Voltage Current Sensing Configuration

This paper proposes a new current-sensing arrangement suitable for low-voltage integrated circuit implementations.

The proposed configuration, shown in Fig. 4, uses two resistors connected between an excitation voltage, V_{EX} and a fixed input common-mode voltage, V_{CM} of a current buffer. Since the voltages across both resistors are fixed, change in resistance due to applied pressure generates an input current to flow into the current buffer. In this work, V_{EX} is equal to V_{DD} and V_{CM} and is designed to be near V_{DD} to minimize the DC current flowing through both resistors. Figures 4(a) and 4(b) show the proposed configurations with one and two piezo-resistors, respectively. Both resistors have the same baseline resistance, R_0 under no pressure variation. Under a pressure variation, the input current signal and the linearity error of both current-sensing configurations can be summarized as shown in Table 1. The two-element varying configuration has a much lower linearity error. However, as previously mentioned, linearity error can be compensated easily by using backend digital systems; therefore, the single-element varying arrangement is chosen in this work to save cost and area, and to mitigate the resistance matching requirement. In addition, the fixed resistor can be used to compensate for temperature dependence of the piezo-resistor [5].

3. Comparison of Input Configurations

This section compares the input configurations described above. In voltage-sensing configurations, both voltage- and current-driven Wheatstone bridges, the DC common-mode voltage of the following input amplifier is about one half of the power supply voltage (assuming that $V_{EX} = V_{DD}$) due to the voltage divider effect. Under low power supply voltage ($V_{DD} <$ 2V), where the transistor's threshold voltage is a significant portion of V_{DD}, it is not easy to realize a high CMRR amplifier with an input common-mode voltage in the middle of V_{DD}. This may be alleviated by using the current-sensing arrangements shown in Figs. 3 and 4.

Compared with the traditional voltage-mode Wheatstone bridge, the AZKA cell offers a number of advantages, including reduction of resistive sensing elements, summation of sensors' effects (namely, superposition ability), and simple linearization technique [6].

However, the input common-mode voltage of the AZKA cell is determined by the values of I_{EX} and the sensor's baseline resistance, R_0. For high input sensitivity, a large I_{EX} is desired; this may prohibit the use of the AZKA cell for low-voltage operation due to the voltage headroom required by I_{EX}. Furthermore, the voltage at the input coupled node V_0 is varied with the resistance variation, ΔR, as described in (1). Due to finite output resistance, R_{EX}, I_{EX} will fluctuate with input pressure variation; this produces an input-dependent and time-varying non-linearity error, which is not easy to compensate. Providing that $R_{EX} >> R_0$ and $\Delta R << R_0$, this consequence may be insignificant in many circumstances; however, it may not be ignored in low-voltage operation when there is not adequate voltage headroom for I_{EX} and the use of cascode structure is prohibited, rendering R_{EX} not much larger than R_0.

$$V_0 = V_1 + \frac{I_{EX}}{2}\left(R_0 - \frac{\Delta R^2}{R_0}\right) \quad (1)$$

The input sensitivity of the proposed current-sensing configuration in Fig. 4 is proportional to $(V_{EX}–V_{CM})/R_0$, which is the current through R_0. This is similar to the AZKA cell whose sensitivity is proportional to I_{EX}. However, the advantage of the circuit in Fig. 4 is that there is no headroom voltage associated with I_{EX}, making it more suitable for low-voltage operation under the same required input sensitivity.

Input-dependent and time-varying non-linearity may also occur in the circuit in Fig. 4, providing R_0 is not much greater than the Thevenin resistance of the excitation voltage or the supply voltage. Nevertheless, in many circumstances, a low-impedance and well-regulated supply voltage is usually and easily provided. Therefore, under low-voltage operation, the current-sensing arrangement in Fig. 4 is likely to provide superior performance.

III. Architecture of the Proposed Interface Circuit

Using the low-voltage single-element varying current-sensing configuration in Fig. 4(a), Fig. 5 shows the simplified circuit diagram of the proposed interface circuit, which consists of an input current buffer and a 1-bit delta-sigma analog-to-digital converter. The piezo-resistor ($R_P = R_0+\Delta R$, assuming that R_P increases with pressure variation) and the reference resistor, R_0, are connected between the power supply voltage and the input of the current buffer. The input common-mode voltage, V_{CM}, of the current buffer is kept constant due to the negative feedback within the circuit. Thus the voltages across the resistors are constant, and when pressure is applied, it creates a current flow into the current buffer. The current buffer measures the input current differentially and delivers a single-ended output current, I_S, to charge a capacitor, which functions

as an integrator of the following delta-sigma converter. The digital output pulse rate will be proportional to the applied pressure variation. The delta-sigma converter is a synchronized charge-balancing converter suitable for an embedded smart sensor due to its simplicity.

The operation of the circuit can be described as follows. When no pressure is applied, I_S is zero and the capacitor will not be charged or discharged; thus, there is no digital output pulse. Assume that the output of the comparator is low, the switch SW will be open and the current I_S charges the capacitor. The voltage across the capacitor increases until it reaches the reference voltage, V_r. At this instance, the output of the comparator goes to the negative saturation state and the output of the flip-flop goes LOW at the next rising edge of the clock. Then, the switch SW is turned on, thus allowing the capacitor to be discharged with the current I_r–I_S, where I_r is a constant reference current. The capacitor voltage is discharged until it is less than V_r, at which the output of the comparator goes back to the positive saturation state. Then, at the next rising of the clock, the output of the flip-flop goes HIGH and turns off SW and I_r; thus, the capacitor is charged again with I_S.

It can be deduced that the number of digital output pulses (N) over a fixed measuring time interval (T_{int}) is proportional to the value of I_S as described in (2), where T_{CLK} is the digital sampling clock period. The output pulses during T_{int} are counted by a digital counter, which acts as a first-order digital decimation filter, and the total number of pulses is the digital representation of the applied pressure.

$$\frac{I_s}{I_r} = \frac{NT_{CLK}}{T_{\text{int}}} \tag{2}$$

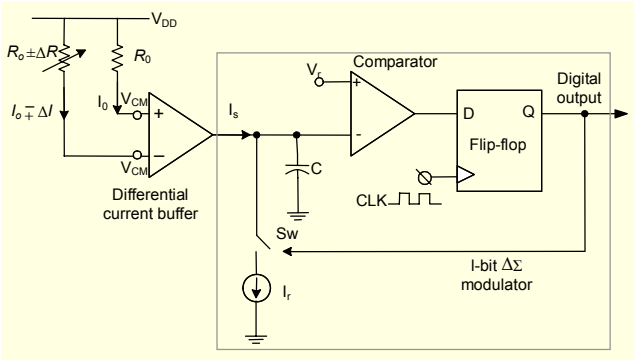

Fig. 5. Proposed low-voltage current-sensing interface circuit.

IV. Proposed Circuit Implementation

1. Differential Input Current Buffer

Figure 6 shows the circuit implementation of the differential input current buffer, which can be described as follows. The input section of the current buffer is realized by M_1-M_4 and DC biased current sources (M_{13}-M_{20}). This kind of circuit has been called the "flipped voltage follower" [8]. The circuit uses negative feedback to achieve small input resistance and to fix the input common-mode voltage, V_{CM}, as given by (2), where $\mu_0 C_{ox}$ is the MOSFET's transconductance parameter and V_{G1}, I_1, V_{TH}, and $(W/L)_1$ are the gate voltage, drain current, threshold voltage, and the aspect ratio of M_1, respectively. Thus, the voltages dropped across both resistors are kept constant to V_{DD}-V_{CM}.

Under a pressure variation, the piezo-resistance is changed, creating an input current (ΔI) into M_4, which is mirrored to M_6. On the other hand, the reference resistor is fixed and does not vary with pressure; thus, a constant common-mode current flows through M_3 and M_5. The common-mode current is subtracted from the input current signal at the output of the current buffer to produce an output current signal which is free of common-mode variation. The accuracy of current mirroring is vital to the linearity and common-mode rejection ratio (CMRR) of the current buffer. Therefore, two auxiliary amplifiers, A_1 and A_2 are used to match the drain-source voltages of M_3, M_5, and M_4, M_6, in order to improve the accuracy of current mirrors. The two amplifiers are identical and are realized by using the conventional two-stage operational amplifier. Transistors M_9-M_{12} realize a cascode current mirror used to eliminate the common-mode component of the input signal.

Note that, although the same circuit functions (that is, detection of resistance change and differential input current) may be obtained with a simpler current differencing circuit [9], which is essentially one of the two identical input sections shown in the dotted box in Fig. 6 with two DC bias current sources, and without the NMOS current mirror, M_9-M_{12}. In this work, we opted for two identical input sections because they provide identical and symmetrical low-input impedance to both inputs, which minimizes input offsets and signal-dependent voltage variations to enhance accuracy and linearity at the expense of increased power dissipation and area.

$$V_{CM} = V_{G1} + \sqrt{\frac{2I_1}{\mu_0 C_{OX}(W/L)_1}} + V_{TH} \tag{3}$$

For DC stability of the following delta-sigma modulator, a DC current, I_2, is added to the output current signal (ΔI) by a current mirror, M_{21}-M_{24}, yielding the final output current, $I_s = I_2 + \Delta I$. Transistors M_{21} and M_{22} also realize a flipped voltage follower to fix the output common-mode voltage of the current buffer for best matching and accuracy of the current mirror.

Since the bandwidth of the pressure signal is in the order of a few tens of hertz, the pressure readout can be sampled with a sufficient sampling rate without any loss of information.

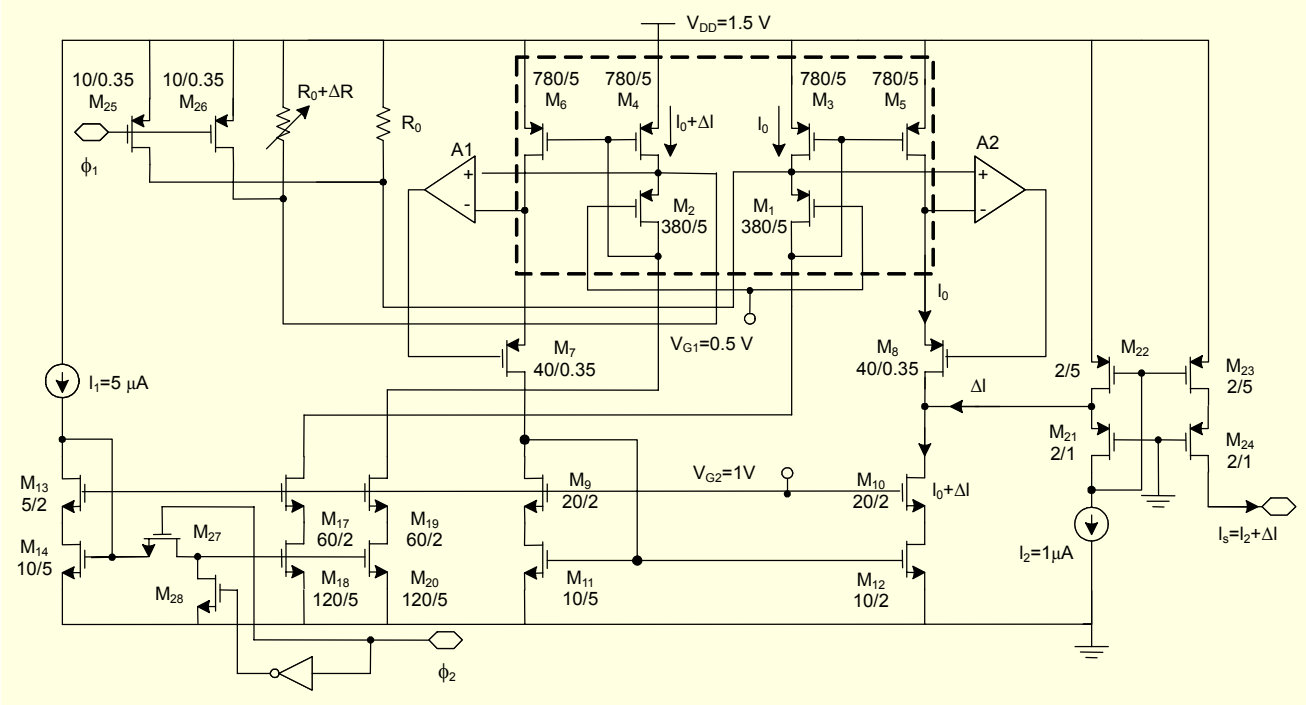

Fig. 6. Differential input current buffer.

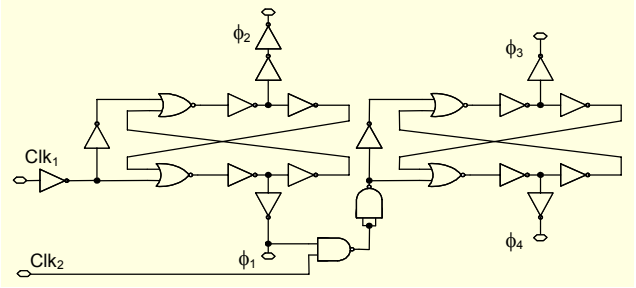

Fig. 7. Clock generator circuit.

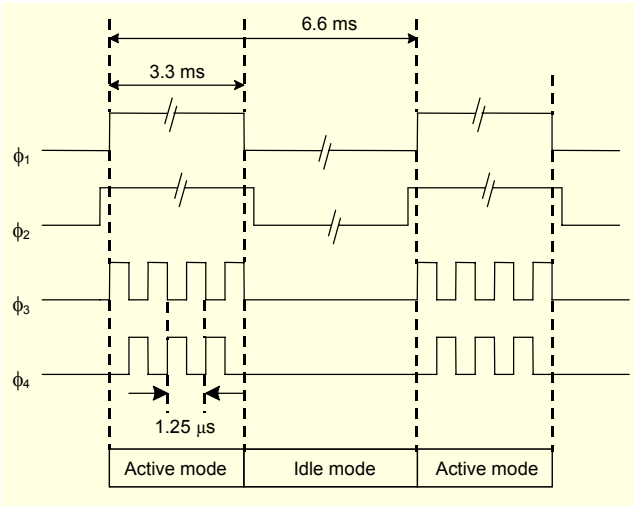

Fig. 8. Timing diagram of clock signals.

Therefore, the circuit operation is controlled by two non-overlapping clock signals, ϕ_1 and ϕ_2, rendering two modes of operation: active and idle modes. In idle mode, ϕ_1 and ϕ_2 are LOW, M_{25} and M_{26} are turned on shorting both resistors, and the input bias current I_1 is turned off to save power and disable the circuit. In active mode, ϕ_1 and ϕ_2 are HIGH, M_{25} and M_{26} are turned off, and I_1 is turned on allowing the circuit to operate and measure the input resistance variation. This scheme allows power saving during the idle interval, which is useful for implantable and battery-operated applications. The clock signals ϕ_1 and ϕ_2 are generated by the circuit in Fig. 7, and its timing diagram is depicted in Fig. 8. In this work, the active sampling clock rate (clk1) and the active time interval (clk2) are chosen as 800 kHz and 3.3 ms, respectively.

2. First-Order Delta-Sigma Modulator

The output current I_s of the current buffer is converted to a digital bitstream by a first order 1-bit delta-sigma modulator as shown in Fig. 9. The circuit consists of an integrating capacitor, C; a reference current source, I_r; and a flip-flop and a dynamic comparator, M_{41}-M_{50}. The capacitor C performs the integration of I_s, yielding the capacitor voltage, V_C. The value of C is chosen so that non-linear clipping does not occur at the desirable maximum input signal amplitude. The dynamic comparator compares V_C with the reference voltage, V_r, and produces the 1-bit output digital bitstream. The comparator

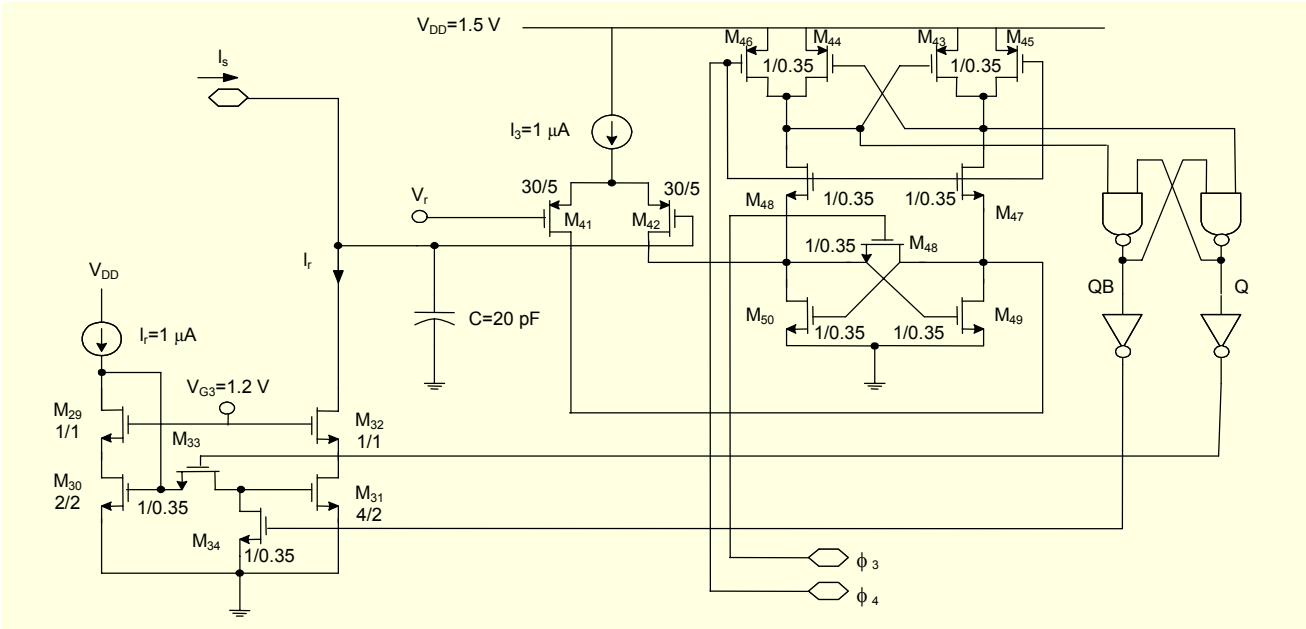

Fig. 9. Circuit diagram of the 1-bit delta-sigma modulator.

[10] consists of a positive feedback differential amplifier and a data latch. Finally, transistors M_{33} and M_{34} switch the current I_r on and off according to the output digital bitstream; thus, performing 1-bit digital-to-analog conversion.

V. Simulation Results

In this work, the proposed interface circuit is targeted for an implantable pressure sensor as in [3], with a sensitivity of 5 μV/V/mmHg. The nominal resistance of piezo-resistance (R_0) is 2.5 kΩ. The maximum change of ±1% from the nominal value is expected from a typical blood pressure range (-500 to +500 mmHg). The circuit was designed to operate with a single 1.5 V power supply, and was simulated using Spectre™ with process parameters from a 0.35 μm CMOS technology. The value of V_{CM} of the input current buffer was set to 1.4 V to minimize the quiescent current flowing through R_0. The value of C was chosen to be 20 pF. Each transistor in the input current buffer was biased to have its drain-source voltage around 0.4 V, except for M_3-M_6 which have 0.1 V.

Main circuit and bias parameters are displayed in Figs. 6 and 7. Bias currents and voltages were provided by on-chip bandgap voltage reference and a regulated cascode current generator with a precision external resistor. In the idle mode, all circuits are powered down, except the bandgap reference, which remains active in order to allow fast recovery return to the active mode.

Figure 10 shows the digital output pulse rate versus the input current and its linear regression. The maximum absolute error,

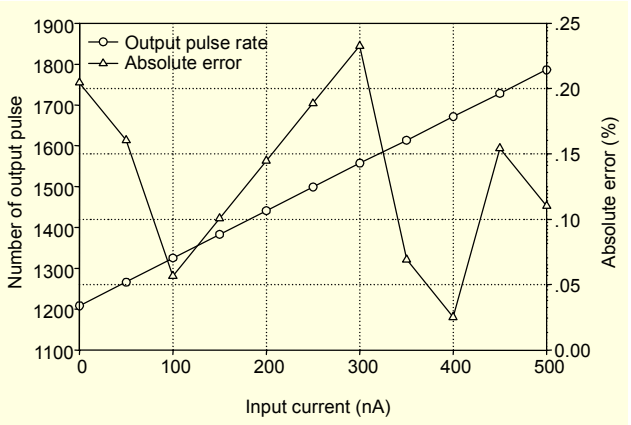

Fig. 10. Number of digital output pulses versus input current.

calculated by the best-fit line method, is less than 0.23% for an input current range of 500 nA, which corresponds to 1% resistance variation of R_0.

Figure 11(a) shows the waveforms of the capacitor voltage and the digital output bitstream, when a 30 Hz 500 nA sinusoidal current is applied to the input. The capacitor voltage does not saturate at the maximum input current amplitude, as desired. Figure 11(b) shows the power spectral density of the output digital data, and the noise-shaping characteristic of the delta-sigma converter is clearly displayed. The in-band noise floor is more than 60 dB below the signal, which is equivalent to an effective number of bits of 9.67. The input-referred noise current, integrated over 30 Hz bandwidth, is equal to 288 nA.

Figure 12 shows the layout of the overall interface circuit,

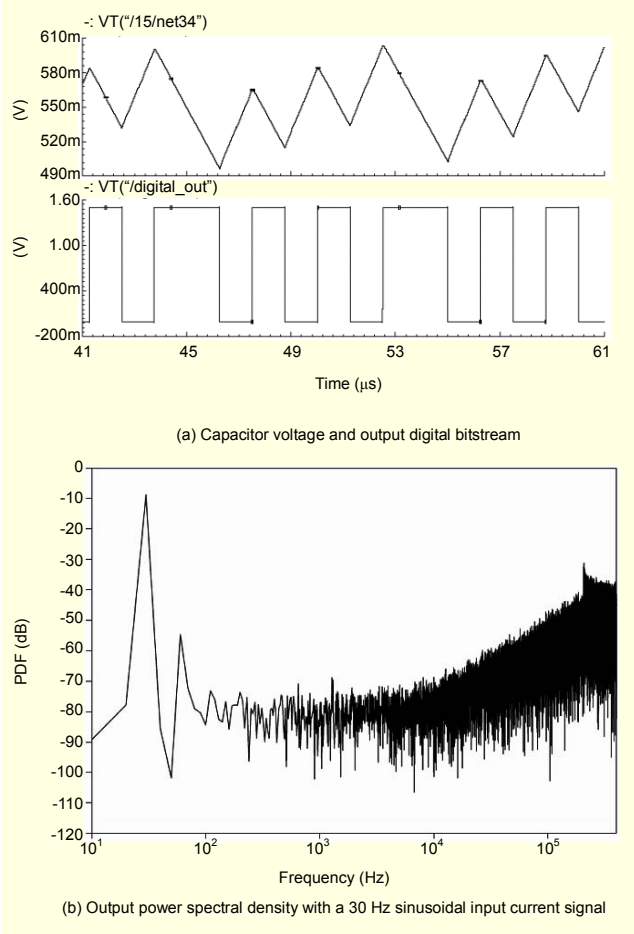

Fig. 11. Output waveforms and power spectral density.

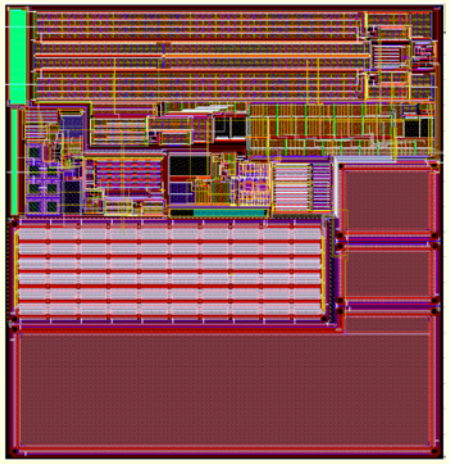

Fig. 12. Layout of the proposed interface circuit.

which occupies 0.2 mm^2 of silicon area. Table 2 summarizes the simulated performance of the proposed circuit. Although the power dissipation of the proposed circuit is not the lowest, it is still on par with those of other sensor interface circuits intended for implantable applications, such as 250 μW in [3].

Table 2. Performance summary of the proposed interface circuit.

Parameters	Value
Supply voltage	1.5 V
Max. linearity error (±1% change in R_P)	0.23%
Effective resolution	9.67 bit
Conversion time	3.3 ms
Power dissipation	270 μW(Active mode)
	13.4 μW (Idle mode)

VI. Conclusion

A low-voltage CMOS interface for a piezo-resistive transducer has been described. The proposed circuit detects change in piezo-resistance by using a current-sensing configuration and employs a simple first-order delta-sigma modulator to convert the resulting input current to an output digital bitstream. Simulation results shows that the circuit can achieve a 60 dB signal-to-noise ratio with less than 0.25% non-linearity error, while operating with a single 1.5 V power supply. The proposed circuit is suitable for a single-chip CMOS smart sensor.

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