An Offset-Compensated LVDS Receiver with Low-Temperature Poly-Si Thin Film Transistor

Kyungyoul Min and Changsik Yoo

The poly-Si thin film transistor (TFT) shows large variations in its characteristics due to the grain boundary of poly-crystalline silicon. This results in unacceptably large input offset of low-voltage differential signaling (LVDS) receivers. To cancel the large input offset of poly-Si TFT LVDS receivers, a full-digital offset compensation scheme has been developed and verified to be able to keep the input offset under 15 mV which is sufficiently small for LVDS signal receiving.

Keywords: LVDS receiver, poly-Si TFT, offset-compensation.

I. Introduction

Due to its reduced cost and form, system on glass (SoG) is the ultimate display device in which all the display electronics are integrated on the same glass substrate as pixels [1], [2]. Because the display electronics are implemented on a glass substrate, single-crystalline Si substrate is not available. For this reason, low-temperature poly-Si (LTPS) thin film transistors (TFTs) are normally used due their much better performance than that of amorphous-silicon (a-Si) [3].

Poly-Si TFTs, of course, show much poorer characteristics than transistors on single-crystalline Si substrate, obstructing the implementation of high-performance SoG. A much more critical issue with poly-Si TFTs is the large variations in their characteristics such as mobility and threshold voltage. The large variations of poly-Si TFTs are due to the grain boundaries of poly-crystalline silicon substrate [4]. Although several techniques have been proposed to increase the grain size, it is impossible to remove the grain boundary unless the grain size is infinitely large.

Due to the low electro-magnetic interference (EMI), high immunity to noise, and low power dissipation, low-voltage differential signaling (LVDS) is widely used to receive digital image data [5], [6]. An LVDS receiver is typically implemented as shown in Fig. 1(a). The small voltage swing of LVDS, however, poses a great design difficulty when an LVDS receiver is to be implemented with a poly-Si TFT for SoG. The large variations of a poly-Si TFT results in the input offset of an LVDS receiver which can be much larger than the voltage swing of the LVDS input. For the typical pre-amplifier (shown in Fig. 1(b)), the mismatches among the TFTs due to the grain boundaries of poly-Si render a huge input offset which can easily exceed 500 mV. Because the minimum voltage swing of

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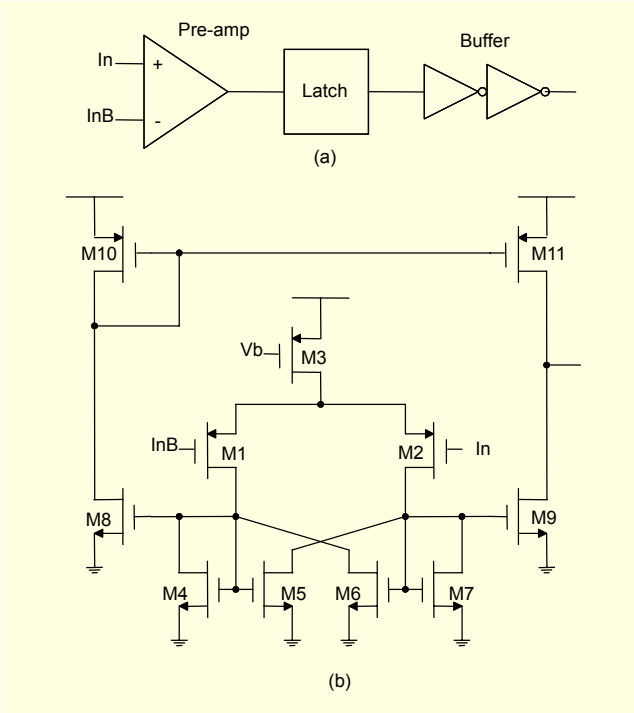

Fig. 1. (a) Typical LVDS receiver and (b) pre-amplifier.

an LVDS receiver is 100 mV, the input offset must be kept under 100 mV for error-free reception of minimum-swing LVDS input [7].

Input offset can be cancelled by storing it on a capacitor and subtracting the stored input offset from the input signal [8]. However, if this type of offset cancellation is employed in a poly-Si TFT LVDS receiver, the data rate will be decreased because of the offset cancellation time. This is critical because even without the offset cancellation time, the maximum achievable data rate with a poly-Si TFT is much lower than that with single-crystalline Si.

In [9] and [10], a digital offset compensation scheme has been proposed with which the input offset can be compensated at power-up and there is no timing loss during normal operation. With the positive and negative inputs shorted, the sign of the input offset is detected and compensated by successive approximation algorithms. This scheme works well for precision comparators and operational amplifiers implemented with single-crystalline Si. For poly-Si TFT LVDS receivers, however, it is very difficult to employ this scheme because the large variations of poly-Si TFTs do not ensure monotonicity of the binary weighted control required for successive approximation. Unlike precision comparators and operational amplifiers, the input offset of an LVDS receiver does not need to be very small but is only required to be smaller than the minimum swing of LVDS signal, that is, 100 mV. Therefore, in this work, a different approach was taken to compensate the input offset of poly-Si TFT LVDS receivers.

II. Offset Compensated Poly-Si TFT LVDS Receiver

As stated above, the input offset of an LVDS receiver is only required to be smaller than the minimum swing of LVDS input. Because the large variations of poly-Si TFT characteristics limit the accuracy of digital offset compensation, the proposed digital offset compensation scheme is not intended to minimize the input offset but to ensure that it is smaller than the minimum LVDS swing.

1. Basic Concept of Full-Digital Offset Compensation

The mismatches among the TFTs in an LVDS receiver appear as an input offset of the pre-amplifier as shown in Fig. 2(a). With the input offset *Vos*, the transfer function of the LVDS receiver is shifted by the *Vos*. If the differential inputs are cross-connected as shown in Fig. 2(b), the transfer function is mirrored along the y-axis and the input offset becomes *Vos*. This fact gives us the basic concept of the proposed digital offset compensation.

If the input offset is to be compensated to less than $|Va|$, the differential inputs are set as $In = Vcm + |Va|/2$ and $InB = Vcm - |Va|/2$. In Fig. 2, the following features can be easily observed:

a) With positive input offset (Fig. 2 solid line)
  1) when $|Vos| > |Va|$,
    - with normal input connection (Fig. 2(a)), *Out* = LOW
    - with cross input connection (Fig. 2(b)), *Out* = LOW
  2) when $|Vos| < |Va|$,
    - with normal input connection (Fig. 2(a)), *Out* = HIGH
    - with cross input connection (Fig. 2(b)), *Out* = LOW
b) With negative input offset (Fig. 2 dotted line)
  1) when $|Vos| > |Va|$,
    - with normal input connection (Fig. 2(a)), *Out* = HIGH
    - with cross input connection (Fig. 2(b)),*Out* = HIGH
  2) when $|Vos| < |Va|$,
    - with normal input connection (Fig. 2(a)), *Out* = HIGH
    - with cross input connection (Fig. 2(b)), *Out* = LOW

From the above, we can make the following observations: a) If the outputs with normal and cross-connected input are different, the offset is smaller than the target value. b) If the outputs are all HIGH, the offset is larger than the target value and positive. c) If the outputs are all LOW, the offset is larger than the target value and negative. Therefore, if the pre-amplifier is configured so that the differential input pair can be cross-connected, the input offset can be monitored and cancelled.

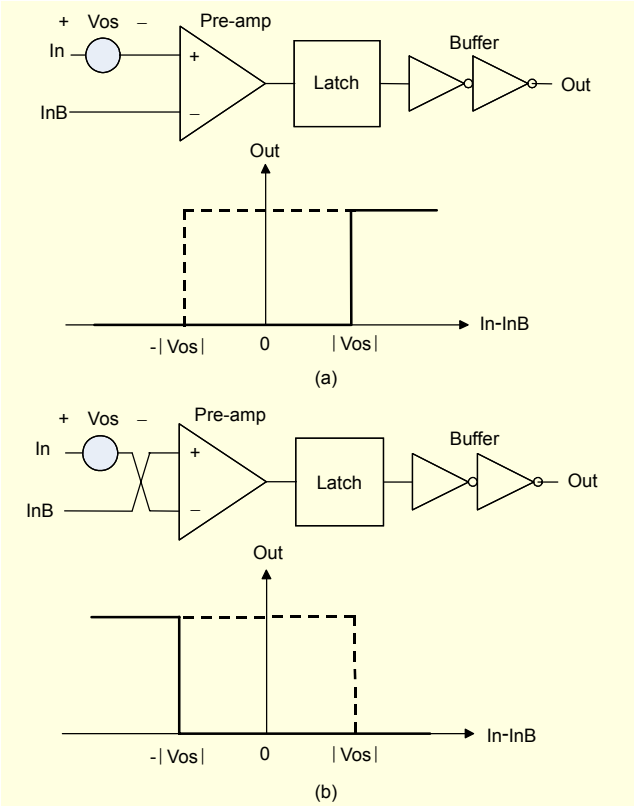

Fig. 2. (a) LVDS receiver with input offset Vos and (b) LVDS receiver with cross connected input (solid-line: positive input offset, dotted-line: negative input offset).

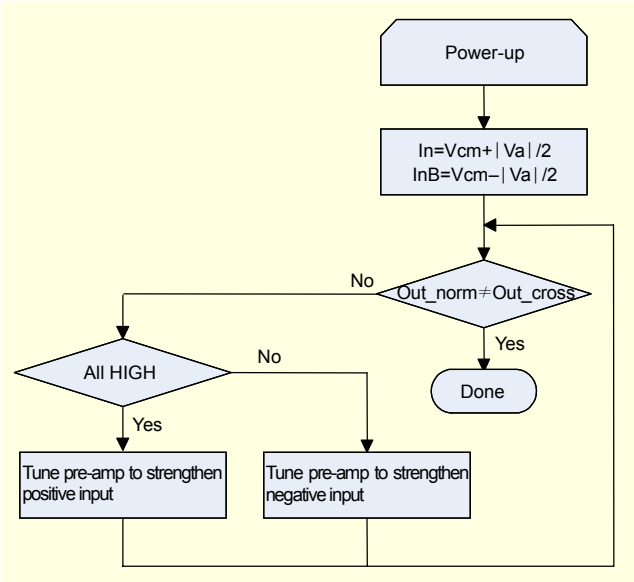

Fig. 3. Conceptual algorithm of the proposed digital input offset compensation.

The offset cancellation algorithm is illustrated as a flow chart in Fig. 3. At power-up, the differential inputs *In* and *InB* are connected to DC voltages *Vcm* + |*Va*|/2 and *Vcm* – |*Va*|/2, respectively. Then, the LVDS receiver output is monitored with the normally- (*Out_norm*) and cross-connected (*Out_cross*) input pair. Depending on the outputs, the strengths of the positive and negative inputs are controlled so that the input offset is compensated.

2. Circuit Implementation

The pre-amplifier is configured so that the positive and negative input side can have different strengths as shown in Fig. 4. With the input transistors M1 and M2 implemented as an array of transistors, the strengths of the positive and negative inputs can be set differently so that the input offset can be compensated. The strengths of the input transistors are calibrated as illustrated in Fig. 3.

With this pre-amplifier, the offset compensated poly-Si TFT LVDS receiver is implemented as shown in Fig. 5. At power-up, the switches S1 and S2 are turned off and the reference voltages *VrefH* and *VrefL* are applied to the LVDS receiver. If the input offset is required to be smaller than |*Va*|, the difference between the two reference voltages *VrefH* and *VrefL* is set to be smaller than |*Va*|. With the switches S4 and S5 turned on, the output of the LVDS receiver is *Out_norm* and *Out_cross* when the switches S3 and S6 are turned on. With the values of *Out_norm* and *Out_cross*, the strengths of the positive and negative input transistors of the pre-amplifier are calibrated until *Out_norm* and *Out_cross* become different, that is, the

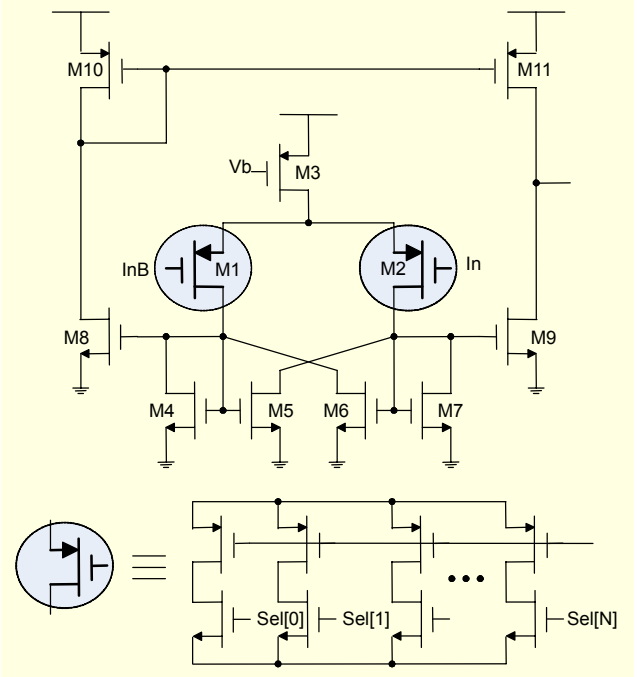

Fig. 4. Pre-amplifier for input offset compensation.

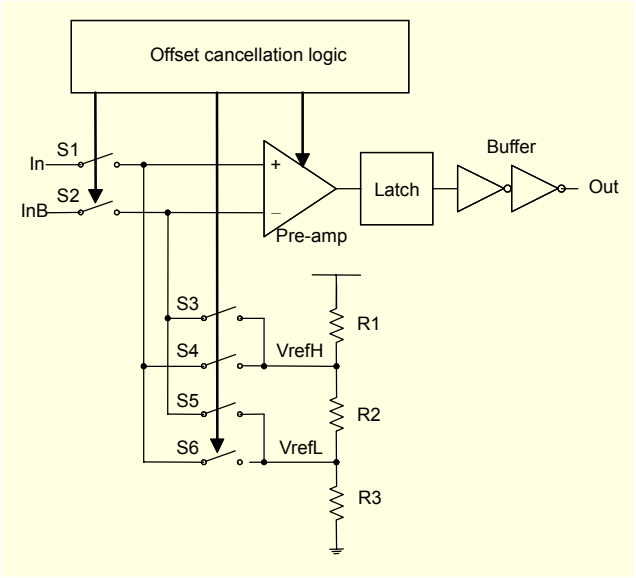

Fig. 5. Offset compensated LVDS receiver.

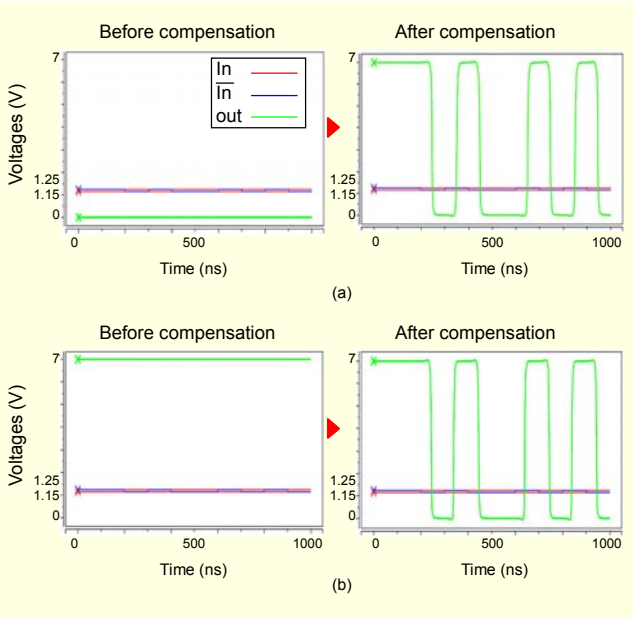

Fig. 6. Simulated waveforms before and after offset compensation with (a) positive input offset and (b) negative input offset.

input offset is smaller than the target value $|Va|$.

III. Simulation Results

The offset compensated LVDS receiver has been designed with a 4 μm minimum channel length low-temperature poly-Si TFT process. According to the measured results of test element group patterns, the threshold voltage and saturation current level can vary more than 65% from the nominal values. With these variations, it is estimated that the input offset of the LVDS receiver can be as large as +/-500 mV while the minimum swing of LVDS is only 100 mV. The reference voltages *VrefH* and *VrefL* are set so that their difference is 30 mV to have sufficiently small input offset after the compensation. The positive and negative input transistors of the pre-amplifier are adjusted to compensate the input offset with 7-bit digital input code generated by the offset compensation logic.

In Fig. 6, the simulated waveforms are shown with 100 mV input swing and 500 mV input offset. Because the input swing is smaller than the offset, the output of the LVDS receiver is stuck at VDD or GND depending on the sign of the input offset. After offset compensation, the input offset is compensated to be smaller than 15 mV; therefore, the correct output can be obtained. Figure 7 shows the input offset of the poly-Si TFT LVDS receiver before and after the offset compensation. The input offset is compensated to be smaller than 15 mV regardless of the initial input offset.

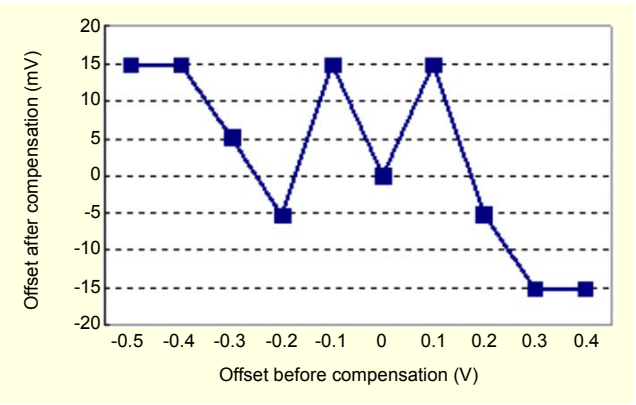

Fig. 7. Input offset of the poly-Si TFT LVDS receiver after full-digital offset compensation.

IV. Conclusion

A poly-Si TFT LVDS receiver has been presented and its large input offset is compensated by a full-digital scheme. Because the offset is compensated at power-up and its result is stored as digital code, during normal operation, there is no need for an offset compensation period; therefore, there is no timing loss. The simulation results show less than 15 mV input offset after the offset compensation. This is sufficiently small for LVDS signal reception.

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