논문 2007-44SC-5-8

PFC 컨버터와 DTC를 이용한 BLDC 모터의 구동 시스템 구현

(Implementation of the BLDC Motor Drive System using PFC converter and DTC)

양 오*

(Oh Yang)

요 약

본 논문에서는 일정 토크영역에서 승압형 PFC 컨버터와 직접토크제어(DTC) 방법을 사용하여 BLDC 모터의 구동 시스템을 DSP(TMS320F2812)로 구현하였다. 기존의 6단계 PWM 전류제어와 달리 미리 정한 샘플시간 마다 간단한 look-up 표로부터 2상 도통 모드에 대한 인버터의 전압 상태 벡터를 설정함으로써 원하는 전류파형을 만들었으며 이로부터 기존의 전류제어기보다 훨씬 빠른 토크 응답특성을 얻을 수 있었다. 또한 BLDC 모터의 비 이상적인 사다리형 역기전력에 의해 발생되는 저주파 토크변동을 저감하기 위하여 위치 loop-up 표를 사용하였다. 아울러 역률을 보정하기 위해 승압형 PFC 컨버터를 구성하였고 이 때 전파 정류된 입력전압과 출력전압, 인덕터의 전류에 의해 평균전류모드 제어 방식으로 80 KHz마다 PWM 듀티(duty)가 조절 되도록 하였다. 이와 같이 복잡한 제어 알고리즘은 초고속 DSP의 출현으로 PFC와 DTC 알고리즘이 동시에 제어가 가능하며, 본 논문에서는 DTC 알고리즘을 구현할 때 DSP의 일반 범용의 출력포트를 사용하여 구현하였고 단지 PFC에서만 1개의 PWM을 사용하여 디지털 제어기를 구현하였다. 실험을 통해 DTC 알고리즘과 PFC 컨버터를 이용한 BLDC 모터 구동 시스템의 타당성과 효용성을 보였고, 실험결과로부터 PFC 컨버터를 사용하지 않았을 때는 역률이 약 0.77이었으나 PFC 컨버터를 사용하였을 때는 부하변동에 관계없이 약 0.9997로 크게 향상됨을 확인하였다.

Abstract

In this paper, the boost Power Factor Correction (PFC) technique for Direct Torque Control (DTC) of brushless DC motor drive in the constant torque region is implemented on a TMS320F2812DSP. Unlike conventional six-step PWM current control, by properly selecting the inverter voltage space vectors of the two-phase conduction mode from a simple look-up table at a predefined sampling time, the desired quasi-square wave current is obtained, therefore a much faster torque response is achieved compared to conventional current control. Furthermore, to eliminate the low-frequency torque oscillations caused by the non-ideal trapezoidal shape of the actual back-EMF waveform of the BLDC motor, a pre-stored back-EMF versus position look-up table is designed. The duty cycle of the boost converter is determined by a control algorithm based on the input voltage, output voltage which is the dc-link of the BLDC motor drive, and inductor current using average current control method with input voltage feed-forward compensation during each sampling period of the drive system. With the emergence of high-speed digital signal processors (DSPs), both PFC and simple DTC algorithms can be executed during a single sampling period of the BLDC motor drive. In the proposed method, since no PWM algorithm is required for DTC of BLDC motor drive, only one PWM output for the boost converter with 80 kHz switching frequency is used in a TMS320F2812 DSP. The validity and effectiveness of the proposed DTC of BLDC motor drive scheme with PFC are verified through the experimental results. The test results verify that the proposed PFC for DTC of BLDC motor drive improves power factor considerably from 0.77 to as close as 0.9997 with and without load conditions.

Keywords: Direct torque control, BLDC motor drive, non-sinusoidal back-EMF, power factor correction (PFC).

Ⅰ. Introduction

Permanent magnet synchronous motor (PMSM) with sinusoidal shape back-EMF and brushless dc (BLDC) motor with trapezoidal shape back-EMF

* 정회원, 청주대학교 전자정보공학부
(School of Electronics and Information Engineering, Cheonju University)
접수일자: 2007년2월12일, 수정완료일: 2007년8월31일

drives have been extensively used in many applications, ranging from servo to traction drives due to several distinct advantages such as high power density, high efficiency, large torque to inertia ratio, and better controllability[1]. Brushless dc motor (BLDC) fed by two-phase conduction scheme has higher power/weight, torque/current ratios and it is less expensive due to the concentrated windings which shorten the end windings compared to three-phase feeding permanent magnet synchronous motor (PMSM)[2]. The most popular way to control BLDC motors is using PWM current control in which a two-phase feeding scheme is considered with variety of PWM modes such as soft switching, hard-switching, and etc. Three hall-effect sensors are usually used as position sensors to detect the current commutation points that occur at every 60 electrical degrees, therefore relatively a low cost drive is achieved when compared to a PMSM drive with expensive high-resolution position sensor, such as optical encoder. In general, ac motor drives have very poor power factor due to the high number of harmonics in the line current. Power factor correction (PFC) method is a good candidate for ac-to-dc switched mode power supply in order to reduce the harmonics in the line current, increase the efficiency and capacity of motor drives, and reduce customers' utility bills. There are two general types of PFC methods to obtain a unity power factor: analog and digital PFC techniques. In the past, due to the absence of fast microprocessors and DSPs, analog PFC methods were the only choice for achieving the unity power factor. Many control strategies using analog circuits have been explored in the past, including average current control[3], peak current control[4], hysteresis control[5], nonlinear carrier control[6], etc. With the recent developments in the microprocessor and DSP technologies, there is a possibility of implementing the complicated PFC algorithms using these fast processors[7].

As compared to conventional analog controllers, digital regulators offer several advantages such as possibility of implementing nonlinear and sophisticated control algorithms, reduction of the number of control components, high reliability, low sensitivity to component aging, better performance than that in analog implementation with the same cost, reduced susceptibility to environmental variations such as thermal drifts, and negligible offsets. Digital control PFC implementations have been investigated by many researchers[8]-[10]. Most of the work have been done are the implementation of the analog PFC techniques in the digital platform. There has been very little work done in the literature to implement the digital PFC methods on ac motor drives. The basic idea of the proposed PFC method in this paper is to update the required amount of duty cycle for boost converter in every sampling time of the DTC of BLDC motor drive.

In this paper, the principle of the average current control boost PFC with feed-forward voltage compensation technique is presented in Section Ⅱ. In Section Ⅲ, the proposed DTC of BLDC motor drive in two-phase conduction mode is explained in detail. In Section Ⅳ, the hardware implementation and experimental results of the proposed DTC of BLDC motor drive in two-phase conduction mode using average current control with input voltage feed-forward compensation boost PFC including load disturbance are presented. The conclusion is presented in Section V.

Ⅱ. The average current control boost PFC with feed-forward voltage compensation

The main topology of the power factor pre-regulator based on boost converter includes two parts: rectifier circuit and boost circuit. The block diagram and DSP control stage of the boost PFC using average current control with feed-forward voltage compensation is shown in Fig. 2. As can be seen in Fig. 2, in contrast to the conventional boost circuit, the large filter capacitor of the power factor pre-regulator is placed at the output of the system. As indicated in Fig. 2, three signals are required to implement the control algorithm. These are, the

rectified input voltage Vin, the inductor current Iin, and the dc output voltage Vo. There are two feedback loops in the control system. The average output dc voltage Vo is regulated by a slow response (high bandwidth), whereas the inner loop that regulates the input current Iin is a much faster loop (low bandwidth). For the purpose of digital control of a boost PFC converter, the instantaneous analog signals Vin, Iin, and Vo are all sensed and fed back to the DSP via three ADC channels ADCIN2, ADCIN3, and ADCIN4 at every sampling period, Ts respectively. Then they are converted to the per-unit equivalents using the gain blocks. The per-unit output voltage Vo(pu) is compared to the desired per-unit reference voltage Vref(pu) and the difference signal (Vref(pu)-Vo(pu)) is then fed into the voltage loop controller Gv. The output of the Gv, indicated as B, controls the amplitude of the per-unit reference current Iref(pu) such that for the applied load current and line voltage, the output voltage Vo is maintained at the reference level. Then, it is multiplied by the two other feed-forward components, A and C, to generate the reference current command for the inner current loop. In Fig. 2, the component A represents the digitized per-unit instantaneous input sensed signal Vin and the component Cis one over square of the per-unit averaged input voltage which equals 1/Vdc(pu)2. The derivation of the feed-forward voltage component C is given in Section II. The per-unit reference current command Iref(pu) for the inner current loop has the shape of a rectified sine wave and its amplitude is such that it maintains the per-unit output dc voltage Vo(pu) at per-unit reference voltage Vref(pu) level overcoming load and input voltage disturbances. The difference signal (Iref(pu)-Iin(pu)) is then passed into the current loop controller Gi in which the PWM duty ratio command is generated for the boost converter switch to maintain the per-unit inductor current Iin(pu) at the per-unit reference current Iref(pu) level. The multiplier gain Km whose derivation is provided in Section II is also added to the control block which allows adjustments of the per-unit reference current Iref(pu) signal based on the converter input voltage operating range Vmin-Vmax[11].

For simplicity per-unit system has been used to describe the components and all variables in the control system. Therefore, the voltage and current signals are automatically saved as per-unit (pu) numbers normalized with respect to their own maximum values.

The multiplier gain Km is useful to adjust the reference current at its maximum when the PFC boost converter delivers the maximum load at the minimum input voltage Vin. In Fig. 2, per-unit reference current Iref(pu) is expressed in terms of Km, A, B, and C as follows:

$$I_{ref(pu)} = K_m ABC \tag{1}$$

where A is the per-unit value of the sensed input voltage Vin, B is the output of the voltage PI controller Gv, and C is the inverse square of the averaged input rectified voltage Vdc, respectively.

The average per-unit value Vdc(pu) of the input per-unit voltage Vin(pu) is given as

$$V_{dc(pu)} = \frac{1}{T}\int_0^T V_{\in(pu)}dt \tag{2}$$

where Tis the time period of the input voltage corresponding to the grid frequency which is 60 Hz in this case and Vin(pu) is the per-unit value of the input rectified voltage normalized with respect to its maximum peak value Vmax. In (2), the base value of the per-unit average rectified input voltage Vdc(pu) is also chosen as Vmax.

The maximum value of the average value Vdc of the sine wave input voltage is only 2Vmax/π. Therefore, the final per-unit representation of the average per-unit voltage Vdc(pu) is given by

$$V_{dcx(pu)} = V_{dc(pu)}\frac{V_{max}}{(2V_{\max}/\pi)} = \frac{\pi V_{dc(pu)}}{2} \tag{3}$$

The per-unit inverse voltage Vinv(pu)of the average per-unit component Vdc(pu) of the per-unit input voltage Vin(pu) can be calculated as follows:

For per-unit representation of the average inverse

voltage Vinv, maximum inverse voltage Vinv_max should be found which equals the inverse minimum of the average input voltage 1/Vdc_min = (2Vmin)/π where Vmin is the minimum peak amplitude of the rectified input voltage selected based on the input operating voltage range of the PFC boost converter. Finally, the per-unit value of the inverse voltage Vinv(pu) in terms of Vdc(pu), Vmin, and Vmax is given as

$$V_{inv(pu)} = \frac{\left(\frac{1}{V_{dcx(pu)} V_{dc\_max}}\right)}{V_{inv\_max}} = \frac{2}{\pi V_{dc(pu)}} \frac{V_{min}}{V_{max}} \quad (4)$$

where Vdc_max is the maximum average input rectified voltage equals 1/Vinv_min = 2Vmax/π. In (4), the numerator in parentheses represents the non per-unit value of the inverse average input voltage Vinv. Once the inverse per-unit voltage Vinv(pu) is calculated, the feed-forward voltage component C can be found as

$$C = V_{inv(pu)}{}^2 = \frac{4}{(\pi V_{dc(pu)})^2}\left(\frac{V_{\min}}{V_{\max}}\right)^2 = \frac{4}{(\pi V_{dc(pu)} K_m)^2} \quad (5)$$

where the multiplier gain Km can be expressed using (1) such that the reference per-unit current Iref(pu) is at its maximum when the PFC boost converter delivers the maximum load at the minimum operating input voltage as

$$K_m = \frac{V_{\max}}{V_{\min}} \quad (6)$$

III. Direct torque control of BLDC motor drive using two-phase conduction mode

The key issue in the DTC of a BLDC motor drive in the constant torque region is to estimate the electromagnetic torque correctly.

For a surface-mounted BLDC motor the back EMF waveform is non-sinusoidal (trapezoidal), irrelevant of conducting mode (two or three-phase), therefore (7) and (8) which are given in the stationary reference frame should be used for the electromagnetic torque calculation[12,13].

$$T_{em} = \frac{3}{2}\frac{P}{2}\left\{\frac{d\varphi_{r\alpha}}{d\theta_e} i_{s\alpha} + \frac{d\varphi_{r\beta}}{d\theta_e} i_{s\beta}\right\} = \frac{3}{2}\frac{P}{2}\left\{\frac{e_{r\alpha}}{\omega_e} i_{s\alpha} + \frac{e_{r\beta}}{\omega_e} i_{s\beta}\right\} \quad (7)$$

$$\begin{aligned} i_{s\alpha} &= i_{sa} \\ i_{s\beta} &= \frac{1}{\sqrt{3}}(i_{sa} + 2i_{sb}) \end{aligned} \quad (8)$$

where P is the number of poles, θ_e is the rotor electrical angle, ω_e is the electrical speed, and $\phi_{r\alpha}$, $\phi_{r\beta}$, $e_{r\alpha}$, $e_{r\beta}$, $i_{s\alpha}$, $i_{s\beta}$ are the stationary reference frame (α β-axes) rotor flux linkages, motor back-EMFs, and stator currents, respectively.

In the constant torque region (below base speed) under two-phase conduction mode when the phase-to-phase back-EMF voltage is smaller than the dc bus voltage there is no reason to change the amplitude of stator flux linkage. Above base speed, however, the motor performance will significantly deteriorate because the line-to-line back-EMF exceeds the dc bus voltage, and the stator inductance, Xs, will not allow the phase current to develop quick enough to catch up to the flat top of the trapezoidal back-EMF. Beyond the base speed the desired torque cannot be achieved unless other techniques such as phase advancing, 180 degree conduction, etc[14] are used. Operation of the DTC of a BLDC motor above the base speed is not in the scope of this paper.

Conventional two-phase conduction quasi-square wave current control causes the locus of the stator flux linkage to be unintentionally kept in hexagonal shape if the unexcited open-phase back-EMF effect and the free-wheeling diodes are neglected, as shown in Fig. 1 with dashed lines. If the free-wheeling diode effect which is caused by commutation is ignored, more circular flux trajectory can be obtained similar to a PMSM drive. It has also been observed from the stator flux linkage trajectory that when conventional two-phase PWM current control is used sharp dips occur every 60 electrical degrees. This is due to the operation of the freewheeling diodes. The same phenomenon has been noticed when the DTC scheme for a BLDC motor is used, as shown in Fig.

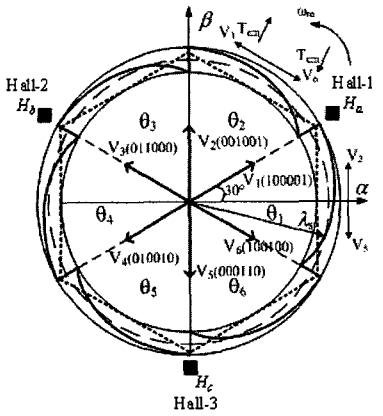


그림 1. 2상 전압 공간벡터.

Fig. 1. Representation of two-phase voltage space vectors.

1 with straight lines. Due to the sharp dips in the stator flux linkage space vector at every commutation and the tendency of the currents to match with the flat top part of the phase back-EMF for smooth torque generation, there is no easy way to control the stator flux linkage amplitude. On the other hand, rotational speed of the stator flux linkage can be easily controlled; therefore fast torque response is obtained. The size of the sharp dips is quite unpredictable and depends on several factors which will be explained in the later part of this section. The best way to control the stator flux linkage amplitude is to know the exact shape of it, but it is considered too cumbersome in the constant torque region. Therefore, in the DTC of a BLDC motor with two-phase conduction scheme, the flux error (ϕ) in the voltage vector selection look-up table is always selected as zero and only the torque error (τ) is used depending on the error level of the actual torque from the reference torque. If the reference torque is bigger than the actual torque, within the hysteresis bandwidth, the torque error (τ) is defined as "1," otherwise it is "-1", as shown in Table 1.

A change in the torque can be achieved by keeping the amplitude of the stator flux linkage constant and increasing the rotational speed of the stator flux linkage as fast as possible. This allows a fast torque response to be achieved. It is shown in this section that the rotational speed of the stator flux linkage can be controlled by selecting the proper voltage

표 1. BLDC 모터에 대한 2상 전압벡터의 선택.

Table 1. Two-phase voltage vector selection for BLDC motor.

τ	θ					
	θ_1	θ_2	θ_3	θ_4	θ_5	θ_6
1	V_2(001001)	V_3(011000)	V_4(010010)	V_5(000110)	V_6(100100)	V_1(100001)
-1	V_5(000110)	V_6(100100)	V_1(100001)	V_2(001001)	V_3(011000)	V_4(010010)

vectors while keeping the flux amplitude almost constant, in other words eliminating the flux control.

Since the upper and lower switches in a phase leg may both be simultaneously off, irrespective of the state of the associated freewheeling diodes in two-phase conduction mode, six digits are required for the inverter operation, one digit for each switch.

Therefore, there is a total of six non-zero voltage vectors and a zero voltage vector for the two-phase conduction mode which can be represented as V1,2 ,…,6 (GPIO1, GPIO2, …., GPIO6), as shown in Fig. 2. The overall block diagram of the closed-loop DTC scheme of a BLDC motor drive with average current control boost PFC in the constant torque region is represented in Fig. 2. In the two-phase conduction mode the shape of stator flux linkage trajectory is ideally expected to be hexagonal, as illustrated with dashed-lines in Fig. 1. However, the influence of the unexcited open-phase back-EMF causes each straight side of the ideal hexagonal shape of the stator flux linkage locus to be curved and the actual stator flux linkage trajectory tends to be more circular in shape, as shown in Fig. 1 with straight lines[13]. In addition of the sharp changes, curved shape in the flux locus between two consecutive commutations complicates the control of the stator flux linkage amplitude because it depends on the size of the sharp dips and the depth of the change may vary with sampling time, dc-link.

Usually the overall control system of a BLDC motor drive includes three hall-effect position sensors mounted on the stator 120 electrical degrees apart, as shown in Fig. 1. These are used to provide low ripple torque control if the back-EMF is ideally trapezoidal because current commutation occurs only every 60 electrical degrees. Nevertheless, using high

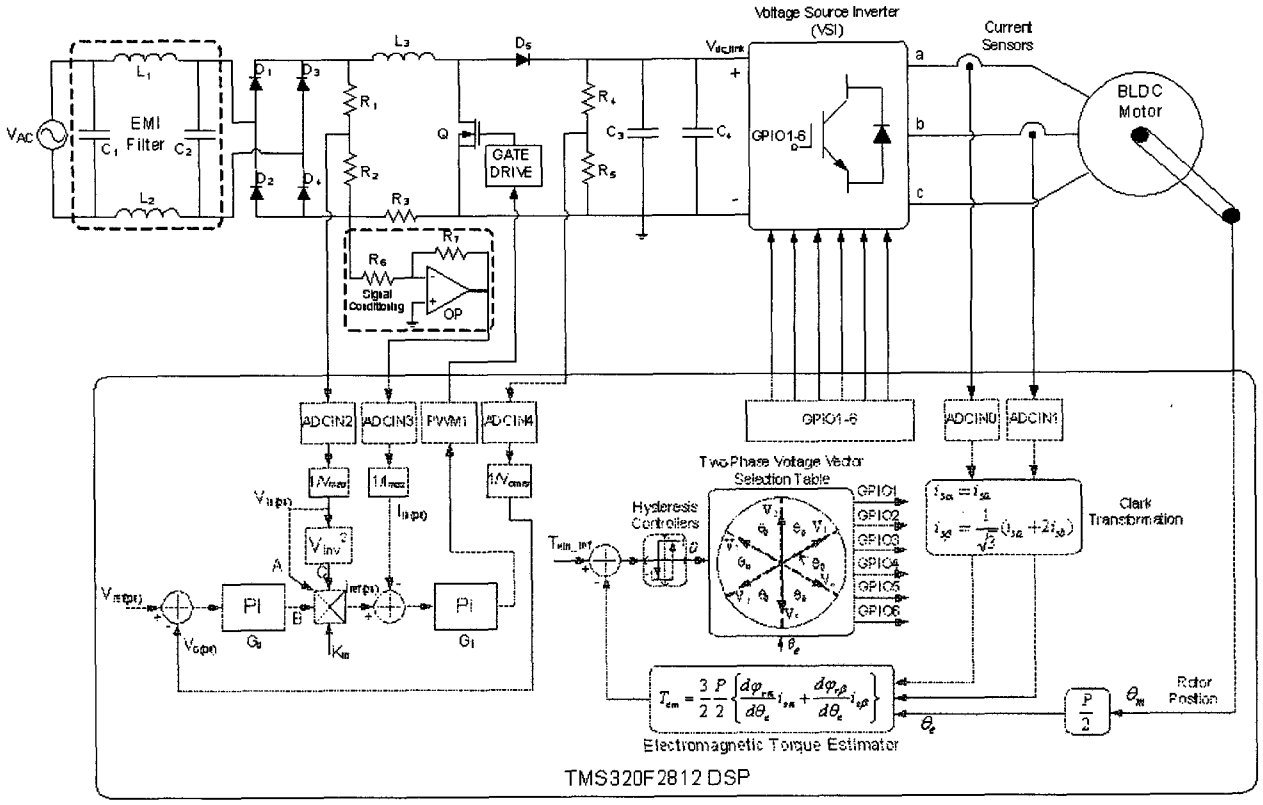


그림 2. 승압형 PFC 컨버터와 DTC를 이용한 BLDC 모터의 구동에 대한 전체적인 구성도.
Fig. 2. Overall block diagram of a BLDC motor drive using the DTC and the boost PFC converter.

resolution position sensors is quite useful if the back-EMF of BLDC motor is not ideally trapezoidal. The derivative of the rotor αβ-axes fluxes over electrical position, which is described in (7) and (8), will cause problems mainly due to the sharp dips at every commutation point.

The $a\beta$-axes rotor back-EMF (e_{ra}, $e_{r\beta}$) vs. electrical position (θ_e) values can be created in the look-up table with great precision depending on the resolution of the position sensor (for example incremental encoder with 2048 pulses/revolution), therefore very accurate $a\beta$-axes back-EMF values and eventually a good torque estimation are obtained.

Ⅳ. Experimental results

The feasibility and practical features of the proposed DTC scheme of a BLDC motor drive with average current controlled boost PFC have been evaluated using an experimental test-bed, shown in Fig. 3. The specifications and parameters of the BLDC Motor are shown in Table 2.

The proposed control algorithm is digitally implemented using the eZdspTM board from Spectrum Digital, Inc. based on a fixed-point TMS320F2812 DSP, as shown in Fig 3(a).

In Fig. 3(b), the BLDC motor whose parameters are given in the Table 2 is coupled to the overall system. The average current controlled boost PFC with feed-forward voltage compensation method has been implemented in single sampling time of the proposed DTC of a BLDC motor drive under two-phase conduction mode in the constant torque region. The boost converter switch is FET47N60C3, and the diode is STTH8R06D. The passive components of the boost converter are the inductor L3 = 1 mH and output filter capacitors C3 = C4 = 270 μF, as seen in Fig. 2.

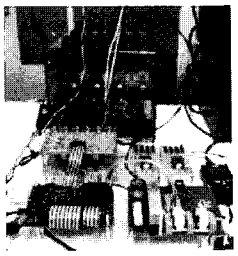
The boost converter switches at 80 kHz which is the sampling frequency of the overall control system and supplies 80 Vdc at the output. The input voltage range, Vmin-Vmax, is 28.28 Vac-70.71 Vac peak.

표 2. BLDC 모터의 사양과 파라미터.
Table 2. Specifications and parameters of the BLDC Motor.

Symbol	Quantity	Value
P	Number of poles	4
VLL	Maximum line-to-line voltage (Vac)	115
Irated	Rated current (A)	5.6
Trated	Rated torque (N·m)	1.28352
Ls	Winding inductance (mH)	1.4
M	Mutual inductance (mH)	0.3125
Rs	Winding resistance (ohm)	0.315
λf	Rotor magnetic flux linkage (Wb)	0.1146

The EMI filter is used in order to reduce the high order switching harmonics in the line current which consists of the inductors L1 = L2 = 10 μH and the capacitors C1 = C2 = 1 μF. Gain of the feed forward path Km = 2.5 was selected in this implementation. In this paper, a digital proportional-integral (PI) controllers are used in the voltage and current loops. The coefficients of the PI voltage and current controllers are chosen as Kpv = 0.1736, Kiv = 0.01388, Kpi = 0.005, and Kii = 0.03125, respectively. One per-unit is 1.146 N·m for torque, 5 A for current, and 1800 rpm for speed, hysteresis bandwidth is 0.001 N·m, and the dead-time compensation is included. In the implementation, over-current and voltage protections have been used for the inductor current and output voltage. Once the sensed inductor current and output dc voltage are higher than 8 A and 140 V, respectively a protection logic signal is generated and used to turn off the gate signal of the boost converter. Steady-state current response of the proposed two-phase conduction DTC scheme of a BLDC motor drive with average current control boost PFC is demonstrated experimentally under 0.4 N·m load torque and 0.573 N·m reference torque.

Fig. 4 shows the measured output voltage, line-voltage, and line-current wave forms from top to bottom, respectively of the two-phase DTC of BLDC motor drive at no load steady-state and 0.4 N·m reference torque without PFC. The power factor under this operating condition is about 0.7667. The



(a) 인버터, DSP 제어보드 및 승압형 PFC 보드.
(a) Inverter, DSP control board, and boost PFC board.

(b) BLDC 모터와 결합된 다이나모미터 및 위치 엔코더.
(b) BLDC motor coupled to dynamometer and position encoder.

그림 3. 실험장치의구성.
Fig. 3. Experimental test bed.

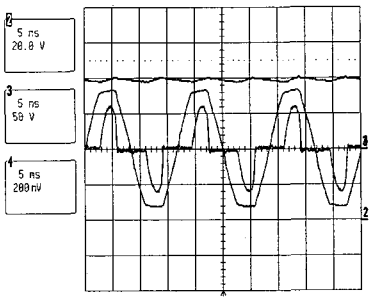


그림 4. 0.4 N·m의 기준 토크와 무부하에서 PFC 없을 때 출력전압 Vo와 선간전압 Vline 및 선간전류 Iline. (상) 출력전압 Vo = 80 V. (중) 선간전압 Vline = 64.53 Vrms. (하) 선간전류 Iline = 1.122 A.
Fig. 4. Output dc voltage Vo, line voltage Vline, and line current Iline without PFC under no load with 0.4 N·m reference torque. (Top) Output dc voltage Vo = 80 V. (Middle) Line voltage Vline = 64.53 Vrms. (Bottom) Line current Iline = 1.122 A.

measured total harmonic distortion (THD) of the line input current and line voltage are 82.23% and 4.79%, respectively. The output active power is 55.3 W.

Since there is no PFC control has been applied to the two-phase conduction DTC of BLDC motor drive, the power factor is poor and the line current has harmonics in it as can be seen in Fig. 4. Moreover, the output dc voltage also has some fluctuations due to the absence of the PFC control. Those problems

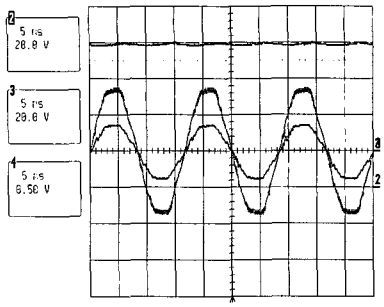


그림 5. 0.4 N·m의 기준 토크와 무부하에서 PFC 있을 때 출력전압 Vo와 선간전압 Vline 및 선간전류 Iline. (상) 출력전압 Vo = 80 V. (중) 선간전압 Vline = 25.43 Vrms. (하) 선간전류 Iline = 2.725 A.

Fig. 5. Steady-state output dc voltage Vo, line voltage Vline, and line current Iline with PFC under no load with 0.4 N·m reference torque. (Top) Output dc voltage Vo = 80 V. (Middle) line voltage Vline = 25.43 Vrms. (Bottom) Line current Iline = 2.725 A.

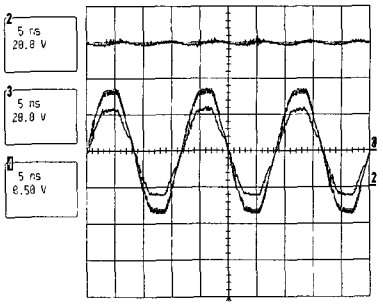


그림 6. 0.573 N·m의 기준 토크와 0.4 N·m의 부하에서 PFC 있을 때 출력전압 Vo와 선간전압 Vline 및 선간전류 Iline. (상) 출력전압 Vo = 80 V. (중) 선간전압 Vline = 25.2 Vrms. (하) 선간전류 Iline = 4.311 A.

Fig. 6. Steady-state output dc voltage Vo, line voltage Vline, and line current Iline with PFC under 0.4 N·m load with 0.573 N·m reference torque. (Top) Output dc voltage Vo = 80 V. (Middle) Line voltage Vline = 25.2 Vrms. (Bottom) Line current Iline = 4.311 A.

can be eliminated by using a PFC control algorithm during a single sampling period of the DTC of BLDC motor drive system.

The output dc voltage, input current, and input line voltage wave forms from top to bottom, respectively of the two-phase DTC of BLDC motor control at no load steady-state with average current controlled boost PFC are shown in Fig. 5. The measured THDs (total harmonic distortion) of the line input current and input voltage are 5.45% and 3.45%, respectively and the measured power factor is about 0.9997. The output active power of the total system is 69.3 W. Since the PFC algorithm is adapted to the overall DTC of BLDC motor drive system, low-frequency oscillations on dc-link voltage is reduced and the line current is more sinusoidal eliminating harmonics as seen in Fig. 5 compared to the ones shown in Fig. 4, thus the power factor and the efficiency of the total system are improved considerably.

Fig. 6 shows the measured output voltage, line-voltage, and line-current wave forms from top to bottom, respectively of the two-phase DTC of BLDC motor control under 0.4 N·m load at steady-state with PFC. The power factor under this operating condition is about 0.9997.

The measured total harmonic distortion of the line input current and line voltage are 5.05% and 3.43%, respectively. The output active power of the total system in this case is 108.6 W. Due to the existence of the load torque, output dc voltage has some distortion as seen in Fig. 6 compared to the dc output voltage shown in Fig. 5.

There has not been a much difference observed in the line currents and line voltages in Fig. 5 and Fig. 6.

V. Conclusion

The digital implementation of the DTC for BLDC motor drive using two-phase conduction mode with average current control boost PFC during a single sampling period of the motor drive system has been successfully demonstrated on the eZdsp board featuring a TMS320F2812 DSP.

A prototype boost PFC controlled by a DSP evaluation board was built to verify the proposed digital control PFC strategy along with the DTC of BLDC motor drive system. Experimental results show that, based on the proposed average current control boost PFC with input voltage compensation algorithm, the power factor of about 0.9997 is achieved in the steady-state under 20 to 50 Vrms

input voltage range conditions.

Moreover, the proposed PFC control strategy can achieve smooth output dc voltage applied to the BLDC motor drive and sinusoidal line current waveform with THD as low as 5%, therefore the power factor and the overall efficiency of the DTC of BLDC motor drive is increased considerably.

References

[1] L. Hao, H.A. Toliyat, "BLDC motor full-speed operation using hybrid sliding mode observer," in Proc. IEEE-APEC Annu. Meeting, Miami, FL, vol. 1, pp. 286-293, Feb. 9-13, 2003.

[2] P. Pillay and R. Krishnan, "Application characteristics of permanent magnet synchronous and brushless DC motors for servo drives," IEEE Trans. Ind. Appl., vol. 27, no. 5, pp. 986 - 996, Sep./Oct. 1991.

[3] P. C. Todd, "UC3854 controlled power factor correction circuit design," U-134, Unitrode Application Note, pp. 3-269 - 3-288.

[4] R. Redl and B. P. Erisman, "Reducing distortion in peak-current-controlled boost power-factor correctors," in Proc. IEEE-APEC Annu. Meeting, Orlando, FL, vol. 2, pp. 576 - 583, Feb. 13-17, 1994.

[5] J. Spangler and A. Behera, "A comparison between hysteretic and fixed frequency boost converters used for power factor correction," in Proc. IEEE-APEC Annu. Meeting, San Diego, CA, pp. 281 - 286, Mar. 7-11, 1993.

[6] R. Zane and D. Maksimovic, "Nonlinear-carrier control for high-power factor rectifiers based on up-down switching converters," IEEE Trans. Power Electron., vol. 13, no.2, pp. 213 - 221, Mar. 1998.

[7] W. Zhang, G. Feng, Y.-F. Liu, and B. Wu, "A digital power factor correction (PFC) control strategy optimized for DSP," IEEE Trans. Power Electron., vol. 19, no. 6, pp. 1474 - 1485, Nov. 2004.

[8] M. Fu and Q. Chen, "A DSP based controller for power factor correction in a rectifier circuit," in Proc. IEEE-APEC Annu. Meeting, Anaheim, CA, pp. 144 - 149, Mar. 4-8, 2001.

[9] S. Buso et al., "Simple digital control improving dynamic performance of power factor pre-regulators," IEEE Trans. Power Electron., vol. 13, no.5, pp. 814 - 823, Sept. 1998.

[10] J. Zhou et al., "Novel sampling algorithm for DSP controlled 2 kW PFC converter," IEEE Trans. Power Electron., vol. 16, no.2, pp. 217 - 222, Mar. 2001.

[11] S. Choudhury, "Average current mode controlled power factor correction converter Using TMS320LF2407A," Texas Instruments Application Note SPRA902A, pp. 1-14, Jul. 2005.

[12] D. Grenier, L. A. Dessaint, O. Akhrif, J. P. Louis, "A park-like transformation for the study and the control of a nonsinusoidal brushless DC motor," in Proc. IEEE-IECON Annu. Meeting, Orlando, FL, vol. 2, pp. 836-843, Nov. 6-10, 1995.

[13] Y. Liu, Z.Q. Zhu, and D. Howe, "Direct torque control of brushless DC drives with reduced torque ripple," IEEE Trans. Ind. Appl., vol. 41, no. 2, pp. 599 - 608, Mar./Apr. 2005.

[14] M. Ehsani, R.C. Becerra, "High-speed torque control of brushless permanent magnet motors," IEEE Trans. Ind. Electron., vol. 35, no. 3, pp. 402 - 406, Aug. 1988.

저 자 소 개

양 오(정회원)

1983년 한양대학교 전기공학과 학사 졸업.

1985년 한양대학교 전기공학과 석사 졸업.

1997년 한양대학교 전기공학과 박사 졸업.

1985년~1997년 8월 LG 산전 연구소 책임연구원

1997년 9월~현재 청주대학교 전자정보공학부 부교수

2006년~2007년 Texas A&M University 방문교수

<주관심분야: 디지털 시스템 설계 및 ASIC 설계, DSP 응용제어>