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Two-loop Hysteretic Control of 3rd Order Buck Converter

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ABSTRACT

In this paper, an analysis and hysteretic controller design of a 3rd order buck converter is presented. The proposed hysteretic controller consists of an inner current-loop, just like the conventional cascade control scheme, and an outer voltage-loop for load voltage regulation. Although it is possible to include an inner current loop from different branches of the converter, from the feasibility and operational point of view, the load side capacitor current would be the better choice. The addition of an inner current-loop improves the dynamic performance of the converter while preserving the robustness of the hysteretic control. The controller formulation and closed-loop converter performance analysis are validated through computer simulations. Few experimental results of the proposed converter are given and compared with the buck converter.

Keywords: Buck converter, Hysteretic control, Input filter, 3rd order buck converter, Voltage regulation

1. Introduction

In recent years, the high frequency switching converters application in low power compact electronic circuits is increasing. As the power conversion system is becoming miniaturized, increasing the power density is one of the challenging issues for the power supply (PS) designers. Lightweight, small size and high power densities with faster dynamic response time are some of the requirements for the power supplies. Different types of topologies have been developed, both in the non-isolated and isolated topologies, to meet the load requirements. For primary as well as secondary bus applications the isolated converters are most suitable, while non-isolated converters give best performance for the point of load (POL) applications. In this paper one such converter, the 3rd order buck converter (TOBC) suitable to the POLA, is proposed.

Several control strategies, including voltage-mode and current-mode, have been reported in literature. Each of these control strategies has their own limitations. However, controller robustness against parameters is one of the important concerns in the field of PS technologies.

Traditionally the hysteretic control[1]-[8] is the robust control. However, robustness can be increased by using an adaptive hysteretic band instead of using a fixed band hysteretic control. Hysteresis control in general can be explained in terms of switching boundaries, in which as long as the output value remains within the boundary [Output $_{(high)}$, Output $_{(low)}$], then it can be said that the output is in normal steady-state condition. The high and low settings can be associated with the switching boundaries that determine the control action and the switch action takes place when the state trajectory crosses the either boundary. When both high and low boundaries

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are used, the region between the two boundaries defines a dead band in which no control action takes place. With simple hysteretic control there are few disadvantages, such as the frequency variation is very large under source and load variations; hence converter elements design becomes problematic. To avoid such large variations in the frequency the authors have proposed a two-loop hysteretic control (TLHC) in this paper.

Conventionally hysteretic control as applied to dc-dc converters consists of sensing only load voltage which is maintained within the switching boundary. At times inductor current along with load voltage is also sensed, making it a two-loop control and several other combinations of TLHC's are also possible depending on which current is included in the control implementation. The proposed hysteretic control here is also a two-loop control, with the second loop being the load side capacitor current loop instead of the inductor current. The theoretical discussion for the formulation of the control logic based on the converter steady-state waveforms is included below, followed by its PSIM[9] simulation results.

As a basis of further comparison, performance of the conventional voltage-mode hysteretic control is also simulated and its results are compared with the proposed controller performance. Both the controllers are being applied to a 3rd order buck converter and its detailed analysis is given in the following lines.

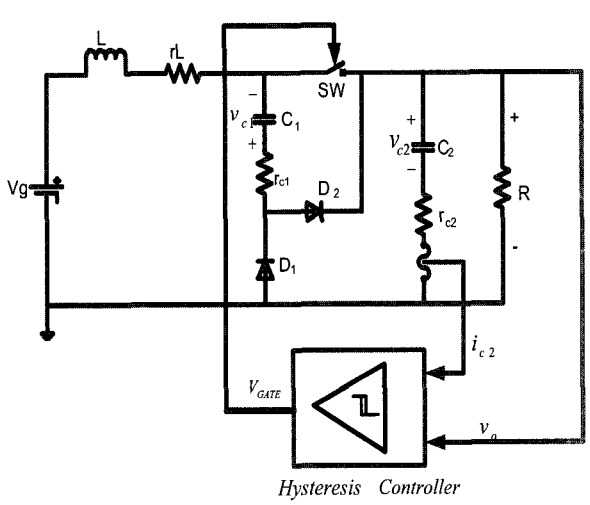


Fig. 1(a) Closed-loop control of 3rd order buck converter

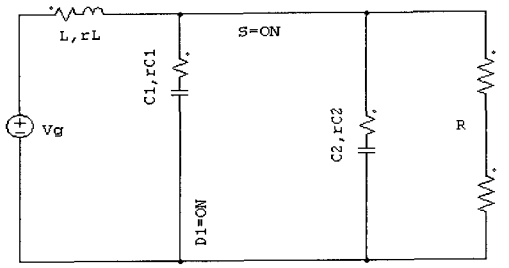


Fig. 1(b) Mode-1 equivalent circuit (S=ON, D_2=OFF)

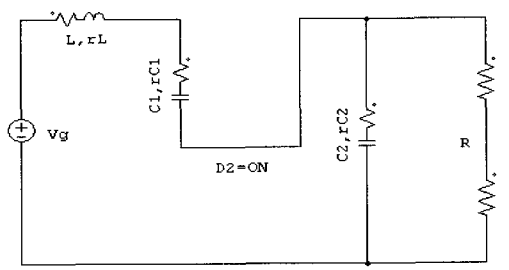


Fig. 1(c) Mode-2 equivalent circuit (S=OFF, D_2=ON)

2. Analysis of 3rd Order Buck Converter

Buck topology is most widely used for step-down applications. However, use of simple buck topology[10] presents high pulsating current stress on the source and in some cases, such as in battery driven applications, it will also affect the source reliability. The buck converter with input filter (BCIF) will be the alternative solution, however it increases the number of inductive energy storage elements and ultimately the analysis of converter dynamics becomes a complex task. It is possible to reduce the number of inductive energy storage elements while retaining the buck conversion property, just by employing one additional diode in place of the inductor and its final circuit connection, TOBC, is shown in Fig. 1. This topology has the following advantages: (i) lower source current ripple, (ii) low EMI, (iii) simpler dynamics than the BCIF, and (iv) simplicity in control due to single switch topology.

This TOBC can be operated in several operating modes depending on the load, switching frequency and supply voltage. However, due to the presence of inductor on the source side, for most of the loads, the converter input current exhibits a lower ripple. Only for very light loadings it does exhibit a higher ripple content and for such light

load applications the proposed converter enters into discontinuous inductor current mode of operation (DICM) and will not provide any benefit as compared to BCIF topology. Hence, converter operation in DICM is of no use for the reasons mentioned above and its operation for continuous inductor current mode (CICM) is discussed here. Necessary theoretical background for TLHC formulation is discussed in Section 3. For CICM operation there are two modes of operation for this converter and they are: (i) Mode-1: 0<t<DT, SW and D_1 are conducting, while D_2 is in OFF-state and (ii) Mode-2: DT<t<T, SW and D_1 are OFF-state, while D_2 is in ON-state. The equivalent circuits for these two modes of operation are shown in Fig. 1(b). In mode-1 operation the load current is supplied by both the source and capacitor 'C_1', while in mode-2 operation it is equal to the inductor or source current. As a result the amount of ripple current flowing through the capacitor 'C_2' increases a little bit as compared to the conventional buck converter. In mode-2 operation the equivalent circuit appears just like a boost converter, with additional series capacitance 'C_1'. In any case, the source is continuously supplying the load and there is no discrete switching from the source point of view. As a result the source ripple current is less as compared to the conventional buck converter.

3. Theoretical Analysis of Proposed Controller

As already mentioned above, the control law formulation is based on the sensing of the load side capacitor current and the load voltage. The ON and OFF criteria of the switch are derived based on the converter steady-state waveforms shown in Fig. 2.

3.1 Switch-ON Criteria

Switch 'S' is switched ON at instant 't_1'. Hence a switching criteria is developed so that $v_o = v_o\ (max)$ at 't_2'. Area A_1 under i_{c2} is integrated from 't_1' to 't_2'. Refer to the waveforms given in Fig. 2:

$$\Delta v_{0,1} = v_{0(max)} - v_0(t_1) = \frac{1}{c_2}\int_{t_1}^{t_2} i_{c2}\,dt \qquad (1)$$

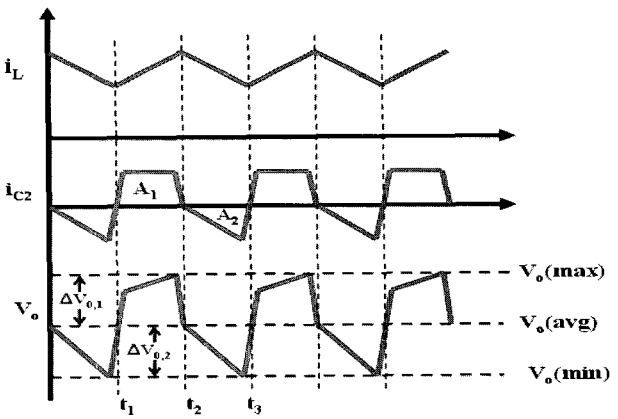


Fig. 2 Converter steady-state waveforms

Now, area A_1 under i_{c2} can be approximated as a rectangle. Hence

$$\int_{t_1}^{t_2} i_{c2}\,dt = length \times breadth = (t_2 - t_1) \times i_{c2}(t_1) \qquad (2)$$

Now during the Switch-ON period;

$$\frac{di_L}{dt} = \frac{1}{L}(v_g - v_o) \qquad (3)$$

Integrating both sides and rearranging the terms we get

$$(t_2 - t_1) = \frac{[i_L(t_2) - i_L(t_1)]}{(v_g - v_0)} L \qquad (4)$$

$$(t_2 - t_1) = \frac{i_{c2}(t_1)}{(v_g - v_0)} L \qquad (5)$$

Since the inductor current ripple can be assumed equal to the capacitor current, thus from (1)

$$v_{0(max)} - v_0(t_1) = \frac{L}{C_2(v_g - v_o)} i_{c2}^2(t_1) \qquad (6)$$

So a criteria is established so that switch 'S' will be Switch-OFF at 't_2' so that 'v_0' won't go beyond $v_{0(max)}$. i.e.

$$v_0(t_1) \geq v_{0(max)} - \frac{L}{C_2(v_g - v_o)} i_{c2}^2(t_1) \quad (7)$$

$$i_{c2}(t_1) \geq 0 \quad (8)$$

Thus the switch will be ON only when the above two conditions (7) and (8) are satisfied, which can be implemented with the help of logic gates and comparators as shown in Fig. 3.

3.2 Switch-OFF Criteria

From the initial ON state before 't_2', Switch 'S' is switched OFF at instant 't_2' Hence again a switching criteria is developed so that $v_o = v_o(min)$ at 't_3'. Area A_2 under i_{c2} is integrated from 't_2' to 't_3'.

Refer again to the waveforms given in Fig. 2:

$$\Delta v_{0,2} = v_0(t_2) - v_{0(\min)} = -\frac{1}{c_2} \int_{t_2}^{t_3} i_{c2} dt \quad (9)$$

Now, area A_2 under i_{c2} can here be approximated as a triangle, Hence

$$\int_{t_2}^{t_3} i_{c2} dt = A_2 = -1/2 \times (base) \times (height)$$

$$= -\frac{1}{2}(t_3 - t_2) \times i_{c2}(t_3) \quad (10)$$

Now during the Switch-OFF period;

$$\frac{di_L}{dt} = \frac{1}{L}(v_g + v_{c1} - v_o) \quad (11)$$

Integrating both sides and rearranging the terms we get

$$(t_3 - t_2) = \frac{[i_L(t_3) - i_L(t_2)]}{(v_g)} L \quad (12)$$

Since under steady state $v_{c1} = v_0$

$$(t_3 - t_2) = \frac{-i_{c2}(t_3)}{v_g} L \quad (13)$$

Since the inductor current ripple can be assumed equal to the capacitor current, thus from (9)

$$v_0(t_2) - v_{0(\min)} = -\frac{L}{2C_2 v_g} i_{c2}^2(t_3) \quad (14)$$

So the criteria is established so that switch 'S' will be again switched to ON at 't_2' so that v_0 will not go below $v_{0(\min)}$, i.e.

$$v_0(t_2) \geq v_{0(\min)} - \frac{L}{2C_2 v_g} i_{c2}^2(t_3) \quad (15)$$

$$i_{c2}(t_1) \leq 0 \quad (16)$$

Thus the switch will be OFF only when the above two conditions (15) and (16) are satisfied which can be implemented with the help of logic gates and comparators. Using equations 7 and 15 the control logic can easily be realized by means of digital logic circuits as shown in Fig. 3.

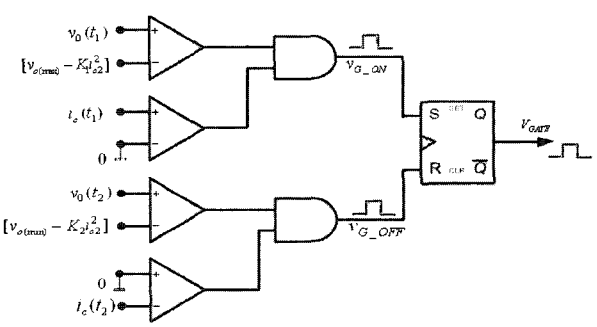


Fig. 3 Layout of proposed two-loop hysteretic control

In the case of simple hysteresis control either the inductor current or load voltage ripple will be the hysteretic band limit for current or voltage control, respectively. But in the case of two-loop hysteretic control the switch-ON/OFF not only depends on the hysteresis band but also depends on the capacitor current and converter parameters as demonstrated by equations 7 and

15. Due to use of capacitor current information in the inner loop, and load voltage in the outer voltage regulation loop, the controller shows the adaptability. As a result this scheme has all the features of the two-loop cascade control in addition to the controller robustness. The justification for the use of the capacitor current in place of the inductor current is as follows:

If the inductor current is used in the hysteresis control the average inductor current will not have any role in finding the actual switching sequence, but the inductor ripple current ultimately defines the control switching sequence. As the load capacitor current is a function of the inductor current, the inductor current ripple information can easily be captured from the capacitor current waveform.

4. Results and Discussions

To verify the developed controller model, a 7.5 Watt TOBC system was designed to supply a constant load voltage of 15 ± 0.25 V from a source voltage of 24 V. The power stage parameters and converter specifications are given in Table 1. With these specifications the converter performance with the proposed logic was studied and simulated using a PSIM electronic circuit simulator[9] as shown in Fig. 4. Firstly, simulation is done with the conventional single loop voltage-mode hysteretic control, shown in Fig. 4. Then the same converter's performance was seen with the TLHC method, by replacing the controller of Fig. 4 with that shown in Fig. 3, based on the sensing of load voltage and the load side capacitor current.

A brief comparison of the two results is also made, which highlights some of the advantages of the later method with the additional capacitor current loop. With these parameters the closed-loop converter system regulation capability is tested for: (i) supply voltage change 20 to 24 V and (ii) load disturbance of 5 to 3 Ω. The load voltage switching boundaries is kept at 15 ± 0.25 V for hysteretic control action and simulation results for these cases are shown in Figs. 5 and 6. In both the cases the load voltage regulation was achieved, but there is a difference in the dynamic response specifications, i.e. the settling time, peak overshoot and frequency variation. The results obtained in the simulations are as tabulated in Table 2 as a comparison between the conventional and improved two loop hysteresis control methods.

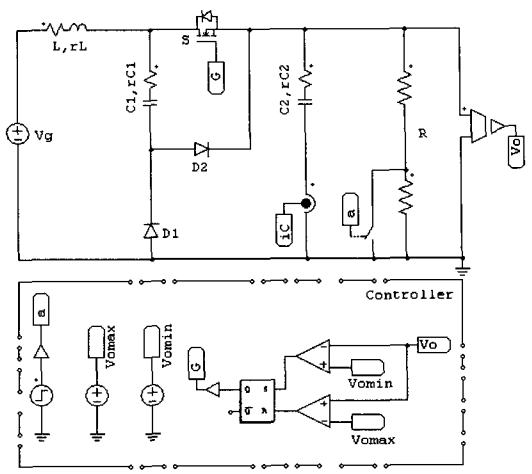
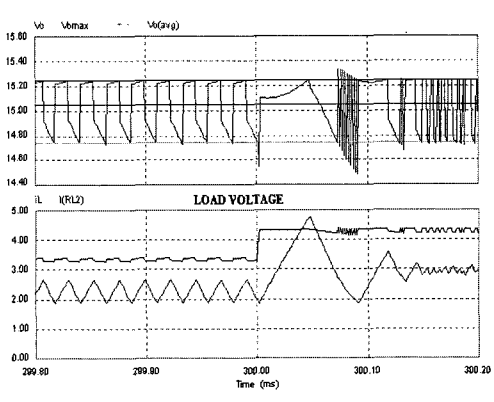


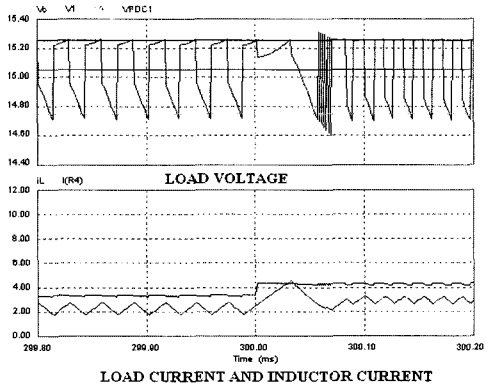
Fig. 4 Simulation diagram of hysteretic controlled converter

Table 1 Converter parameters

CONVERTER SPECIFICATIONS	
V_g	24 V
V_o	15 V ± 0.25 V
P_o	7.5 W
CONVERTER PARAMETERS	
L,	120 μH
C_1	100 μF
C2	200 μF
R_{LOAD}	30 Ω
rL	0.34 Ω
rc1	0.3 Ω
rc2	0.2 Ω

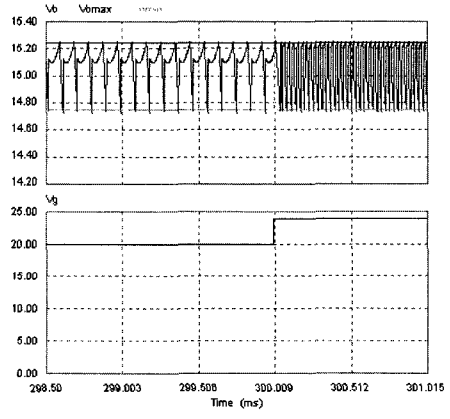


(a) Conventional hysteretic control

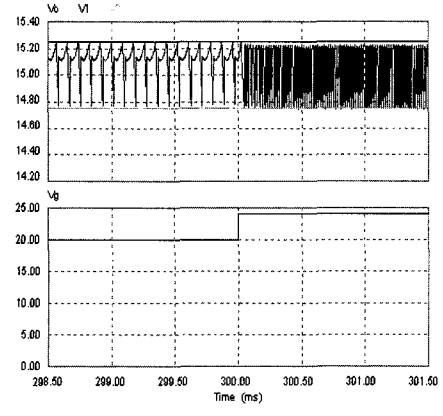


(b) Proposed two-loop hysteretic control

Fig. 5 Dynamic response against load perturbation(R: 5 → 3 Ω)

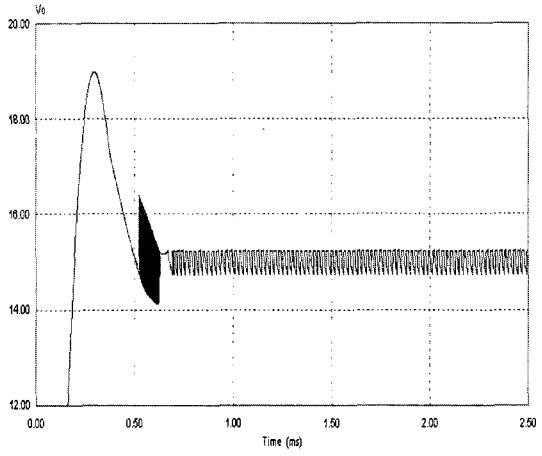


(a) Conventional hysteretic control

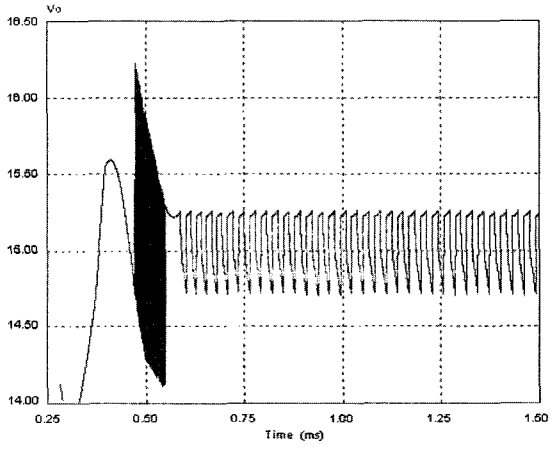


(b) Proposed two-loop hysteretic control

Fig. 6 Dynamic response against source perturbation (V_g: 20 → 24 V)



(a) Conventional hysteretic control



(b) Proposed two-loop hysteretic control

Fig. 7 Load voltage peak overshoot during starting

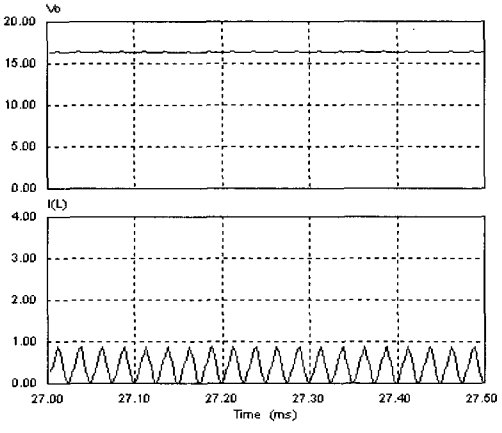


Fig. 8 Simulated steady-state v_o, i_L waveforms

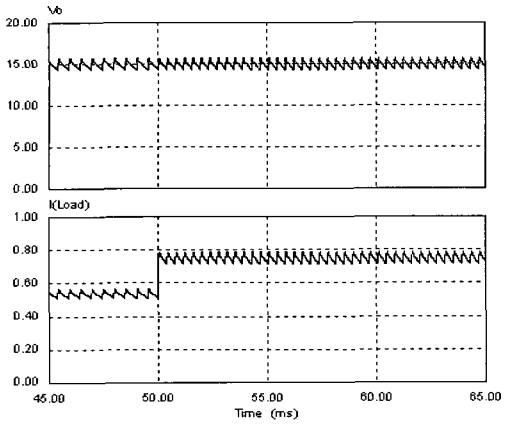


Fig. 9 Simulated dynamic response of load voltage against load disturbance (R: 28 → 20 Ω)

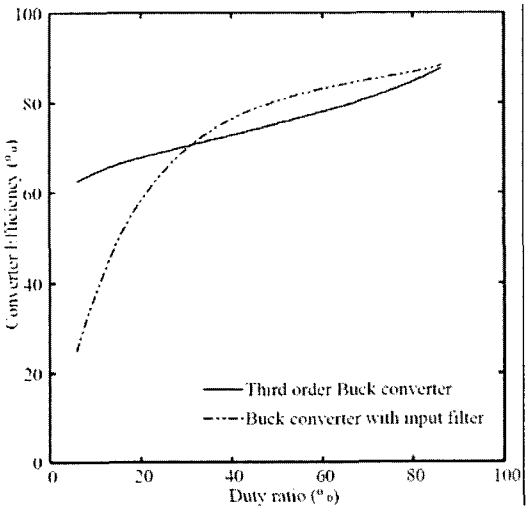


Fig. 10 Comparison of efficiency with duty ratio

The starting performance of these two control methods are compared in Fig. 7 and these observations indicates that the starting peak overshoot is less in the proposed control scheme. Simulated steady-state waveforms of load voltage and source current are shown in Fig. 8. It can be noted that the load voltage is almost constant and the source current is continuous. Simulated dynamic responses of the converter for load variation, R: 28 → 20 Ω, is plotted in Fig. 9. From the comparative simulation study, given in Table 2, it is seen that there are some major benefits gained after inclusion of an additional capacitor current loop as compared to the conventional voltage-mode hysteretic control summarized as:

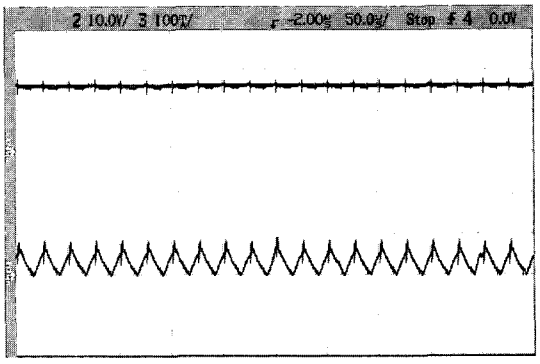


Fig. 11 Experimental steady-state v_o, i_L waveforms

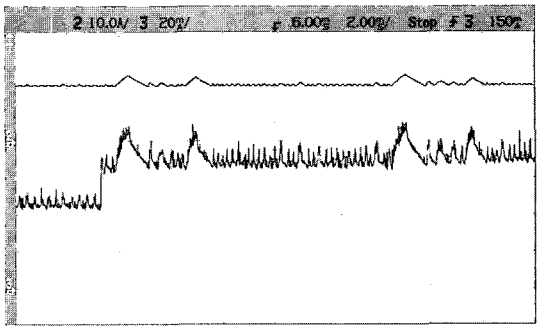


Fig. 12 Measured dynamic response of load voltage against load disturbance (R: 28 → 20 Ω)

Table 2 Comparison of dynamic response characteristics

	Conventional Hysteresis Control	Two-loop Hysteresis Control
Transient Settling Time	109 μs	83 μs
Change in Frequency	44 → 125 kHz	35→ 55.5 kHz
Starting peak overshoot	19 *V*	16.25 *V*

1. The transient settling time after the occurrence of load disturbance is considerably reduced i.e. there is improvement in the dynamic response of the converter.
2. Comparatively narrower switching frequency variation against disturbances, so that converter parameter design meets the steady-state requirements.
3. The starting peak overshoot is also reduced.

As compared to the BCIF there is only one additional component, 'D_2', used in the proposed converter. As a result the efficiency reduction of this TOBC may not be so much. However, for comparison purposes the measured efficiency of the BCIF and TOBC are plotted in Fig. 10. The proposed converter efficiency is higher or almost equal to the BCIF for the extreme duty ratios of operation. However, the measurements show that for a medium range of duty ratio's the efficiency reduction of TOBC is 5 %. These experimental observations show that just an increase in one additional diode may not penalize much from the efficiency reduction point of view.

In order to validate the simulation studies, experimental prototype was built and measurements of steady-state and dynamic responses were recorded, which are shown in Figs. 11 and 12, respectively. These results closely match the simulated results. Slight discrepancies in the simulation and experimental results are mainly due to: (i) parasitic voltage drops within the converter circuit, (ii) mismatch in the fine tuning of controller constants, K_1 and K_2, and (iii) accuracy of the sensing, etc.

5. Conclusions

A two-loop hysteresis control was proposed for the TOBC. As the hysteresis controller contains two loops, one for current control and the other for voltage regulation, the converter performance is the same as with the conventional current-mode controller. In addition, this two-loop scheme results in robust control. Simulation results demonstrated the performance improvement of two-loop control over the single-loop hysteretic control in terms of starting peak, peak overshoot, and frequency variation.

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