논문 2007-44SD-10-3

PHS용 Automatic Tuning 방법을 이용한 Complex Filter

(A CMOS Complex Filter with a New Automatic Tuning Method for PHS Application)

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요 약

이 논문에서는 PHS용 new automatic tuning 방법을 가지는 baseband complex bandpass filter를 제안하였다. DC offset 문제를 해결하기 위한 Low_IF 구조로 CMOS로만 집적된 PHS용 수신기를 설계하였다. ACS 특성을 만족시키기 위해 3차 Chebyshev complex filter를 이용하여 baseband를 선택할 수 있는 filter를 설계하였다. 새롭게 제시한 Corner frequency tuning 방법은 공정의 변화에 보상을 해주는 방식이고, MOS 스위치에 의한 노이즈 레벨을 감소시킨다. 이 filter는 CMOS 0.35um 공정이며, 전력소모는 12mW였다.

Abstract

This paper presents a baseband complex bandpass filter for PHS applications with a new automatic tuning method. The full-CMOS PHS transceiver is implemented by adopting the Low-IF architecture to overcome the DCoffset problems. To meet the Adjacent Channel Selectivity (ACS) performance, the 3rd-order Chebyshev complex bandpass filter is designed as the baseband channel-select filter. The new corner frequency tuning method is proposed to compensate the process variation. This method can reduce the noise level due to MOS switches. The filter was fabricated using a 0.35μm CMOS process, and the power consumption is 12mW.

Keywords: PHS, complex filter, Low-IF, bandpass, corner frequency, tuning

I. 서 론

The personal handy-phone system (PHS), which was first commercially launched in Japan in 1995, has enjoyed a recent resurgence in China with over 50 million subscribers in 2004. Recently, to implement the fully integrated RF transceiver, the direct-conversion receiver architecture is widely used. But, DC-offset is the one of the most serious problem in the direct-conversion architecture. A key challenge in the design of the PHS system is that it has a very short guard time (~30s) between the active slots, in whichtime the DC-offset should be corrected. Therefore, there is not enough time for DC offset correction. So, the Low-IF architecture is adopted in this design. However, the Adjacent Channel Selectivity (ACS) specification is tighter in Low-IF architecture.

In this paper, the complex bandpass filter is proposed as an alternative of the lowpass filter. And a new cut-off frequency tuning method which can

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※ This work was sponsored by MIC/ IITA/ ETRI SoC Industry Promotion Center, Human Resource Development Project for IT SoC Architect.

※ This research is supported by the ubiquitous Computing and Network (UCN) Project, the Ministry of Information and Communication (MIC) 21st Century Frontier R&D Program in Korea.

접수일자: 2007년5월26일, 수정완료일: 2007년9월20일

reduce the number of switches in programmable capacitor arrays is proposed.

Ⅱ. 본 론

1. Complex Bandpass Filter Architecture

Fig. 1 shows the Adjacent Channel Interference (ACI) of the PHS system. The nearest interferer is located at 600kHz, and its magnitude is 50dB larger than the wanted signal. As shown in Fig. 1(a), if the direct conversion receiver architecture is used, the interferences are located at 600kHz, which can be attenuated by the lowpass filter. However, if the IF frequency is 150kHz, the interferences are shifted to -450kHz, +750kHz, respectively as shown in Fig. 1(b). Ifthe lowpass filter is used, the attenuation characteristic is tighter because the worst case interferer is seemed to be located at 450kHz. Therefore, the complex banpass filter whose center frequency is located at 150kHz is designed for the ACS performance.

Fig. 2(a) shows the designed 3rd-order Chebyshev complex bandpass filter. The wanted signal is composed of the in-phase signal and quadrature signal, which are separated by the 90 phase. Complex bandpass filter uses both signals to perform the complex operations. As shown in Fig. 2(a), the complex bandpass filter has the in-phase signal path and the quadrature-phase signal path. Internal nodes of each paths are inter-connected to other paths. Therefore, I/Q mismatches is one of the most critical design issues in the complex filter. In this design, because I/Q mismatch compensation scheme is applied, I/Q mismatch is drastically reduced.

Resistor arrays and capacitor arrays are shown in Figure 2(b). Resistor arrays are composed of resistors and switches. Resistor arrays control the center

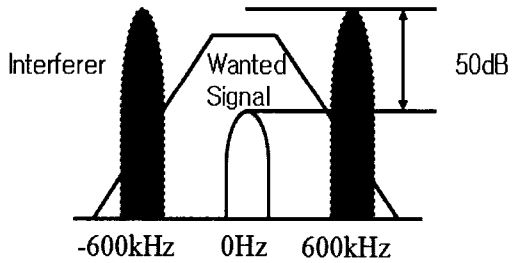

그림 1. (a) Direct Conversion에서 Low-pass Filtering
Fig. 1. (a) Low-Pass Filtering in Direct-Conversion Receiver.

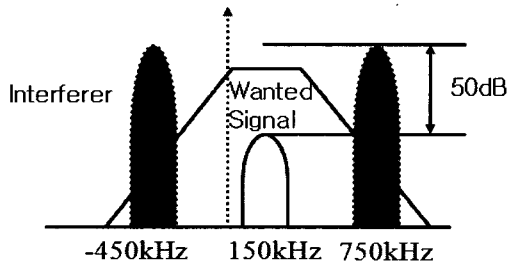

그림 1. (b) Low-IF 수신기에서 Complex bandpass Filtering
Fig. 1. (b) Complex bandpass Filtering in Low-IF Receiver.

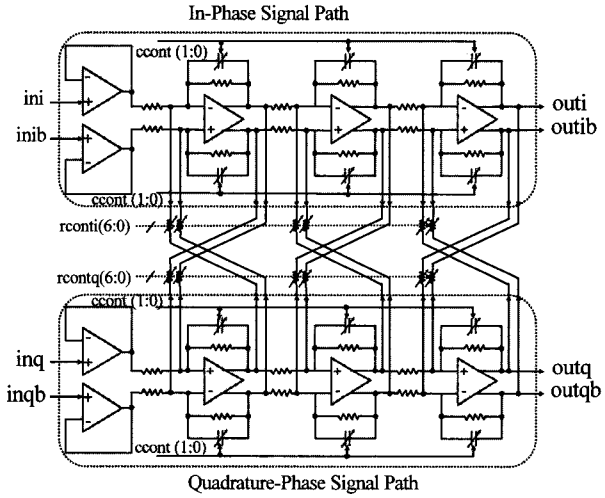

그림 2. (a) 회로도
Fig. 2. (a) Schematic.

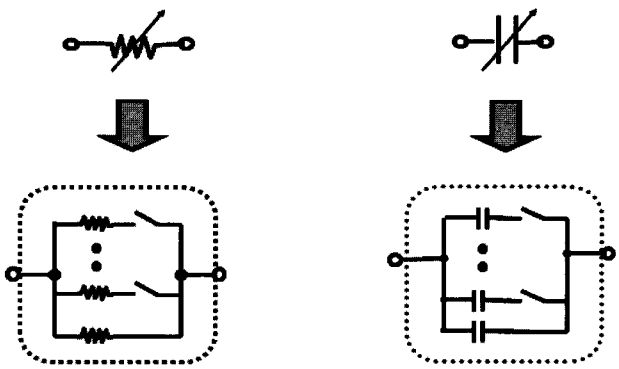

그림 2. (b) Complex filter에서 사용된 저항 배열과 cap 배열
Fig. 2. (b) resistor arrays and capacitor arrays of the complex bandpass filter.

frequency of the bandpass filter and its control signals, rconti(6:0), rcontq(6:0), are set through the serial interface and represented in thermometer code.

The corner frequency was made tunable by using programmable capacitor arrays. Capacitor arrays are composed of capacitors and switches. The tuning bits, ccont(1:0), are determined from the on-chip tuning block. There are trade-offs between resistor values and capacitor values. When resistor values are reduced to make thermal noise small, capacitor values become large. That leads to a large area. On the other hand, as capacitor values become smaller to reduce the area, the noise level rises. So, capacitor values and resistor values were optimized.

2. Proposed Filter Tuning

Resistors and capacitors are usually varied about 15% due to the process variation. In continuous time filters, this leads to a large variation of the corner frequency, which in most case, must be compensated by adjusting the component values. Conventional tuning circuit based on VCO is shown in Fig. 3(a). However, this tuning circuit is not suitable to tune an active-RC filter with programmable capacitor matrices. The output of the loop filter in the PLL is analog voltage, which can not be interfaced directly with the capacitor matrices.

The proposed two-step tuning scheme is shown in Fig. 3(b). The clock generator provides the clocks, clk0, clk1 to coarse and fine tuning controllers. Ctu is charged during clk0 is high, and VCOMP is sampled by clk1. Reference voltages for comparators, Vref, Refl, RefH, RefM are generated in the reference voltage generator block. The operation is as follows. Before main capacitor tuning steps, the reference tuning loop is enabled to compensate the resistor variation. Pbias is compared with Vref, and vres(2:0) is controlled according to the result. When pbias is larger than Vref, resistor load should be smaller, so vres(2:0) is increased. On the other hand, if pbias is smaller than Vref, resistor load should be larger, so vres(2:0) is decreased. Reference tuning is completed when pbias crosses the Vref.

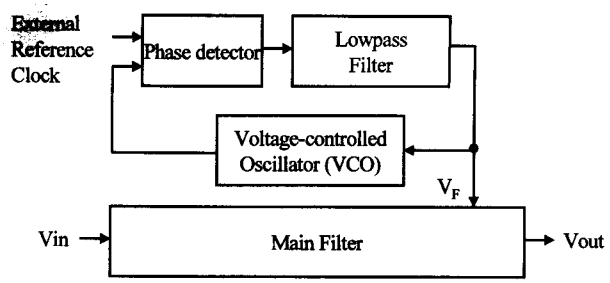

그림 3. (a) 기존의 튜닝 방법
Fig. 3. (a) Conventional tuning method.

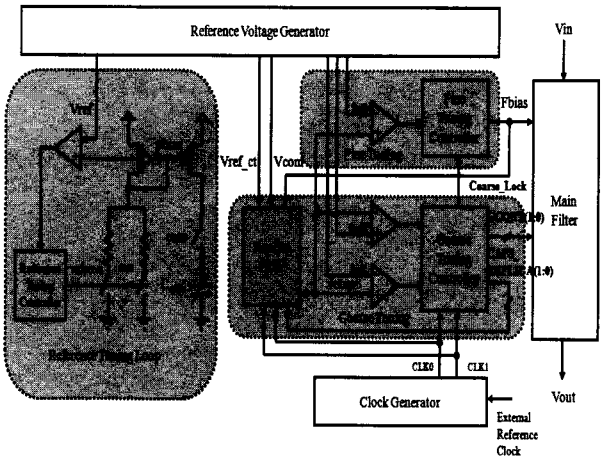

그림 3. (b) 제안된 2단계 튜닝 방법
Fig. 3. (b) proposed two-step tuning method.

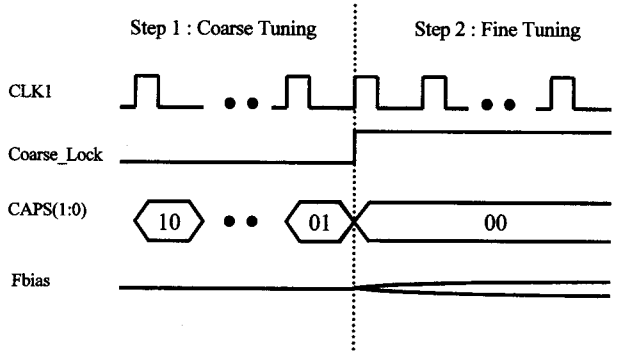

그림 4. 제안된 튜닝 방법에서의 타이밍 다이어그램
Fig. 4. Timing diagram of the proposed tuning method.

After reference tuning, main capacitor tuning is done in two-steps, that is, the coarse tuning and the fine tuning. Fig. 4 shows the timing diagram of the proposed two-step tuning method. Fig. 5 shows the block diagram and the timing diagram of the replica filter in the coarse tuning block. When VCOMP voltage is precharged when clk0 and clk1 are high. When clk0 goes from high to low, the VCOMP voltage is determined as Eq. 1.

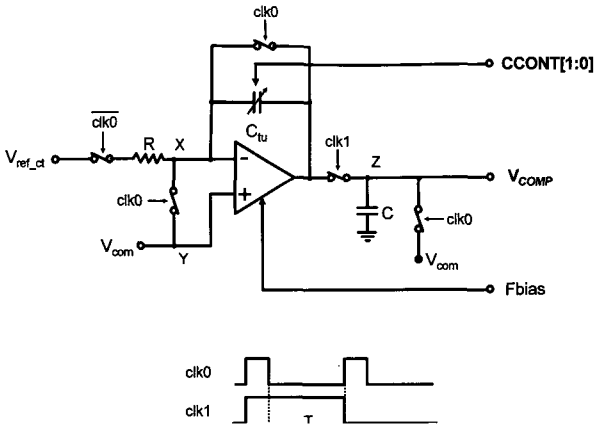

그림 5. Coarse 튜닝 블록에서 레플리카 필터의 블럭다이어그램과 타이밍 다이어그램

Fig. 5. Block diagram 와 timing diagram of the replica filter in coarse tuning block.

$$VCOMP = V_{com} - \frac{1}{RC_{tu}}(V_{ref\_ct} - V_{com})T \quad (1)$$

Fig. 5. (a) Block diagram (b) timing diagram of the replica filter in coarse tuning block.

First, CCONT(1:0) are tuned until VCOMP is located between pre-determined ranges. VCOMP is compared with refL and refH. When VCOMP is higher than refH, CCONT(1:0) are increased. Whereas, if VCOMP is lower than refL, CCONT(1:0) are decreased. When VCOMP is located between refL and refH, coarse_Lock signal goes from low to high. Usually, many tuning capacitance levels are required for fine resolution[3, 6]. But, only two bits are sufficient in this design with the two-step tuning method. After the coarse_lock signal is asserted, the corner frequency is tuned by the fine tuning control block.

Fbias controls the tail current of the op-amp[4~5]. Thus, the DC-gain of the op-amp is changed according to the Fbias voltage. If the DC-gain of the op-amp is infinite, the cut-off frequency does not change. However, because the DC-gain of the op-amp is finite, the cut-off frequency of the filter is changed as the DC-gain of the op-amp changes. Fbias is compared with refM. When VCOMP is larger than refM, Fbias should be increased. On the other hand, Fbias should be decreased when VCOMP is smaller than refM. The range of Fbias is 0.8V to 1.2V. The bandwidth of the op-amp is adjustable according to the mode to save the power. And the transistor sizes in the op-amp are designed to be very large to reduce the 1/f noise.

III. 실 험

The complex bandpass filter was fabricated using a 0.35m CMOS process. The chip area is 3.8mm2. The supply voltage is 3 V. Fig. 6 shows the microphotograph.

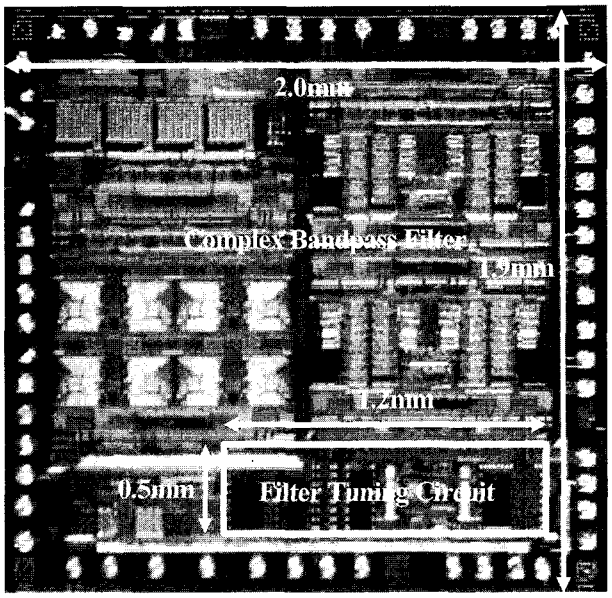

그림 6. Chip microphotograph

Fig. 6. Chip microphotograph.

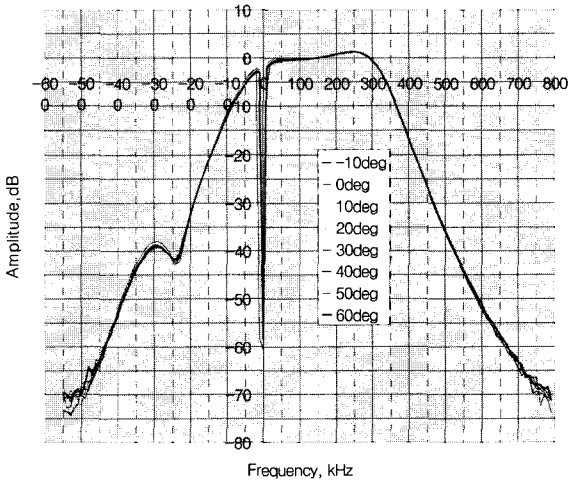

그림 7. Complex filter에서 측정한 Amplitude 응답

Fig. 7. Measured amplitude response of the complex bandpass filter.

표 1. 성능 요약
Table 1. Perfomance summary.

Technology	0.35 m CMOS
Chip area	3.8 mm^2
Supply voltage	3 V
Tuning range	100 kHz
Power (mW)	13
IIP3 (dBm)	25
Noise (nV / $\sqrt{Hz}$)	85
Passband ripple	0.8

Fig. 7 shows measured amplitude response of the complex baseband filter, when the temperature is changed from -10C to 60C. The cut-off frequency is 150kHz 110kHz. The cut-off frequency is almost constant as the temperature is changed due to the proposed filter tuning method.

The power consumption is 13mW. The frequency tuning range is 100kHz, which is the 50% of the signal bandwidth. That is, the cut-off frequencycan be adjusted by 100kHz although it is shifted due to the temperature, the supply voltage, and the process variations.

Out-of-band IIP3 was determined by performing IM3 test. When two tones of -44 dBm at 600 kHz and 1.2 MHz are applied, IIP3 is +25 dBm.

Input-referred average passband noise densitie of the filter is 85nV / $\sqrt{Hz}$. The passband ripple is less than 0.8 dB, and the stopband rejection at -450kHz is 66 dB. Table 1 summarizes the performance of the filter.

IV. 결 론

The CMOS complex bandpass filter for PHS transceiver was presented. Capacitors and resistors arrays set the cut-off frequency and the center frequency, respectively. Proposed two-step tuning method can reduce the number of switches and thus, can reduce the noise and the area.

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