Advanced Hybrid EER Transmitter for WCDMA Application Using Efficiency Optimized Power Amplifier and Modified Bias Modulator

효율이 특화된 전력 증폭기와 개선된 바이어스 모듈레이터로 구성되는 진보된 WCDMA용 하이브리드 포락선 제거 및 복원 전력 송신기

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Abstract

We have proposed a new "hybrid" envelope elimination and restoration(EER) transmitter architecture using an efficiency optimized power amplifier(PA) and modified bias modulator. The efficiency of the PA at the average drain voltage is very important for the overall transmitter efficiency because the PA operates mostly at the average power region of the modulation signal. Accordingly, the efficiency of the PA has been optimized at the region. Besides, the bias modulator has been accompanied with the emitter follower for the minimization of memory effect. A saturation amplifier, class F^{-1} is built using a 5-W PEP LDMOSFET for forward-link single-carrier wideband code-division multiple-access(WCDMA) at 1-GHz. For the interlock experiment, the bias modulator has been built with the efficiency of 64.16 % and peak output voltage of 31.8 V. The transmitter with the proposed PA and bias modulator has been achieved an efficiency of 44.19 %, an improvement of 8.11 %. Besides, the output power is enhanced to 32.33 dBm due to the class F operation and the PAE is 38.28 % with ACLRs of −35.9 dBc at 5-MHz offset. These results show that the proposed architecture is a very good candidate for the linear and efficient high power transmitter.

요 약

본 논문에서는 효율 특성에서 특화된 전력 증폭기(PA)와 개선된 바이어스 모듈레이터를 이용하여 새로운 하이브리드 포락선 제거 및 복원(EER) 전력 송신기를 제안하였다. 전력 증폭기는 모듈레이션 신호의 평균 전력 영역에서 대부분 동작하기 때문에 평균 드레인 바이어스 전압에서 전력 증폭기의 효율은 전체 전력 송신기의 효율 특성에 매우 중요한 영향을 미친다. 따라서 전력 증폭기의 효율을 평균 드레인 바이어스 전압 영역에서 최적화하였다. 또한, 바이어스 모듈레이터는 메모리 영향을 최소화하기 위하여 에미터 팔로워(Emitter Follower)와 결합되도록 하였다. 포화 전력 증폭기인 역 Class F급 전력 증폭기가 1 GHz 대역 포워드 링크 싱글 캐리어를 가지는 WCDMA 신호에 대해서 최고 전력이 5 W인 LDMOSFET을 이용하여 설계되었다. 실험 결과, 바이어스 모듈레이터는 31.8 V의 최고 전력 크기를 가지면서 64.16 %의 효율을 유지하였다. 제안된 전력 증폭기와 바이어스 모듈레이터를 결합한 전력 송신기는 기존 방식으로 설계된 전력 증폭기와 결합하였을 경우보다 8.11 %나 개선된 44.19 %의 전체 효율 특성을 보였다. 게다가, F 급 동작을 보이면서 전체 출력 전력은 기존 방식의 전력

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증폭기를 결합한 경우보다 2.9 dB 개선된 32.33 dBm으로 개선되었고, PAE와 5 MHz 옵셋에서의 ACLR은 각각 38.28 %, −35.9 dBc를 기록하였다. 이와 같은 결과들은 고선형성과 함께 고효율 특성을 가지는 전력 송신기에 매우 적합한 구조가 될 수 있다는 것을 명확히 보여주고 있다.

Key words : WCDMA, EER, DPD, Transmitter, Saturation Amplifier, Envelope Signal

Ⅰ. Introduction

High efficiency with high linearity is essential for a low-cost wideband code-division multiple-access(WCDMA) transmitter. As a good candidate for the techniques, LINC, Δ-Σ modulation, Doherty, and EER/Polar modulator have been suggested. The first two techniques show a high linearity with a moderate efficiency and the latter two techniques show a high efficiency with a moderate linearity characteristic generally[1]. However, if the digital predistortion(DPD) technique is applied to the latter two techniques, the moderate linearity can be enhanced sufficiently for the base station application.

The traditional envelope elimination and restoration (EER) transmitter is based on the decomposition of the emitted signal in the envelope and phase parts to improve the overall efficiency. The Radio Frequency (RF) transistor is driven in switch or saturation mode with constant amplitude phase signal for a high efficiency. The amplified envelope signal through the efficient bias modulator is combined with the amplified phase signal at the drain of the RF transistor and we can obtain an amplified modulation signal at the output of the transmitter with a high efficiency[2]. To achieve a high linearity and PAE at the same time, we have selected the "hybrid" EER architecture shown in Fig. 1[2]. Because this architecture uses the modulation signal as an input signal of the PA instead of the phase modulated signal, the PA covers only the modulation signal bandwidth and the input power can be much lower. Therefore, a more reliable transmitter with high linearity and an improved PAE can be realized by the hybrid EER architecture.

The memory effects are defined as changes of the amplitude and phase in distortion components due to

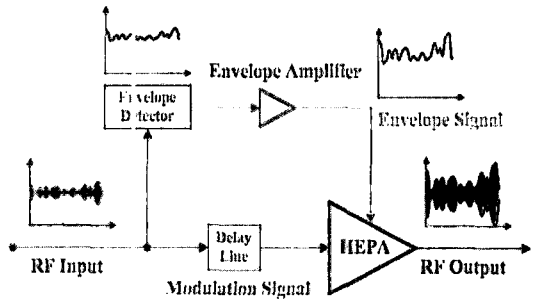


Fig. 1. Architecture of the hybrid EER transmitter with highly efficient bias modulator and power amplifier.

the previous signals and it generates serious nonlinearity of the Power Amplifier(PA)[3]. For the minimization of the effect, the tantalum capacitor is generally applied at the drain bias line of the PA but it makes distorted the envelope signal from the bias modulator for EER transmitter. Therefore, the memory effect is very important for the EER transmitter, and we have applied the emitter follower at the end of the bias modulator to short the second harmonics for the reduced memory effect.

For the highly efficient EER transmitter, the efficiency of the drain modulated PA is very important. The PA operates mostly at the average power region and the PAE of the PA should be optimized at the region[4]. However, the PA for a conventional transmitter has been designed to achieve peak efficiency at the peak drain voltage region generally and does not have a good efficiency at the average region. It causes a degradation of the overall efficiency of the EER transmitter. In this paper, we have verified the hybrid EER transmitter with the PA optimized at the average drain voltage region can deliver the improved performances.

Ⅱ. Bias Modulator for Hybrid EER Transmitter

The efficiency of the bias modulator is critical to the

hybrid EER transmitter, too. The overall efficiency can be defined as the product of bias modulator efficiency and the highly efficient PA(HEPA) drain efficiency, i.e:

$$\eta_{EER}=\frac{P_{OUT}}{P_{DC}}=\frac{P_{ENV}}{P_{DC}}\cdot\frac{P_{OUT}}{P_{ENV}}=\eta_{B.M.}\cdot\eta_{HEPA}$$

For an efficient operation, the bias modulator should cover the envelope signal bandwidth with a high efficiency. The envelope signal bandwidth of the WCDMA signal is above 5-MHz. Accordingly, we have been implemented the bias modulator composed of a parallel linear voltage source and a highly efficient switched current source. The linear voltage source has been utilized OP amplifier and Class AB amplifier and the switched current source has been used a buck dc-dc converter[2]. The proposed emitter follower has been added at the end of the bias modulator for the minimization of memory effect as shown in Fig. 2. The performances are illustrated in Table 1 and 2. Table 1 show the performance of the bias modulator without emitter follower versus different load impedance. Its peak output voltage is 31.8 V and a high efficiency of 67.73 % has been maintained constantly for the load impedances of the WCDMA envelope signal. The load impedances are evaluated at the drain bias line of the PA and change according to the drain bias, as illustrated in the next section. In the Table 2, the proposed bias modulator shows a little degradation about 3.57 %

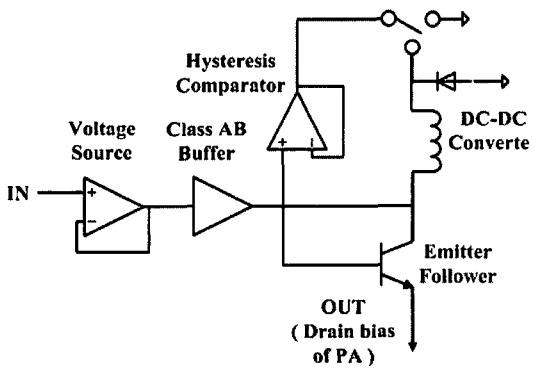


Fig. 2. Proposed bias modulator for hybrid EER transmitter.

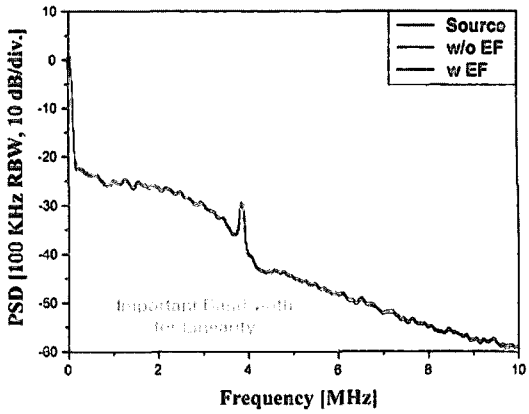


Fig. 3. The output spectra of the bias modulator for forward-link single carrier WCDMA envelope signal.

Table 1. The performance of the bias modulator with different load impedance.

R_{LOAD}	V_{PEAK}	P_{OUT}	P_{DC}	Eff.
77.6 Ω	31.8 V	1.588 W	2.345 W	67.73 %
49 Ω	31.8 V	2.514 W	3.712 W	67.73 %

Table 2. The performance of the bias modulator with /without emitter follower.

Condition	V_{PEAK}	P_{OUT}	P_{DC}	Eff.
w/o EF	31.8 V	2.099 W	3.099 W	67.73 %
w EF	31.8 V	2.037 W	3.174 W	64.16 %

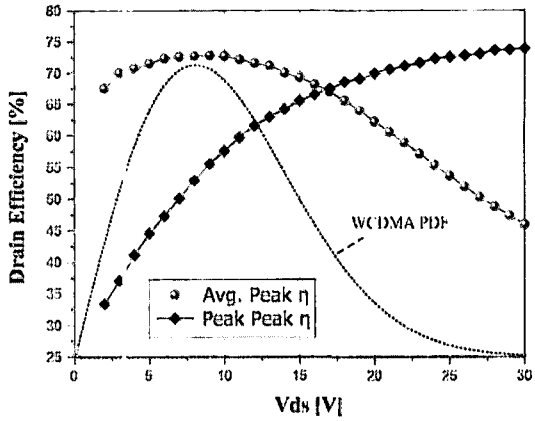
because of the V_{be} offset voltage drop at the output. Its peak output voltage is 31.8 V and a high efficiency of 64.16 % has been achieved at the WCDMA envelope signal. The linearity of the bias modulator can be checked from the output spectra as shown in Fig. 3. The implemented bias modulator has covered linearly more than 6 MHz bandwidth of the envelope signal. Therefore, it is verified that the bias modulator can be operated efficiently and linearly for the modulation signal.

Ⅲ. Highly Efficient Power Amplifier at the Average Region

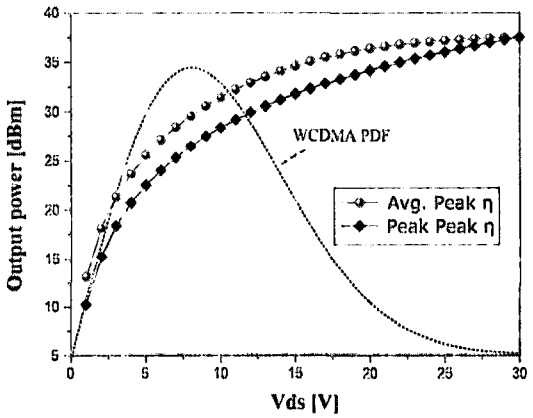
For a highly efficient EER transmitter, the class D,

E, F, or F^{-1} is generally used as a PA of the transmitter[1],[5]. The switching or saturation amplifier has a high efficiency at the peak power. When the V_{ds} is reduced for the EER operation, the efficiency is decreased because of the impedance mismatch due to the drain voltage dependent capacitive components of the LDMOSFET[6]. In the hybrid EER transmitter, the PA operates mostly at the average drain envelope voltage of the modulation signal, that is, at the peak p.d.f. point of the modulation envelope, as shown in Fig. 4. It reduces the overall EER transmitter efficiency for the modulation signal with a high peak to average ratio(PAR). Therefore, we have designed the bias modulation PA for the EER transmitter that is optimized to deliver the maximum efficiency at the average drain voltage region.

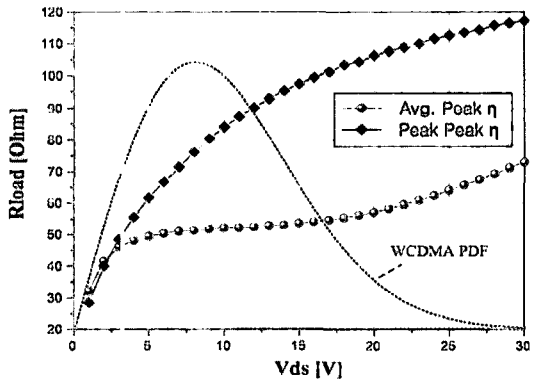
The highly efficient power amplifier has been realized as a class F^{-1} scheme at 1 GHz using 5-W PEP MRF281S LDMOSFET and the quiescent gate bias voltage is 2.2 V, class C bias for enhanced efficiency. The harmonic control circuit provides open impedance at the second harmonic and short impedance at the third harmonic. The output matching network has been designed considering the impedance mismatch by nonlinear capacitive components. For comparison, the two PAs have been designed to achieve the peak efficiency at the average region and the peak region, respectively. The drain efficiency performances are shown in Fig. 4(a). The PA optimized at the average region has been recorded the drain efficiency of 72.8 % and it is higher by about 17.3 % than that of the PA optimized at peak region. The high efficiency is maintained across the broad power range. Due to the better matching including the harmonic tuning, both the output power and efficiency are enhanced at the average region. The PA optimized at average region has about 2.9 dB more power than the other PA at the average V_{ds} as shown in Fig. 4(b), although the peak powers at the peak V_{ds} are similar. Therefore, our PA is slightly off-tuned for the optimum EER operation. The increased output for the average power tuning requires the high drain current and the bias modulator should supply more current to



(a) Measured drain efficiency versus V_{ds} of each PA



(b) Measured output power versus V_{ds} of each PA



(c) Load resistance of the bias modulator versus V_{ds} of each PA

Fig. 4. The characteristics of the highly efficient PAs for CW signal.

the PA drain. The load resistance(R_{load}) is the dc bias resistance given by V_{ds}/I_{ds} and the tendency is illustrated in Fig. 4(c). The load resistance of the average case is

decreased considerably because of the drain current and the resistance is maintained almost constant across bias range, indicating that it operates more linearly than the other case. As presented above section, the bias modulator has the high efficiency performance over broad output power range around the average power with the variation of the load. Therefore we have utilized the PA optimized at the average region as a HEPA of the hybrid EER transmitter.

Ⅳ. Interlock Experiment and Results

The hybrid EER transmitter has been evaluated at 1 GHz with single-carrier WCDMA signal of 3.84-MHz bandwidth and the PAR of 9.8 dB. For the interlock experiment, Agilent E4433B and E4438C have been used as master and slave units for the envelope signal and modulation signal generators, respectively. The measured results are shown in Table 3. The hybrid EER transmitter using the PA optimized at peak region has the output power of 29.42 dBm with the drain efficiency of 36.08 %. Due to the low gain characteristic of LDMOSFET, the PAE has been recorded a little low about 30.12 %.

On the other hand, the transmitter using the proposed PA and bias modulator has 2.9 dB more output power with the efficiency enhancement of 8.11 % and the overall PAE improved 8.16 %. The output spectra of the hybrid EER transmitter are presented in Fig. 5. The

Table 3. Summarized performance of the hybrid EER transmitter.

Max. Eff. region	Peak region	Avg. region	Avg. region (Added EF)
P_{OUT}	29.42 dBm	32.32 dBm	32.33 dBm
P_{DC}	2.425 W	3.763 W	3.852 W
Eff.	36.08 %	45.34 %	44.19 %
PAE	30.12 %	39.08 %	38.28 %
ACLR1 @ 5 MHz	−34 dBc	−35.9 dBc	−35.9 dBc
ACLR2 @ 10 MHz	−43.5 dBc	−44.8 dBc	−45.7 dBc

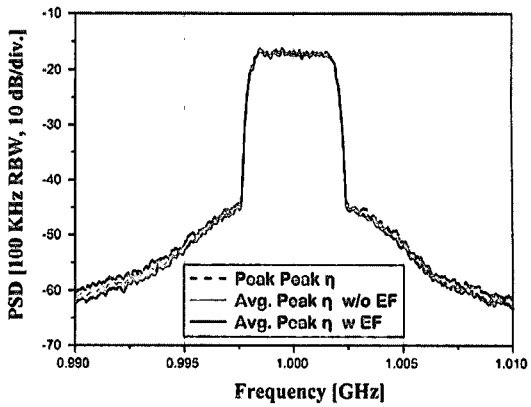


Fig. 5. Measured output spectra of the hybrid EER transmitter.

ACLRs of the average tuning are better than the other case as we have expected earlier. The ACLRs are −35.9 dBc and −44.8 dBc at 5-MHz and 10-MHz offsets, respectively. The ACLR at 10 MHz offset has increased a little by employing the emitter follower due to the small memory effect of low power LDMOSFET, but the proposed bias modulator is expected to deliver a huge improvement at high power EER transmitter in terms of linearity.

Ⅴ. Conclusions

In this paper, we have demonstrated the hybrid EER transmitter using the optimum PA architecture and bias modulator. For the experiment, the HEPA has been designed for a saturation amplifier, class F^{-1} using 5-W PEP LDMOSFET at 1- GHz and implemented with a proper matching network to deliver the maximum efficiency at an average drain voltage region for a single-carrier WCDMA modulation signal with a PAR of 9.8 dB. The characteristics of the amplifier are compared favorably over the conventional amplifier optimized at the maximum power. We have designed a highly efficient and linear bias modulator with emitter follower for the minimization of memory effect. In the interlock experiment, the hybrid EER transmitter consisted of the proposed PA and bias modulator has improved for the output power, drain efficiency, and li-

nearity by 2.9 dB, 8.11 %, and 1.9 dB at 5-MHz offset, respectively. Besides, the proposed bias modulator is expected to be a good alternative of memory effect minimization for high power EER transmitter. These improvements describe clearly the advantages of the new PA and bias modulator on the hybrid EER transmitter and show that the proposed architecture is very attractive to the efficient and linear high power transmitter system.

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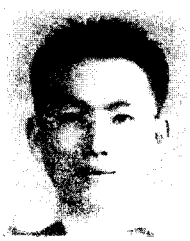

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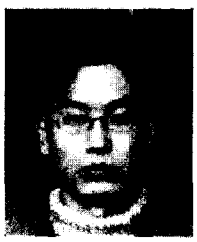

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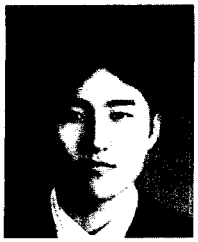

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