Electrical Properties of $F_{16}CuPc$ Single Layer FET and $F_{16}CuPc$/CuPc Double Layer FET

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We fabricated organic field-effect transistors (OFETs) based a fluorinated copper phthalocyanine ($F_{16}CuPc$) and copper phthalocyanine (CuPc) as an active layer. And we observed the surface morphology of the $F_{16}CuPc$ thin film. The $F_{16}CuPc$ thin film thickness was 40 nm, and the channel length was 50 μm, channel width was 3 mm. And we also fabricated the $F_{16}CuPc$/CuPc double layer FET and with different $F_{16}CuPc$ film thickness devices. We observed the typical current-voltage (I-V) characteristics and capacitance-voltage (C-V) in $F_{16}CuPc$ FET and we calculated the effective mobility. From the double layer FET devices, we observed the higher drain current more than single layer FET devices.

Keywords : Fluorinated copper phthalocyanine($F_{16}CuPc$), Organic field-effect transistor(OFET), Effective mobility, Current-voltage characteristics(I-V), Capacitance-voltage characteristics(C-V)

1. INTRODUCTION

Organic field effect transistors (OFETs) are very attractive for low-cost and low performance applications devices, such as Organic light-emitting diode (OLED) and integrated circuit for organic circuits[1]. It has been known phthalocyanine derivate materials with high thermal and chemical stability represent one of the most promoting candidates for modern optical electronic devices such as optical recording, gas sensors, thin film transistors and solar cells[2,3]. The $F_{16}CuPc$ material has a similar molecular shape and a similar crystal structure, with a hole mobility of about 0.04 cm^2/Vs. The highly ordered polycrystalline thin film of the $F_{16}CuPc$ can be deposited on amorphous SiO_2/Si substrates under similar optimized growth conditions. Figure 1 show the related energy levels of the highest occupied molecular orbital (HOMO) is 5.9 eV and the lowest occupied molecular orbital (LUMO) is 4.6 eV of the $F_{16}CuPc$ and the line was indicated the Fermi-level[2,5].

In this paper, we fabricated the single layer $F_{16}CuPc$ (40 nm) FET and $F_{16}CuPc$(10, 20 nm)/CuPc(20 nm) double layer FET devices. And we measured the drain current-drain voltage (I_D-V_D), capacitance-gate voltage (C-V_G) characteristics with various applied frequency and observed the AFM images of the $F_{16}CuPc$ thin film surface. The single and double layer FET device have the channel length and width was 50 μm and 3 mm, respectively. The I-V and C-V characteristics were carried out in an ambient condition by using a source-meter (Keithley type-2400) and LCR meter (Hioki type-3522-50)[4,6,7].

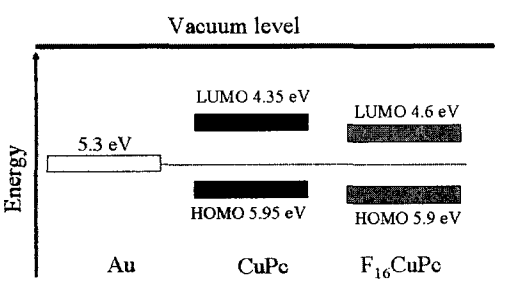
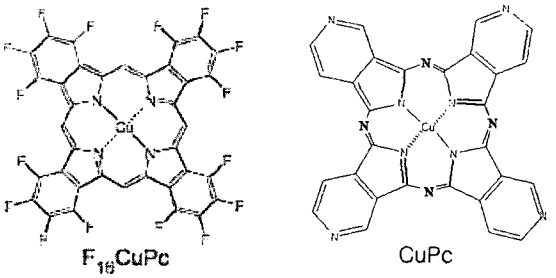
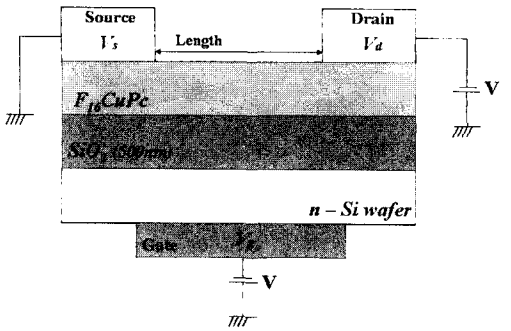


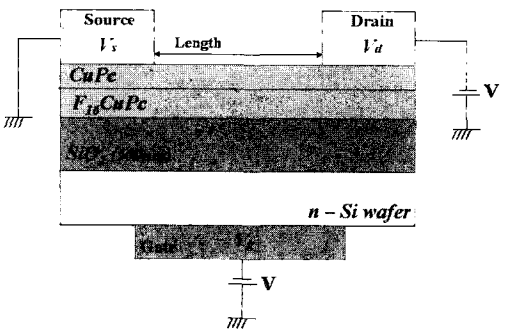
Fig. 1. Energy levels of $F_{16}CuPC$ and CuPc and work function of Au.



(a) Molecular structure

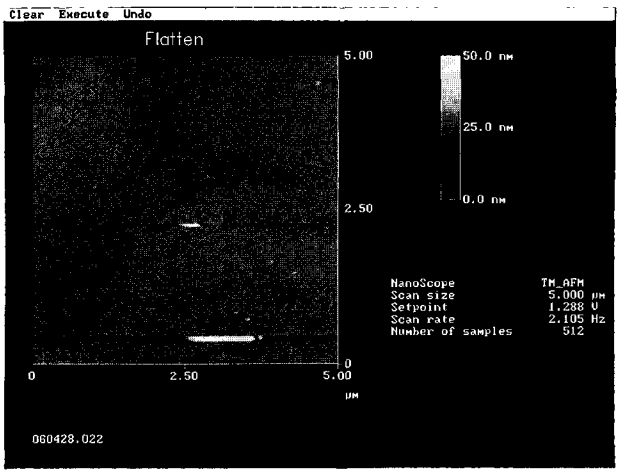


(b) Device structure (single layer)

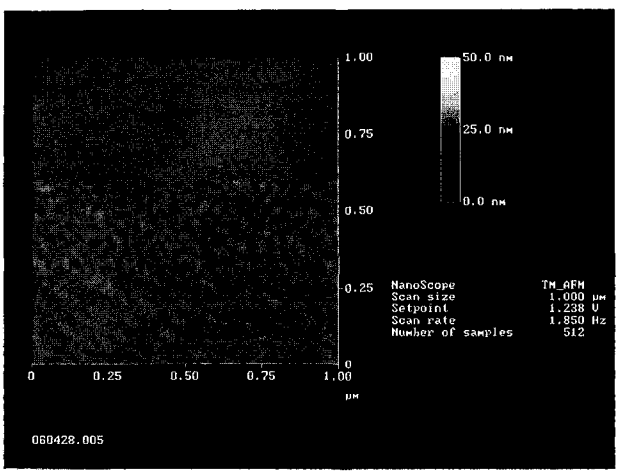


(c) Device structure (double layer)

Fig. 2. Device and molecular structures of the $F_{16}CuPc$ FET and $F_{16}CuPc/CuPc$ FET devices.



(a) $F_{16}CuPc$ surface morphology (5×5 μm^2)



(b) $F_{16}CuPc$ surface morphology (1×1 μm^2)

Fig. 3. AFM images of the bulk $F_{16}CuPc$ thin film surface at 40 nm.

2. EXPERIMENTALS

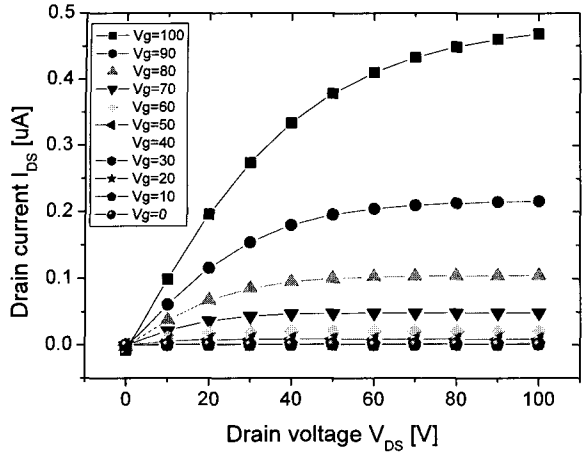
Figure 2 shows a molecular structure and the device structure of the single layer $F_{16}CuPc$ FET (Fig. 2(b)) and double layer $F_{16}CuPc/CuPc$ FET (Fig. 2(c)). The $F_{16}CuPc$ FET was fabricated using the silicon substrate and the UV/ozone treatment for 30 min with oxygen gas before deposition of the active materials. The $F_{16}CuPc$ and CuPc were deposited on to the substrate by thermal evaporation method with a deposition rate of 0.5 Å/s in 10^{-7} torr. The channel length (L) and width (W) were 50 μm and 3 mm, respectively.

3. RESULTS AND DISCUSSION

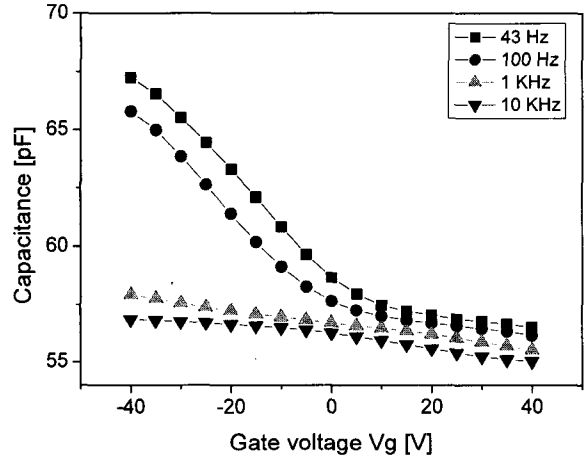
Figure 3 shows the AFM images of the bulk $F_{16}CuPc$ thin film surface at room temperature and the $F_{16}CuPc$ thin film thickness was 40 nm. From the large area (Fig. 3(a)) AFM images we could observe the very smoothly surface characteristics of the $F_{16}CuPc$ organic thin film. Also we could guess that the $F_{16}CuPc$ materials were layered to parallel with the substrate from the small area (Fig. 3(b)) AFM image.

Figure 4 shows the I-V and C-V characteristics of the $F_{16}CuPc$ single FET. The Fig. 4(a) shows the typical FET characteristics as the n-type characteristics and we were calculated the field-effect mobility of 1.5×10^{-4} cm^2/Vs.

Also we measured the C-V characteristics of the $F_{16}CuPc$ FET with various applied frequency in Fig. 4(b). We applied the varying frequency 43, 100, 1 K, and 10 K [Hz] to the $F_{16}CuPc$ FET for the capacitance measurement. The applied gate voltage was increase the

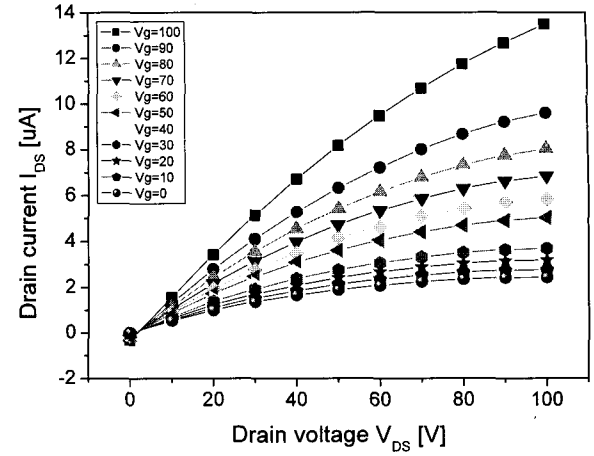


(a) Typical I-V characteristics (n-type)

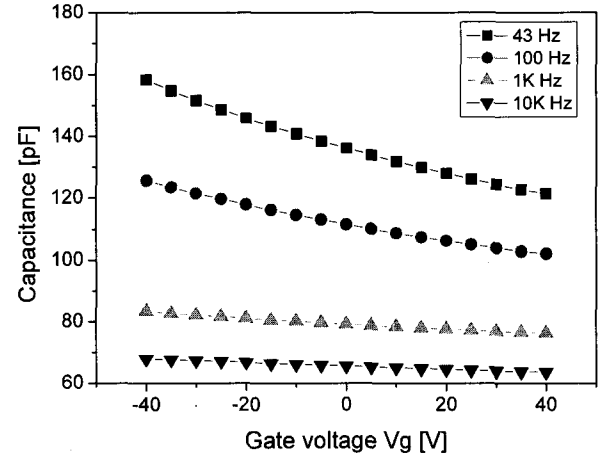


(b) C-V characteristics with various applied frequency

Fig. 4. I-V and C-V characteristics of the F_{16}CuPc single layer FET.



(a) I-V characteristics



(b) C-V characteristics

Fig. 5. I-V and C-V characteristics of the F_{16}CuPc(10 nm)/CuPc(20 nm) double layer FET.

capacitance was also increased in the between dielectric layer and F_{16}CuPc layer in range of the 40 V to –40 V. The capacitance measurement can be used to evaluate the interface-trapped charge between semiconductor and insulator materials. In high frequencies, interface traps cannot flow the ac applied voltage swing, so the capacitance could be observed clearly[8].

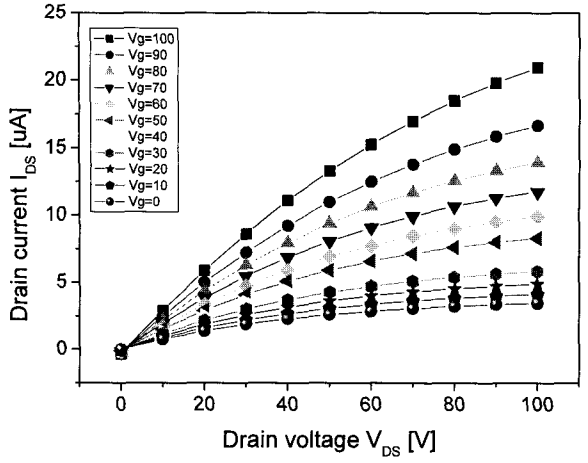
Figure 5 and 6 show the I-V and C-V characteristics of the F_{16}CuPc(10, 20 nm)/CuPc(20 nm) double layer FET. The Fig. 5, 6(a) shows the typical FET characteristics as the n-type characteristics and we could observe the higher drain current more than single F_{16}CuPc FET. We could consider that the increase in drain current of the double layer FET device was due to charge carriers in CuPc and F_{16}CuPc material.

Also, in double layer FET device, we could obtain the higher mobility more than single F_{16}CuPc FET device. We were calculated the field-effect mobility of the two type double layer FET about 5.5×10^{-3} cm^2/Vs and 1.5×10^{-3} cm^2/Vs, respectively. We also we measured the C-V characteristics of the F_{16}CuPc/CuPc double layer FET in Fig. 5(b), 6(b).

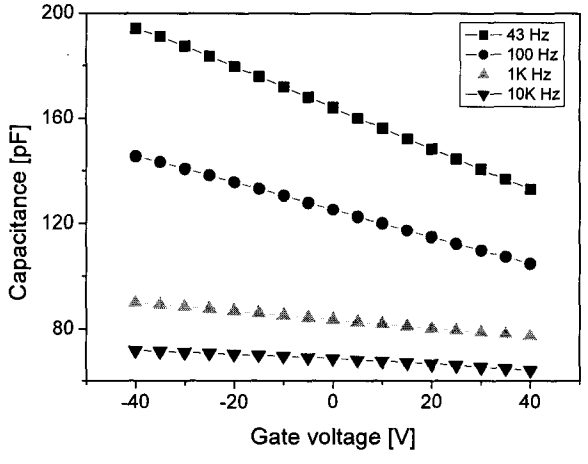
From the Fig. 5(b), 6(b), we could not observe the clearly C-V characteristics, because the interface of between F_{16}CuPc and CuPc were not clearly separated two layers in FET device. But the capacitance was not so small at organic/organic interface from the applied gate voltage. That means that the F_{16}CuPc and CuPc layer were effect to C-V characteristics at the organic/organic interface.

4. CONCLUSION

We fabricated the top-contact F_{16}CuPc single FET and F_{16}CuPc (10, 20 nm)/CuPc (20 nm) double layer FET. We



(a) I-V characteristics



(b) C-V characteristics

Fig. 6. I-V and C-V characteristics of the $F_{16}CuPc$(20 nm)/CuPc(20 nm) double layer FET.

observed the more than higher drain current and more higher effective mobility from the double layer FET devices.

Also, we were measured the C-V characteristics of the $F_{16}CuPc$ single FET and $F_{16}CuPc/CuPc$ double layer FET. From the result, we could not observe the clearly C-V characteristics, because the reason is the interface of between $F_{16}CuPc$ and CuPc not clearly separated two layers in FET device.

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