Research on the WIP-based Dispatching Rules for Photolithography Area in Wafer Fabrication Industries

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Abstract

Constructing an effective production control policy is the most important issue in wafer fabrication factories. Most of researches focus on the input regulations of wafer fabrication. Although many of these policies have been proven to be effective for wafer fabrication manufacturing, in practical, there is a need to help operators decide which lots should be pulled in the right time and to develop a systematic way to alleviate the long queues at the bottleneck workstation. The purpose of this study is to construct a photolithography workstation dispatching rule (PADR). This dispatching rule considers several characteristics of wafer fabrication and influential factors. Then utilize the weights and threshold values to design a hierarchical priority rule. A simulation model is also constructed to demonstrate the effect of the PADR dispatching rule. The PADR performs better in throughput, yield rate, and mean cycle time than FIFO (First-In-First-Out) and SPT (Shortest Process Time).

Key Words: Wafer Fabrication, Photolithography, Dispatching Rule

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1. Introduction

Wafer fabrication is a process oriented, capital intensive manufacturing. There are lots of characteristics that are different from traditional industries, e.g. long cycle time, reentrant process flow, lot splitting process, batching process, limited queuing time, unpredictable yield rate and machine breakdown etc., which make the production control tasks more complicated. Therefore, how to develop an effective production control policy is the most important issue in wafer fabrication factories. Dispatching rules and input regulation strategies form a class of methods in production planning and control (Uzsoy *et al.*, 1994). A number of researches have been directed towards dispatching and input policy problem in the wafer industries (Glassey *et al.*, 1988a, 1988b; Wein, 1988; Miller, 1990; Uzsoy *et al.*, 1994; Tsai *et al.*, 2003). Some past studies indicated that simple dispatching rules have little impact on the cycle time and throughput improvement as compared to the policy of wafer start (Glassey *et al.*, 1988a/1988b; Wein, 1988; Miller, 1990; Tsai *et al.*, 2003). However, the most common approach to shop-floor control problems is the utilization of dispatching rules (Uzsoy *et al.*, 1994).

Nevertheless, one can not expect using extremely simple dispatching rules to perform well on extremely complex systems. There are rarely dispatching rules considering the characteristics of operational processes and workstations. There are also practical needs to designate different priorities to wafer lots for dispatching problems, such as assisting operators to decide which lots should be pulled in the right time as well as developing a systematic way to alleviate the long queues at the Photostepper in order to smooth the sporadic workflow to the other areas (Johri, 1994). The need for developing dispatching rules arises from the fact that no dispatching rule has been approved to be optimal for job shop environment (Blackstone, 1990). The priorities must reflect the characteristics in production operations, such as the queue-time-limitation, resource conditions etc. Therefore, utilizing a comprehensive dispatching rule is necessary. This rule must consider specific industrial characteristics to facilitate effectiveness of wafer releasing policies. In most cases of wafer fabrication, the photolithography area is defined as the bottleneck. Therefore, a WIP-based dispatching rule for photolithography area is developed to enhance the performance of wafer fabrication factories.

2. Input Control Policies and Dispatching Rules

Input regulation strategies and dispatching rules form a class of methods widely used in practice (Uzsoy *et al.*, 1994; Tsai *et al.*, 1997; Tsai & Li, 2000). In wafer fabrication, studies addressing the production activity control issue have concentrated on wafer release and dispatching policies (Glassey *et al.*, 1988a/1988b; Wein, 1988; Johri, 1989; Lou *et al.*, 1989;

Tsai *et al.*, 2003). Many practitioners in wafer fabrication adopted a standard WIP as a decision variable to release or dispatch wafer lots (Glassey *et al.*, 1988a, 1988b; Johri, 1989; Lou *et al.*, 1989). However, determining a standard WIP level and designing a corresponding WIP-based dispatching rule in wafer fabrication are difficult tasks. Due to the complexity nature of scheduling problems in the wafer industries, the most common approach is the input control policies (Glassey *et al.*, 1988a/1988b; Wein, 1988; Miller, 1990). However, the most common method for shop-floor control problems, in practice, is applying dispatching rules. Uzsoy *et al.* (1994) indicated that there are strong interaction between the input regulations and sequencing of jobs on the shop floor. A dispatching decision is needed when different products and process steps are in a queue in front of the same workstation.

In recent years, many dispatching rules have been developed specifically for wafer fabrication. Glassey and Resende (1988a, 1988b), Lozinski and Glassey (1988), and Lou and Kager (1989) proposed several simple dispatching rules to correspond to specific releasing policies. Atherton and Dayhoff (1986a, 1986b) explored the dispatching scheme in masking area. They emphasized on dispatch schemes to assign priorities among process steps that are competing for the same workstation. They concluded that the later-steps-first-dispatched system attains higher throughputs with a reasonable level of inventory and relatively fast cycle time. It is the first paper of scheduling strategies for manufacturing systems that have a specific organization of semiconductor processing. However, it lacks of key parameters considered in dispatching schemes. Wein *et al.* (1992) regulated the inputs and dispatched the jobs while maintaining a set of throughput levels and then set due dates for jobs. Their scheme performed better than the combinations of due date setting, job releasing, and dispatching. Lozinski *et al.* (1988) and Glassey *et al.* (1988a, 1988b) developed bottleneck starvation indicators to aid in shop floor control. They defined virtual inventory, i.e. the expected time for the bottleneck to process all wafers, for the factory to prevent bottlenecks from starvation and to trigger wafer released into the fab. However, how the control mechanism to be applied is left to the shop operators. Pravin (1989) calculated the lots' slack time, the maximum waiting time of idle avoidance for critical workstations. Higher priority is set to the lot that has the smaller slack. Glassey *et al.* (1991), Fowler *et al.* (1992), and Weng *et al.* (1993) considered the batching effect in their dispatching rules. However, few of them are designed for photolithography area.

According to the requirements of several real wafer fabs, a feasible dispatching rule must consider process reentrance, bottleneck utilization, WIP level control, queue time limitation, rush orders, output balance, machine breakdown, machine maintenance, and specific characteristics of machine etc. However, it's impossible to design a rule that is embedded all of the above characteristics, especially when some of them are conflict inherently. In this paper, therefore, a parameterized WIP-based dispatching rule is designed for the bottleneck work-

station in a wafer factory. This dispatching rule treats all the characteristics as priority values. It's convenient to achieve a specific performance target by setting the weights of priority values.

3. The Construction of Dispatching Rule for Bottleneck Workstation

The wafer fabrication process is divided by photolithography workstation. The process flow started at photolithography workstation is referred as a loop (layer) and the photolithography workstation is treated as the starting point of material flow in each loop. That is, the entire wafer fabrication process is composed by a serial of loops. The number of loops that a product required depends on the number of times of visiting the photolithography workstation. The wafers flow through the photolithography workstation and enter the next process cycle until finish the entire process. Thus, the photolithography workstation can be viewed as a wafer distributed center. The dispatching decisions of photolithography workstation affect the loading balance of each area deeply. For photolithography area, several characteristics such as In-Line and Off-line Stepper, setup change, mask constraint, Preventive Maintenance (PM), output balance of each layer, and queue-time-limitation (waiting-time limitation) will be included in this dispatching rule. In this section, dispatching rules for photolithography, Furnace, and Implantation areas are developed.

3.1 Factors for Dispatching Rule

The aim of dispatching rule is to pick the "best" option without knowing which one of the options leading toward the better for the long-term performance measure. Hence, selection of a dispatching decision requires prediction of the system evolution (Johri, 1994). Nevertheless, predictions require knowledge of both the current system state, e.g. WIP levels, and characteristics of workstations, etc. Thus, properly looking ahead and considering the characteristics of wafer processing are needed in constructing a dispatching rule. The priority value is composed of an initial priority value and dynamic priority values. That is, when the wafer is released into Fab, an initial priority value, PO_i will be assigned according to the due date, order quantity, engineering needs, and hot lot etc. The dynamic priority values will be changed over time and updated through the manufacturing process according to the manufacturing steps, equipment types, and the status of Fab. In this paper, the dynamic priority values are determined respectively for the following characteristics:

3.1.1 *Queue-time-limitation*

If the lot's waiting time exceeds its allowable queue-time-limitation, the lot will be scrap-

ed or reworked which will have negative impacts on the yield and the cycle time. The notations and queue-time-limitation related to priority values are defined as follows:

T_n : The present.

T_{i0} : The completion time of lot i in the precedent operation step.

T_{ik} : The queue-time-limitation of lot i at workstation k.

F_{ik} : The maximum rework frequencies of lot i at workstation k.

Q_{ik} : The current rework frequencies of lot i at workstation k.

WQ_k : The weight for queue-time-limitation at workstation k.

PQ_{ik} : The priority value for queue-time-limitation of lot i at workstation k.

$$\text{The emergency degree of queue-time-limitation} = \frac{T_{ik}}{T_{i0}+T_{ik}-T_n} \tag{1}$$

$$\text{The weight for allowed remaining reworked times} = \frac{F_{ik}}{F_{ik}-Q_{ik}} \tag{2}$$

$$PQ_{ik} = \left(\frac{T_{ik}}{T_{i0}+T_{ik}-T_n}\right) \times \left(\frac{F_{ik}}{F_{ik}-Q_{ik}}\right) \times WQ_k \tag{3}$$

3.1.2 Rework lot

Yields and rework distributions are critical process parameters. The rework lot may cause from defects or lot's waiting time exceeds its queue-time-limitation. Too many numbers of times a lot been reworked will increase the cycle time. A higher priority value is, therefore, assigned to a rework lot than a normal lot. The notations and rework related to priority values are defined as follows,

R_i : The number of times lot i has been reworked.

WR_k: The weight of rework consideration assigned to workstation k.

PR_{ik}: The priority value for rework of lot i at workstation k.

$$PR_{ik} = R_i \times WR_k \tag{4}$$

3.1.3 Setup time

Setup dependence is a critical factor when making dispatching decisions. If the queuing lots, in front of a bottleneck workstation, have the same setup type as the preceding setup type of the workstation and its quantity is smaller than four lots (according to practical suggestion of shop floor dispatcher from a real world semiconductor Fab.), a higher priority value is assigned to these lots. The notations and setup related to a priority value are defined as follows,

WS_k: The weight of setup dependency for workstation k.

PS_{ik} : The lot i's priority value for same setup type at workstation k.

$$PS_{ik} = WS_k \tag{5}$$

3.1.4 The layer's WIP level

A higher priority value is assigned to the lot whose WIP level is lower than a standard WIP level. The relative priority value and notations are defined as follows,

N_k : The WIP level in front of workstation k.

RWL_{ij} : The actual WIP level of product i in its j th layer.

SWL_{ij} : The standard WIP level of product i in its j th layer.

W_{1ij} : The difference of actual and standard layer WIP level of product i in its j th layer.

$WD1_k$: The weight for difference between actual and standard layer's WIP level at workstation k.

$PW1_{ik}$: The priority value for difference between actual and standard layer's WIP level of product type i at workstation k.

The difference of layer's WIP level: $W_{1ij} = SWL_{ij} - RWL_{ij}$

The priority value of layer's WIP level difference: $$PW1_{ik} = \left(\frac{W_{1ij}}{\sum_{i=1}^{N_k} W_{1ij}}\right) \times WD1_k \tag{6}$$

3.1.5 WIP Levels of Sub-bottleneck Workstations

In practice, the wafer fabrication process is divided into several "routes" to facilitate production planning and control. Each route is composed of several steps. A sub-bottleneck workstation, relatively, is identified in each route. In order to avoid the WIP level of sub-bottleneck workstation in the next route to be excessive, the lot has a lower priority value when the WIP level of sub-bottleneck workstation in its corresponding next route is higher than its standard WIP level. The relative priority value and notations can be defined as:

RWM_{ib} : The actual WIP level of lot i in front of sub-bottleneck workstation b in its corresponding next route.

SWM_{ib} : The standard WIP level of lot i in front of sub-bottleneck workstation b in its next route.

W_{2ib} : The differences between actual and standard WIP level of sub-bottleneck workstation b, which located in the next process route of lot i.

$WD2_k$: The weight for difference between actual and standard WIP level in front of sub-bottleneck workstation k.

$PW2_{ik}$: The priority value of WIP level discrepancy of sub-bottleneck workstation k for lot i.

In which, $$W_{2ib} = SWM_{ib} - RWM_{ib} \tag{7}$$

$$\text{and } PW2_{ik} = \left(\frac{W_{2ib}}{\sum_{i=1}^{N_k} W_{2ib}}\right) \times WD2_k \tag{8}$$

In the PARDR rule, the WIP level is an important factor. Proper management of WIP levels is critical to the success of manufacturing operations (Lin and Lee, 2001). It can regulate the material flow, make full use of bottleneck capacity, and act as a valuable parameter for wafer release control. The standard WIP level of the entire factory (named *std_WIP*) is derived from Lin and Lee (2001). According to the total standard WIP level, the standard WIP level of product type i and the standard WIP level of product type i in its jth layer are derived as follows:

D_i = The fraction of product i processed through the factory;
CT_i = The cycle time of product i;
T_{ij} = The summation of processing time of product i in its jth layer.
SWP_i = The standard WIP level of product i;
SWL_{ij} = The standard WIP level of product type i in its jth layer;

The standard WIP level of product i: $SWP_i = std\_WIP \times \frac{D_i \times CT_i}{\sum_i (D_i \times CT_i)}$ (9)

The standard WIP level of product i in its jth layer: $SWL_{ij} = SWP_i \times \frac{T_{ij}}{CT_i}$ (10)

3.2 A Dispatching Rule for Photolithography Area

According to the priority values, defined in previous section, a photolithography area dispatching rule (PADR) is constructed based on the following procedures:

Step 1: Machine is available.
Step 2: Does the machine need to be maintained? In a simulation model, the PM is treated as a PM lot. That is, if there is a PM lot in the queue, then go to step 3, otherwise go to Step 4.
Step 3: Machine proceeds to maintenance. If PM is finished, go back to Step1.
Step 4: Select lots that match the operation condition from the queues in front of workstations.
Step 5: Select lots that have queue-time-limitation characteristic? If there are no such lots, then go to Step 7.
Step 6: Calculating the queue-time-limit priority value for all lots.
Step 7: Select lots that are in the status of rework. If there are no such lots, then go to Step 9.

Step 8: Calculate the rework priority value.
$PR_{ik} = R_i \times WR_k$

Step 9: Collect lots that have the same setup type with current running lot. If there is no such lot, go to Step 12.

Step 10: If the number of collected lot is less than four lots, go to step 11, otherwise go to Step 12.

Step 11: Set the setup priority value be $PS_{ik} = WS_k$ for all lots collected in Step 10.

Step 12: Calculate the priority value, $PW1_{ik}$.

Step 13: Calculate the priority value, $PW2_{ik}$.

Step 14: Determine the summarized priority value for each product type i at workstation k; $.P_{ik}$. In which, P_{0i} is the initial priority value of product i, the other priority values will change through manufacturing progress.

Step 15: Rank the P_{ik} and select the highest one.

Step 16: Process the selected lot.

3.3 Dispatching Rules for Non-bottleneck Workstations

Generally speaking, the Furnace areas and Implanter areas do not belong to bottleneck sections. Deploying suitable dispatching rule for their specific operation characteristics is required. For batch processing operations, such as Furnace, no matter how many lots are loaded at a time (the number of lots batched must be smaller than the maximal batch size), the processing time generally does not vary with the number of lots batched. Thus, the batching problem is to determine the number of lots loaded at a time to attain a better performance. Two batching rules are used in the simulation model: FIFO/B (First In First Out/Batch) and SPT/B (Shortest Processing Time/Batch). For Implanter machines, MI and HI implanter, there are two types of setup changes, dosage change and recipe change. In order to reduce the setup time, a lot is collected according to the same recipe type. In addition, to resolve the setup change issue, two-lot batch operation of MI implanter is also considered in the dispatching decisions. In this paper, SSU/B (Same SetUp/Batching) which embedded in Autosched (Burdett *et al.*, 1993) is applied in a simulation model.

4. Simulation Model

Simulation is the most common modeling technique in semiconductor manufacturing (Atherton and Dayhoff, 1986a, 1986b; Burman *et al.*, 1986; Miller, 1990; Glassey *et al.*, 1988a, 1988b; Wein, 1988). Therefore, a simulation model was adopted to analyze the effectiveness of the proposed dispatching rule. In this simulation model, wafer releasing strategies,

dispatching schemes, setup dependency, the schedules of prevention maintenance, and random machine breakdown, which all affect the manufacturing dynamics (Atherton and Dayhoff, 1986a, 1986b), are considered. There are several assumptions in this paper:

1. The move time between equipment is neglected.
2. A workstation includes several machines which have the same function.
3. A single lot contains twenty-five pieces of wafers.
4. Rework lots will only happen when the waiting time exceeds lots' queue-time-limitation.
6. The percentage of hot lot is 5% and appears randomly.
7. The bottleneck workstation is known and fixed during the planning horizon.
8. The queue-time-limitation is only happened in photolithography area.

In this section, a wafer fabrication factory of a global company, located in the Science Based Industrial Park in Taiwan, is analyzed. In this simulation model, five product types and 96 types of workstations, which totally contain 244 machines, are included. The frequencies of PM and machine breakdown are also considered in this model. Setup times are set for Stepper, MI and HI implanter. Input regulations and sequencing of jobs on the shop floor interact heavily (Uzsoy *et al.*, 1994). In this paper, the Uniform Loading (UL) and Fixed-WIP (FW) release policies are adopted in this simulation model to evaluate the performance of PADR dispatching rule. The simulation model was constructed in Visual Fox Pro 3.0b and AutoSched V4.5. The raw processing cycle time is around seven days; therefore, the data are collected after warm-up length (three weeks) and total six months of periods were simulated. Common random number stream, one of the variance-reduction techniques (Law & Kelton, 1991), is used. To demonstrate the effectiveness of PADR, three scenarios of the dispatching rule combination are designed (as shown in Table 1).

Table 1. Combinations of dispatching rules used in different type of equipment

Equipment	Scenario 1	Scenario 2	Scenario 3
Photolithography Area	FIFO	SPT	PADR
Implanter	SSU/B(MI) SSU(HI)	SSU/B(MI) SSU(HI)	SSU/B(MI) SSU(HI)
Furnace	FIFO/B	SPT/B	FIFO/B
Others	FIFO	SPT	FIFO

5. Simulation Experiment

First, the simulation model is used to analyze the effectiveness of combinations of three dispatching rules, PADR, SPT, and FIFO, and two releasing policies, Uniform Loading (UL)

and Fixed-WIP (FW). Then different weights of combinations are used to test the effectiveness of priority values under the PADR dispatching rule.

5.1 Wafer Releasing/dispatching Rules Experiments

The simulation outputs of the throughputs and the yield rates are displayed in Table 2. It shows that the FW performs better than UL under different dispatching rules. That is, by keeping a suitable WIP level, it can reduce the cycle time and result in a higher throughput rate. The PADR generates a higher effective throughput rate than FIFO and SPT. To avoid lots to be scraped, a high priority value is set for the lots when the waiting time exceeds the queue time limitation. This results in a 100% yield rate and a higher throughput (as shown in Table 3). From Tables 4 and Tables 5, the PADR produces lower average cycle time, average waiting time, and standard deviation of cycle time than FIFO and SPT.

Table 2. Throughput (lot) and yield rate under releasing policies/Dispatching rules

Releasing policies	**UL**			**FW**		
Dispatching rules	SPT	FIFO	PADR	SPT	FIFO	PADR
product A	64	72	78	67	76	78
product B	57	54	51	51	50	51
product C	176	184	186	203	198	202
product D	72	72	72	62	66	66
product E	18	17	18	17	17	16
Total	387	399	405	400	407	413
Scrap	11	5	0	7	3	0
Yield rate	97.24%	98.76%	100%	98.28%	99.27%	100%

Table 3. The number of times lots' waiting time exceed queue time limit

Releasing policies	**UL**			**FW**		
Dispatching rules	SPT	FIFO	PADR	SPT	FIFO	PADR
exceed 1 time	125	85	41	21	9	3
exceed 2 times	47	24	1	15	6	0
exceed 3 times	20	10	0	11	3	0
scrape	11	5	0	7	3	0

Table 4. Average cycle time and average waiting time under UL releasing policy (minutes)

Dispatching rules	SPT		FIFO		PADR	
	average	Std	average	Std	average	Std
Cycle time of all lots	23,394	4,337.23	22,664	3,810.08	21,755	3,768.99
Cycle time of rework lots	24,283	4,310.01	23,059	4,048.55	21,836	3,667.49
Cycle time of hot lots	23,190	4,322.79	21,962	3,771.42	20,077	3,538.57
Waiting time of all lots	69.88	36.71	56.01	20.08	53.20	20.43
Waiting time of rework lots	73.45	31.03	54.69	19.46	53.33	19.70
Waiting time of hot lots	83.44	47.34	53.88	21.82	44.48	22.61

Table 5. Average cycle time and average waiting time under FW releasing policy (minutes)

Dispatching rules	SPT		FIFO		PADR	
	average	Std	average	Std	average	Std
Cycle time of all lots	22,474	3,926.79	21,954	3,598.09	20,942	3,674.08
Cycle time of rework lots	23,127	3,769.58	22,844	3,593.98	21,191	3,552.08
Cycle time of hot lots	22,635	3,920.01	21,579	3,628.87	19,919	3,428.96
Waiting time of all lots	65.93	32.02	53.56	19.57	49.18	17.25
Waiting time of rework lots	65.14	28.62	56.53	18.23	48.82	18.03
Waiting time of hot lots	81.82	42.89	53.41	24.17	41.47	23.58

5.2 Factor Level Experiment

Multiple factors experiment design is adopted to analyze the effects of different levels under specific factor. Two tails hypothesis test is used for mean values (null hypothesis H_0: $\mu_1 = \mu_2$, alternative hypothesis H_1: $\mu_1 \neq \mu_2$) under $\alpha = 0.05$. The weights combinations are listed in Table 6. The objectives of a detailed schedule are to meet the due dates, determine flow times, and keep the shop floor running smoothly. Therefore, reducing the variance of cycle time is a practical objective for designing a dispatching rule to meet the customer requested due date. The hypothesis test for cycle times under different initial priority values is shown in Table 7. When the initial priority value is increased to 200, there is significant difference in cycle time. That is, it can notably reduce the cycle time of hot lots.

By increasing the weights of queue-time-limitation, the cycle time of reworked lots can be reduced (Table 8). However, when a larger weight is adopted, the cycle times of rush orders will increase significantly. From previous discussions, wafer releasing policy affects the

performance of weights for different WIP levels. In the simulation, different combinations of releasing policies and weights of WIP levels are tested. The combinations of weights of WIP levels and the weights of layer WIP levels of sub-bottleneck workstations are set to be (0, 0), (100, 100), and (200, 200) (Table 9). It shows that the weight scenario (200, 200) gives a significant improvement in average cycle time of rush orders. And the other weight combinations almost result in the same performance.

Table 6. The Weights Combinations

Run	PO_i	WS_k	WQ_{ik}	WR_k	$WD1_k$	$WD2_k$
1	**40**	10	20	20	100	100
2	**0**	10	20	20	100	100
3	**80**	10	20	20	100	100
4	**200**	10	20	20	100	100
5	40	**0**	20	20	100	100
6	40	**40**	20	20	100	100
7	40	10	**0**	20	100	100
8	40	10	**120**	20	100	100
9	40	10	20	**0**	100	100
10	40	10	20	**60**	100	100
11	40	10	20	**100**	100	100
12	40	10	20	20	**0**	**0**
13	40	10	20	20	**200(UL)**	**200(UL)**
14	40	10	20	20	**200(FW)**	**200(FW)**

Table 7. Testing of cycle times for initial priority values

PO_i	All lots' average CT	Reworked lots' average CT	Hot lots' average CT
0-40	Z = 0.305 < 1.96	Z = -0.588 > -1.96	T = 1.508 > 0.20*
40-80	Z = 0.527 < 1.96	Z = 0.663 < 1.96	T = 0.151 < 0.20
40-200	Z = 0.353 < 1.96	Z = 0.490 < 1.96	T = 0.293 > 0.20*
0-200	Z = 0.651 < 1.96	Z = -0.094 > -1.96	T = 1.832 > 0.20*

*: means significant difference, T0.025, 40 = 0.20.

Table 8. Testing of cycle times for weights of queue-time-limitation

WQ_{ik}	All lots' average CT	Reworked lots' average CT	Hot lots' average CT
0-20	Z = -0.013 > -1.96	Z = 3.963 > 1.96*	T = -0.082 > -0.20
0-120	Z = 0.534 < 1.96	Z = 4.424 > 1.96*	T = -0.310 < -0.20*
20-120	Z = 0.538 < 1.96	Z = 0.423 < 1.96	T = -0.225 > -0.20

*: means significant difference, T0.025, 40 = 0.20.

Table 9. Testing of cycle times for the weights of WIP level under UL releasing policy

$WD1_k$, $WD2_k$	All lots' average CT	Reworked lots' average CT	Hot lots' average CT
(0,0)-(100,100)	Z = 0.540 < 1.96	Z = 0.113 < 1.96	T = 0.187 < 0.20
(0,0)-(200,200)	Z = 0.997 < 1.96	Z = 0.302 < 1.96	T = 0.308 > 0.20*
(100,100)-(200,200)	Z = 0.457 < 1.96	Z = 0.194 < 1.96	T = -0.112 < 0.20

*: means significant difference, T0.025, 40 = 0.20.

According to the analysis, some conclusions can be drawn for the factors that used in PADR:

1. The adaptation of weight values for different factors influences the corresponding performance measurement indicator.
2. Weight values can improve the performance of selected measurement.
3. A higher weight value probably results in negative impacts on other factors. Therefore, the determination of weight values is a trade-off issue when apply the PADR rule.
4. The performance of PADR dispatching rule can be significantly enhanced while wafer releasing policy is applied.

6. Conclusions

In this paper, a dispatching rule (PADR) is designed for photolithography area in wafer fabrication factories. A simulation model is also constructed to demonstrate the effect of the PADR dispatching rule. Some conclusions are made in this paper:

1. The PADR performs better in the throughput, the yield rate, and the mean cycle time than FIFO and SPT. Therefore, considering all affecting factors and utilizing weights and threshold values to design a hierarchical priority rule is an effective approach.
2. The UL produces too much WIP stock which compensates the effect of the dispatching rule. On the other hand, the FW always keeps constant WIP in a system and results in a smoothing flow. The performance of dispatching rules under FW policy is better than the one under UL policy. Therefore, an adequate WIP level kept in system is important, which can promote system performance, especially when FW works with a good dispatching rule.

According to Section 5, system performance is affected by different factors which considered in PADR. Although the combinations of weight values perform well, it still needs to adjust the combinations according to different product mixture and equipment status, etc. Through the use of simulations, the factor's interactions can be analyzed conveniently and a better weight value combination can also be conducted. In addition, it is critical to carefully

design the weight values for different factors in order to reach the desired performance target.

References

1. Atherton, R. W. and Dayhoff, J. E.(1986a), Signatures Analysis: Simulation of Inventory, Cycle Time, and Throughput Trade-Offs in Wafer Fabrication. IEEE Transactions on Components, Hybrids, and *Manufacturing Technology*, Vol. 9, No. 4, pp. 498-507.
2. Atherton, R. W. and Dayhoff, J. E.(1986b), Signatures Analysis of dispatch Schemes in Wafer Fabrication. IEEE Transactions on Components, Hybrids, and *Manufacturing Technology*, Vol. 9, No. 4, pp. 518-525.
3. Blackstone, J. H.(1990), Capacity Management. South-Western Publishing Co.
4. Burdett, D. and Thompson, M.(1993), AutoSched and The Simulator System User's Manual. AutoSimulations Inc.
5. Burman, D. Y., Gurrola-Gal, F. J., Nozari, A., Sathaye, S. and Sitarik, J. P.(1986), Performance Analysis Techniques for IC Manufacturing Lines. *AT&T Bell Labs Technical Journal*, Vol. 65, No. 4, pp. 46-57.
6. Fowler, J. W., Phillips, D. T. and Hogg, G. L.(1992), Real-Time Control of Multi-product Bulk-Service Semiconductor Manufacturing Processes. *IEEE Transactions on Semiconductor Manufacturing*, Vol. 5, No. 2, pp. 158-163.
7. Glassey, C. R. and Resende, M. G. C.(1988a), Closed-Loop Job Release Control for VLSI Circuit Manufacturing. *IEEE Transactions on Semiconductor Manufacturing*, Vol. 1, No. 1, pp. 36-46.
8. Glassey, C. R. and Resende, M. G. C.(1988b), A Scheduling Rule for Job Release in Semiconductor Fabrication. Operation Research Letters, Vol. 7, No. 5, pp. 213-217.
9. Glassey, C. R. and Weng, W. W.(1991), Dynamic Batching Heuristic for Simultaneous Processing. *IEEE Transactions on Semiconductor Manufacturing*, Vol. 4, No. 2, pp. 77-82.
10. Johri, P. K.(1989), Dispatching in an Integrated Circuit Wafer Fabrication Line. Proceedings of the 1989 Winter Simulation Conference, pp. 918-921.
11. Johri, P. K.(1994), Practical Issues in Scheduling and Dispatching in Semi-conductor Wafer Fabrication. *Journal of Manufacturing Systems*, Vol. 12, No. 6, pp. 471-185.
12. Lin, Y. H. and Lee, C. E.(2001), The Total Standard WIP Estimation Method for Wafer Fabrication. *European Journal of Operational Research*, Vol. 9, No. 3, pp. 78-94.
13. Law, A. M. and Kelton, W. D.(1991), Simulation modeling & analyze. Singapore: McGraw-Hill Ltd.
14. Lou, S. and Kager, P. W.(1989), A Robust Production Control Policy for VLSI Wafer

Fabrication. *IEEE Transactions on Semiconductor Manufacturing*, Vol. 2, No. 4, pp. 159-164.

15. Lozinski C. and Glassey, C. R.(1988), Bottleneck Starvation Indicators for Shop Floor Control. *IEEE Transactions on Semiconductor Manufacturing*, Vol. 1, No. 4, pp. 147-153.
16. Tsai, C. H., G. T. Chang and R. K. Li.(1997), Integrating Order Release Control With Due-Date Assignment Rules. *International Journal of Production Research*, Vol. 35, No. 12, pp. 3379-3392.
17. Tsai, C. H. and R. K. Li.(2000), A Due-Date Oriented Scheduling Heuristic for Job Shop Cellular Manufacturing System. *International Journal of Industrial Engineering-Theory*, Applications, and Practice, Vol. 7, No. 1, pp. 76-88.
18. Tsai, C. H., Y. M. Feng and R. K. Li.(2003), A Hybrid Dispatching Rules in Wafer Fabrication Factories. *International Journal of the Computer, the Internet and Management*, Vol. 11, No. 1, pp. 64-72.
19. Uzsoy, R., Lee, C. Y. and Louis, A.(1994), A Review of Production and Scheduling Models in the Semiconductor Industry Part II: Shop-Floor Control. *IIE Transactions*, Vol. 26, No. 5, pp. 44-55.
20. Wein, L. M.(1988), Scheduling Semiconductor Wafer Fabrication. *IEEE Transactions on Semiconductor Manufacturing*, Vol. 1, No. 3, pp. 115-130.
21. Wein, L. M. and Chevalier, P. B.(1992), A Broader View of the Job-Shop Scheduling Problem. *Management Science*, Vol. 38, No. 7, pp. 1018-1033.
22. Weng, W. W. and Leachman, R. C.(1993), An Improved Methodology for Real-Time Production Decisions at Batch-Process Work Stations. *IEEE Transactions on Semiconductor Manufacturing*, Vol. 6, No. 3, pp. 219-225.