Design and Control of Interleaved Buck Converter in High Power Applications

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Abstract

This paper presents design of interleave configured dc-dc converter for high power distributed power system applications. The multi channel interleaving buck converter with small inductance has proved to be suitable for micro-grid, requiring medium output voltages, high output currents and fast transient response. Integrated magnetic components are used to reduce the size of the converter and improve efficiency. Unlike conventional methods, the distributed approach requires no centralized control, automatically accommodates varying numbers of converter cells, and is highly tolerant of subsystem failures. A general methodology for achieving distributed interleaving is proposed, along with a specific implementation approach. The design and simulation verification of switching frequency 10 kHz system is presented with interleaved clocking of the converter cells. The simulation (simulated by PSIM 6.1) results corroborate the analytical predictions and demonstrate the tremendous benefits of the distributed interleaving approach.

Keywords: Interleaved buck converter, phase shift gate pulse, ripple cancellation, output passive filter

Nomenclature

V_o	output dc voltage
I_o	output dc current
L_1, L_2,L_3,L_4	are inductance of converter cell
C_f	capacitance of filter capacitor
N	number of cell
f_s	switching frequency
f_r	rectified ripple frequency
D	duty ratio
D1, D2, D3, D4	are diodes of individual cell
Q1, Q2, Q3, Q4	are switches of individual cell

I. Introduction

High power converter has become the essential part of the distributed power system that enables energy to be fully utilized in photovoltaic power and stationary power systems (see Fig.1). The design and simulation verification of switching frequency 10 kHz system is presented and quantitative performance comparisons are made between synchronized clocking, independent clocking and interleaved clocking of the converter cells as in Fig.4.

The rms input and output current ripples will be reduced by a factor of $N^{1/2}$duetothepassive(stochastic) ripplecancellation,whichoccursamongcells [1]. In the interleaving method, the cells are operated at the same switching frequency with their switching waveforms displaced in phase over a switching period. This paper presents analysis and design of a high-power multi-leg interleaved buck converter with typical proportional integral controller. A 250-kW converter was designed with small rating inductors to allow core-loss reduction and designed with high frequency switching to minimize the component size and eliminate the switching losses under discontinuous conducting mode operation [1].A major design aspect in a high power converter is the selection of the cell inductor. The major concern here is the size and weight of such a high power inductor that is perhaps the single heaviest component in the entire converter. In order to reduce the inductor size and weight, a small inductance value is preferred. In this case, the converter is typically designed with DCM operation. The problem with DCM operation is the high input current ripple, which is highly objectionable for a fuel-cell type source. In order to reduce the input current ripple, the converter can be designed with multiple legs interleaving each other allowing for ripple cancellation. For high power applications, the technique

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has not been widely used. In this paper, the interleaved technique with minimum inductors is proposed for high-power applications to reduce the size and weight of the inductor and at the same time to reduce the energy stored into the passive element. Simulation and

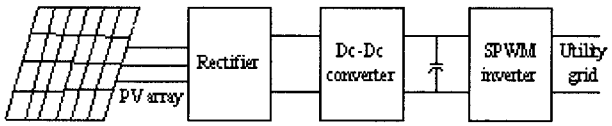

Fig.1. Block diagram of a distributed power system

theoretical results show that the steady-state current ripple is reduced with higher equivalent inductance and the center leg of the EE core has a further reduced ac current ripple. A means for implementing the new approach is described, and some of the major design issues are addressed [2].

The proposed control uses interleaving techniques based on a phase shift PWM gate pulses diagram (in Fig.4). In Section II, main aspects of the interleaved conversion based on current-mode control (CMC) are presented. A control scheme is performed in Section III between voltage and current control interleaved converter considering identical inductive stored energy in both cases. Ripple cancellations in the converters and duty cycle values as well as alternative control modifications are discussed in Section IV. Simulated results are presented in Section VI for four interleaved switching cells. Advantages of interleaved conversion based on CMC are then summarized in Section VIII.

II. 4-Cell Interleaved Buck Converter

Figure 2 has shown the basic structure of proposed high power dc-dc converter. The proposed interleaved converter based on buck structures in parallel and the use of current mode control is depicted in Fig.3. The status of the switches is represented by a binary code. Namely, "1" switch on and "0" switch off. From the possible binary states, a concrete state-transition cyclic sequence is chosen in order to generate the required phase shift among the converter waveforms when applied to the switches control. In steady state, all the binary states have the same duration and the cyclic sequence imposes a complementary duty cycle for each state, this resulting in an average output voltage value of times the input voltage. The source characteristics

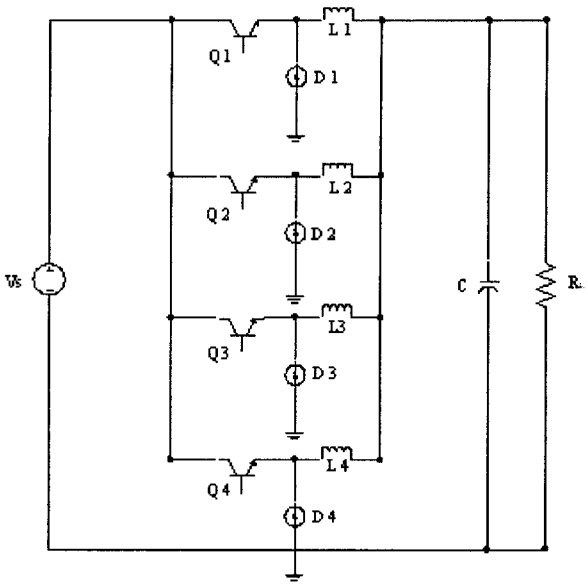

Fig.2. Proposed 4-cell interleaved buck converter

and the topology of the interconnection of the modular switching cells determine their control strategy. In most of the practical cases, the source has a nearly voltage source characteristic.

It has been found that switched-mode converters exhibit in natural way (without control) specific two-port characteristics, such as transformers, gyrators, and loss-free resistors [3]. In the case of voltage mode control, the converter is actually equivalent to a transformer, and in the case of CMC to a gyrator [3]. Interconnection of modular interleaved switching cells can be represented by means of a two-port parallel configuration. In the case of voltage-controlled switching cells (Fig. 2), the transfer ratios of the transformers must be equal and slight variations imply high circulating currents between voltage sources. These currents are practically limited only by the small resistance in series with each of the voltage sources. In the case of CMC, the equivalent gyrators transform the voltage source into current sources connected in parallel. It is easy to see that such a type of arrangement is not sensitive to variations in the gyration conductance of the gyrators. Based on the previous discussion, it is clear that CMC is more suitable than a voltage control method in the case of parallel topology [3]. The simplest case of interleaving corresponds to whose corresponding state-transition diagram is illustrated in Fig. 4.

Figure 3 shows an application diagram of the proposed controller. The justification for using an interleaved

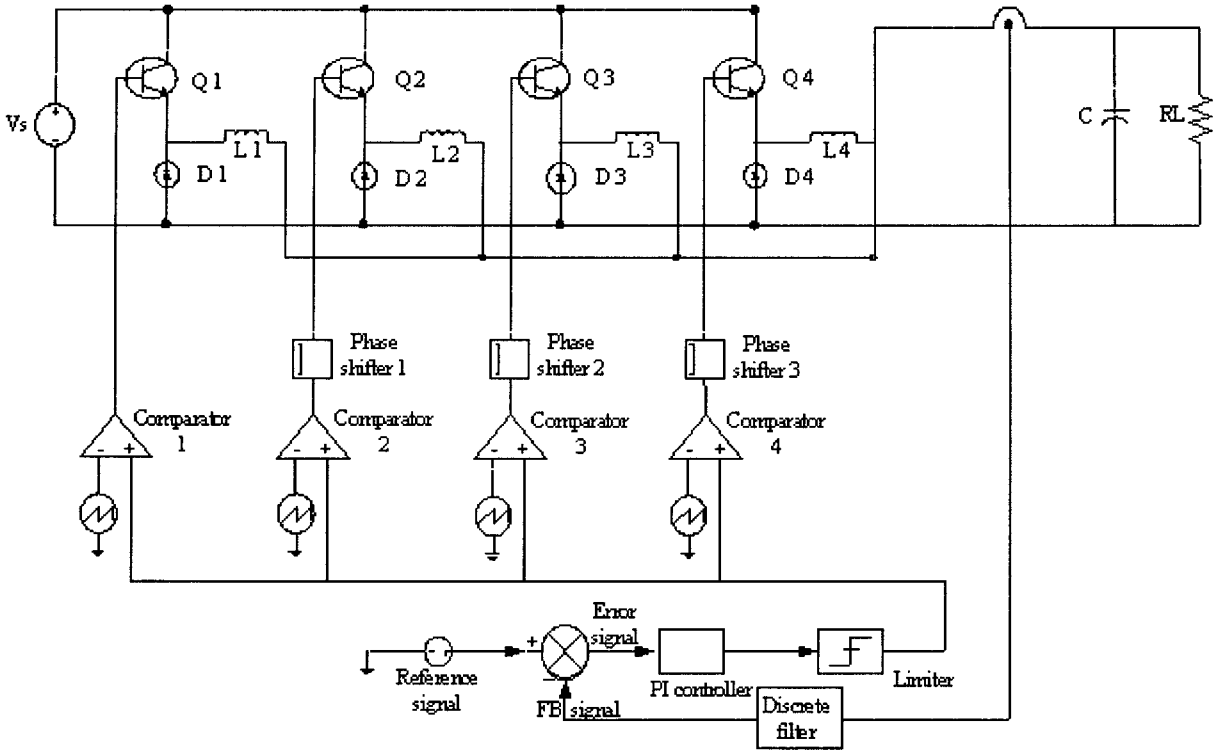

Fig. 3. Control diagram of 4-cell interleaved buck converter.

Digital circuits are potentially less susceptible to noise and parameter variations. With the recent explosion of cheap computing power, and availability of advanced integrated circuit design and synthesis tools, a digital controller design can be ported to new integrated circuit technology generations with little additional effort. In this paper, we focus on the design of an analog controller for an interleaved dc-dc buck converter for micro-grid or stand alone power system.

A simple design and implementation process of the compensators for the feedback loops is presented so as to attain the desired response of the system. A simple controller is obtained for a 4-phase interleaved converter which can be easily be implemented on a simple platform. The discrete-time filter structure of such implementation is also presented; the desired accuracy of the output current can easily be realized using controllers operating at high clock frequencies well into desired range. Thus there is need to develop algorithms for designing the control loops. Having obtained these transfer functions for a multi-loop controller, a digital system needs to be designed which gives the same performance as this analog counter part. Normally the discrete-time systems are derived using the pole-zero mapping or by using zero-order-hold (ZOH) sampler.

The sampling frequency should be chosen such that it is much higher than the open-loop resonant frequency of the converters. ($w0$ =1/ vLC).

$$\Delta\varphi_m = -\frac{\omega T_s}{2} \tag{1}$$

where is the gain cross over frequency[6]. This reduction in the phase margin becomes worse when the sampling rate is low. At those sampling frequencies, direct conversion of continuous time controllers to discrete-time controllers may not be suitable. As mentioned above, sampling frequency plays a major role in determining the system performance of the systems. In the analog system, the phase margin of the compensated system is 60 degrees, while in the digital system with different sampling frequencies the system performance has degraded with the lower of sampling frequency [6].

Figure 4 shows the typical gate pulse sequences of an interleaved buck converter with four phases. The gate drive signals are operated in quadrature as shown figure.

IV. Ripple Calculations

One of the main features of interleaved converters is the ripple reduction. Previous works have quantified the system improvement comparing the waveforms obtained in interleaving with waveforms obtained either in a single converter or in a synchronous parallel connection. In the first case, the comparison is carried out considering identical inductors whereas in the second case the converters are compared on the basis of identical inductive stored energy. In the work here reported, the interleaved converters operate in continuous conduction mode (CCM) at an optimum duty cycle in order to minimize the ripple. The ripple comparative analysis is made between a single and an interleaved converter considering identical inductive stored energy as in [3].

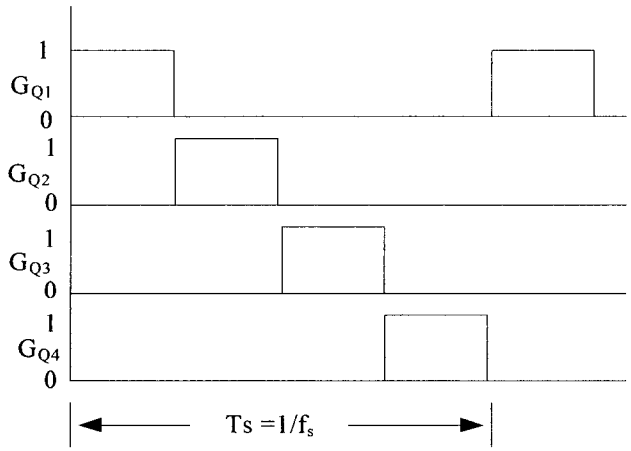

Fig.4. Interleaving gate clock pulse of proposed converter.

V. Output Filter Optimization

In order to properly design the output filter of the multiphase buckconverter it is convenient to represent, in a log plot, the required output capacitance and equivalent inductance, *L*eq, of the converter, that meet all the design restrictions. The equivalent inductance is defined as:

$$L_{eq} = \frac{L_{cell}}{N} \qquad (2)$$

where *L*cell is the inductance per cell and *N* is the number of cells.

Neglecting *R*ESR , it is possible to calculate the *L*eq, *C* pair to meet the required output voltage ripple. This is a reasonable assumption since, as shown above, the *CR*ESR product decreases with the capacitance:

$$C.L_{eq} = 0.03125 \frac{V_{in}}{\Delta V_o N^3 f_s^2} \qquad (3)$$

This equation shows how the *CL*eq product decreases with a power of three with the number of cells. This means that if the number of cells is increased from 1 cell to 8 cells, keeping the same equivalent inductance, the output capacitor could be 512 times smaller. The effect of increasing the switching frequency, from the point of view of the ripple, is similar to increase the number of phases, in the sense that it reduces the *L*eq *C* product [5].

VI. Simulation Results

The output voltage and current waveforms are depicted in Fig.5. Theoretical analysis presented so far has been verified by simulation of a four-phase channel buck converter using PSIM 6.1. The specification of the buck converter is as Table1. Steady state ripple wave forms of 4-cell converter are depicted in Fig.6.
In Fig.7 presents inductor current of each channel. This figure has shown discontinuous current mode due to small values of inducto

Table 1. Proposed circuit paramete

Dc input voltage [*V*dc]	900 V
Output voltage [*V*o]	600 V
Output current [ILoad]	400 A
Switching frequency [*f*s]	10 kHz
Inductance of each module inductors [L]	50 H
Capacitance of filter capacitor[*C*f]	100 F
Resistive load [*R*L]	1.53 Ω

In Fig. 8, the simulation results are shown inductor and capacitor current waveforms. Capacitor is also optimum designed as shown in current waveform is equal format. Switching voltage and current waveforms has shown in Fig.9. Switches are turn-on at zero current condition

VII. Analysis of Switching and Conduction Loss

In the buck converter, switching losses include switch turn-on loss and switch turn-off loss, as

illustrated in Fig. 9. At turn-on transition, two time intervals tri and tfv are mainly involved. Therefore, the turn-on switching loss can be approximated as

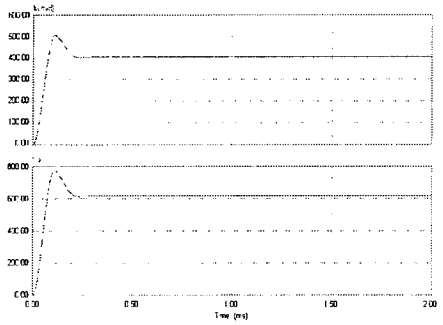

Fig.5. Simulated output voltage and current waveforms.

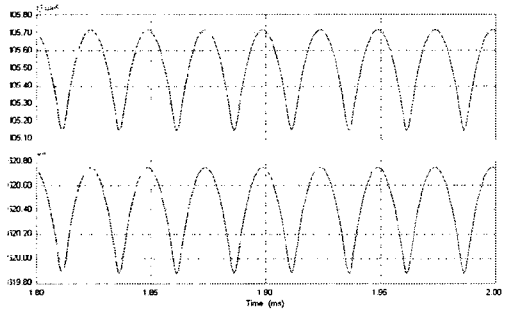

Fig.6. Ripple in output voltage and current waveforms.

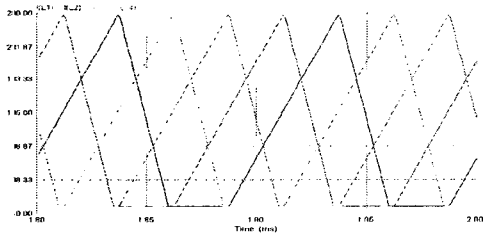

Fig.7. DCM inductor current of each channel.

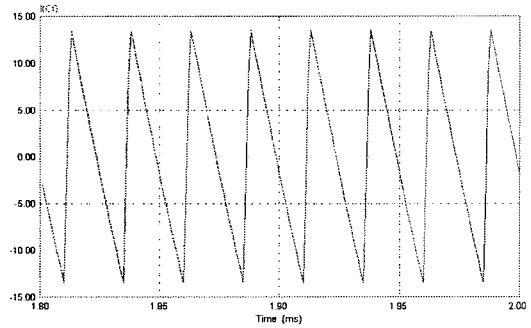

Fig.8. Capacitor current of output filter.

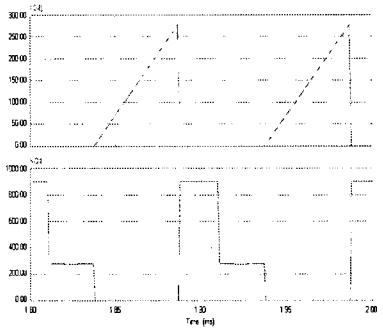

Fig.9. Switching voltage and current waveforms.

VII. Analysis of Switching and Conduction Loss

In the buck converter, switching losses include switch turn-on loss and switch turn-off loss, as illustrated in Fig. 9. At turn-on transition, two time intervals tri and tfv are mainly involved. Therefore, the turn-on switching loss can be approximated as

$$W_{son} = \frac{t_{son}}{2} V_s I_{stn} \quad (4)$$

where tson= tri +tfv, Vs is the voltage across the switch and Istn is its current. During turn-off transition, another two time intervals, trv and tfi, are involved and the turn-off switching loss can be approximated as

$$W_{soff} = \frac{t_{soff}}{2} V_s I_{stf} \quad (5)$$

where tsoff= trv +tri. From (3) and (4), the total switching losses over a switching cycle can be determined as follows:

$$W_T = \frac{1}{2} V_s (t_{son} I_{stn} + t_{soff} I_{stf}) \quad (6)$$

where ton= DT is the conduction time, Istn is the initial current, Istf is the peak current, and Rds is an equivalent conduction resistance of the switch. Therefore, if the buck converter is operated at the boundary of CCM and DCM, Istn is equal to zero and the conduction loss can be expressed as follows:

$$W_{CL} = \frac{1}{3} t_{on} R_{ds} (I_{stn}^2 + I_{stn} \cdot I_{stf} + I_{stf}^2) \quad (7)$$

$$W_{CD} = \frac{1}{3} t_{on} R_{ds} I_{stf}^2 \quad (8)$$

VIII. Conclusions

In this paper, an exhaustive analysis of the effect of the number of cells on the passive components for interleaved buck converters has been carried out. The analysis has been performed with actual components and technologies and the implication of the number of cells on the use of better technologies has been highlighted. Based on the designs for this application, experimental relations between volume, energy and losses have been established. The input capacitor could be strongly reduced by ripple cancellation if all the cells where closely connected to same input point. From a practical point of view, as the input capacitors should be placed very close to each phase the power stage, they will only benefit from the IRMS reduction, almost proportional to the number of phases. Additional improvement can be achieved if the capacitance reduction allows a change in the capacitor technology. The output capacitor will rapidly decrease with the number of phases allowing the use of better technologies that will improve further the behavior of theses devices. An output filter optimization process has been shown providing some design rules. All results and discussions are based on simulation and theoretical point of view.

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