A Low-Noise and Small-Size DC Reference Circuit for High Speed CMOS A/D Converters

Sanghoon Hwang and Minkyu Song

Abstract—In a high-speed flash style or a pipelining style analog-to-digital converter (A/D converter), the DC reference fluctuation caused by external noises becomes serious, as the sampling frequency is increased. To reduce the fluctuations in conventional A/D converters, capacitors have been simply used, but the layout area was large. Instead of capacitors, a low-noise and small-size DC reference circuit based on transmission gate (TG) is proposed in this paper. In order to verify the proposed technique, we designed and manufactured a 6-bit 2GSPS CMOS A/D converter. The A/D converter is designed with a 0.18um 1-poly 6-metal n-well CMOS technology, and it consumes 145mW at 1.8V power supply. It occupies the chip area of 977um by 1040um. The measured result shows that SNDR is 36.25 dB and INL/DNL is within 0.5LSB, even though the DC reference fluctuation is serious.

Index Terms—High-speed A/D converter, low-noise DC reference circuit, transmission gate

I. INTRODUCTION

The demands for analog/digital interface are now being increased, according to the development of SOC (System-On-Chip) technique. Specially, a high-speed and low-power A/D converter is a key component to improve the SOC performance in the area of analog/digital interface. Thus many kinds of A/D

converters have been reported, but the best-known architectures for a high-speed A/D converter are the flash style and the pipelining style. At the present time, the reported flash type A/D converters are the 6-bit 4GSPS A/D converter [1], the 6-bit 1.6GSPS A/D converter [2], and so on. Further, the 10-bit 200MSPS A/D converter [3], the 12-bit 50MSPS A/D converter [4], and others are reported with a pipelining style.

However, the high-speed architectures have two main problems that impair the dynamic performance of the A/D converters: timing and distortion. The two problems become serious, as the clock speed is increased. Firstly, in terms of timing errors, there are four main sources of them: the sampling clock jitter, the limited rising and falling time of the sampling clock, the skew of the clock and input signal at different places on the chip, and the signal-dependent delay. Therefore, the design techniques considering the relative delay time and careful layout are required to reduce the timing errors [5]. With those considerations, most of timing errors can be reduced.

Secondly, the distortion of quantized signal can be generated from five main reasons: the sampling aperture time, the distortion in input, the offset in input amplifier, the changes in the reference voltage values, and the delays of analog signal and clock signal. Among them, the most serious problem in a high-speed A/D converter is the DC reference fluctuation caused by a clock feed-through and kickback errors at the comparator stage. Most of the high-speed A/D converters require a large number of DC reference voltages that are normally designed with a resistive divider. The DC reference voltage is fluctuated by clock errors, because the value of the resistor impedance is not infinite. The errors in these reference voltages introduce a nonlinear distortion

in the input amplifier. During the sampling period of the input signal, further, the reference voltage temporarily deviates from the nominal value, resulting in additional quantization errors. It degrades INL (Integral Non-Linearity) and DNL (Differential Non-Linearity) of A/D converter [5][6]. As the clock speed is increased, the DC reference fluctuation becomes more serious. Therefore the reduction of DC reference fluctuation is one of the main issues for a high performance and high-speed A/D converter.

Many conventional A/D converters employed simple capacitors to attenuate the DC reference fluctuation. The reference fluctuation is compensated easily, but the required value of capacitor is increased for high performance. Consequently, it occupied large chip area. In this paper, for that reason, a novel efficient fluctuation-attenuation circuit based on transmission gate is proposed

The contents of the paper are as follows. In Section II, the phenomena of a DC reference fluctuation are presented. In Section III, the quantitative analysis of the proposed reference-attenuation circuit is discussed, and the verified performance with experiment is shown. The fabrication results and measured results are described in Section IV. Finally, the conclusions are summarized in Section V.

II. REFERENCE FLUCTUATION

1. Reference Voltage Fluctuation

Fig. 1 (a) shows a simple block diagram of a flash type ADC. The reference voltages are normally designed with a resistive divider. According to the operation of system clock, the comparators are worked either on or off. Especially, the signal distortion is generated from kick-back errors and channel charge injection, when the switch of comparator is off. Further, the kick-back errors are transferred to the resistor ladder through the input stage of comparator. It causes the DC reference fluctuation in A/D converter. Moreover, the reference fluctuation is increased by the fast operating frequency, as the conversion speed is becoming higher. Fig. 1 (b) shows the experimental result of reference fluctuation only using a resistor ladder. The fluctuation noise is about 10mV when the sampling clock is 2GHz.

(a)

(b)
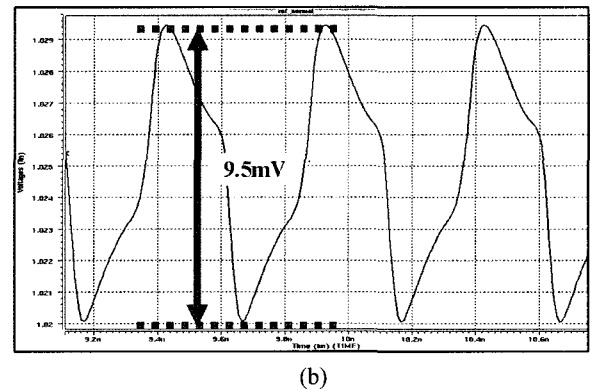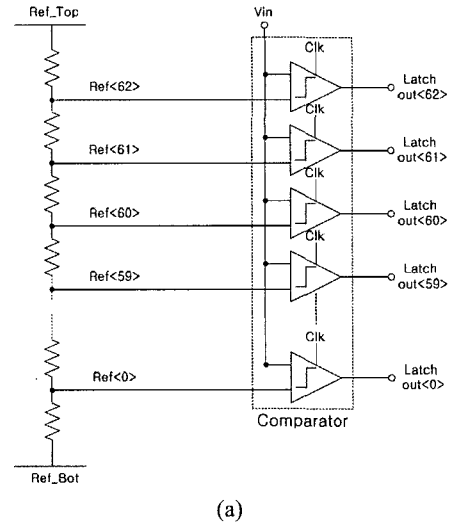
Fig. 1. Reference voltage fluctuation at resistor ladder: (a) the block diagram of reference generation (b) simulation results (only using resistor ladder).

2. Conventional Fluctuation-Attenuation Circuit

In general, the simple capacitors have been used for reduction of reference fluctuation in Fig. 2 (a) [7]. In the conventional technique, the reference fluctuation is attenuated by an equivalent simple 1st order LPF (Low Pass Filter). Hence, the performance of LPF is good, as the capacitor value is increased. However, it has a disadvantage that the layout area is large (the number of capacitor is the same as the number of comparator). If the capacitor value of a reference is increased by 1pF, the area of capacitor layout becomes twice. Fig. 2 (b) shows the comparison of simulation results for the two cases of no-capacitor and with-capacitor. When the capacitor value is 1pF, the reference fluctuation is reduced to 0.42mV from 10mV (the fluctuation is decreased to 1/23).
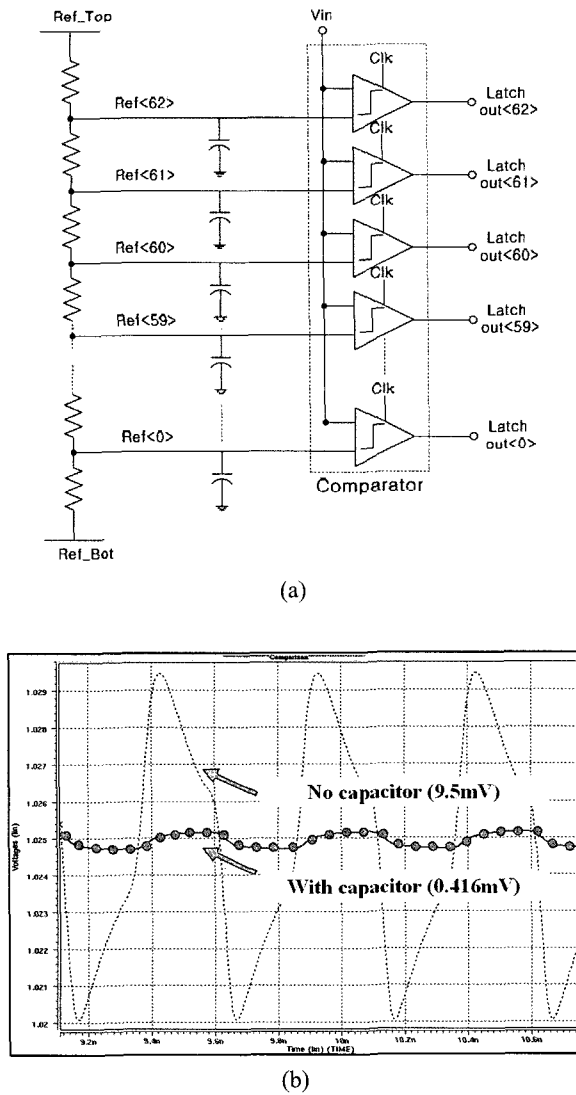
(a)

(b)

Fig. 2. Conventional fluctuation-attenuation circuit (a) the block diagram using capacitor (b) the simulation results.

III. DESIGN OF THE PROPOSED CIRCUIT

1. The Proposed Circuit

The proposed DC reference fluctuation-attenuation circuit is shown in Fig. 3. The proposed circuit is composed of transmission gate (TG) switches. Further, a PMOS gate and a NMOS gate are connected to VDD and GND, respectively. Namely, the TG switches are always turned on. As a consequence, the parasitic capacitance and resistance of MOS are built up in TG switches. Thus the proposed DC reference fluctuation-attenuation technique uses the parasitic capacitance and resistance of MOS, instead of a simple capacitor. The
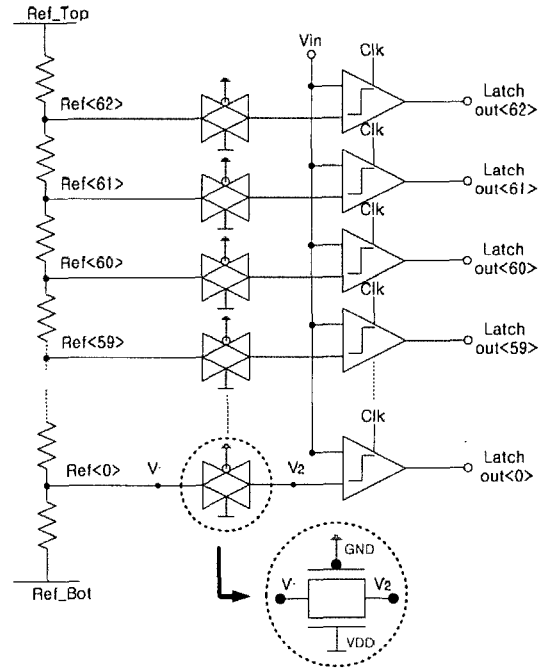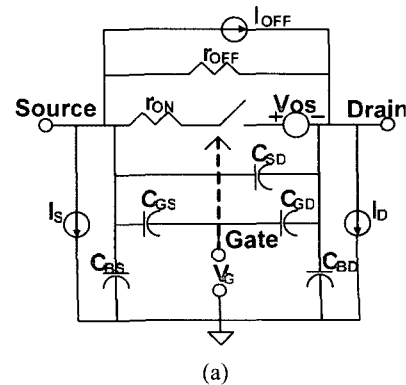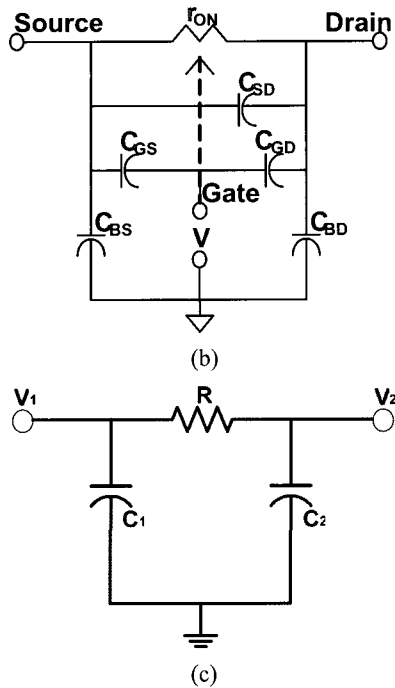

Fig. 3. The proposed fluctuation-attenuation circuit.

proposed technique reduces the reference fluctuation more efficiently than the conventional technique.

2. Equivalent Model of the Proposed Circuit

Fig. 4 (a) presents the model of a non-ideal MOS switch. The voltage V_G controls the state of the switch-ON or OFF. The voltage-controlled switch is a three-terminal network; drain, source, and gate. The most important characteristics of a switch are its ON resistance, r_{ON}, and its OFF resistance, r_{OFF}. Ideally, r_{ON} is zero and r_{OFF} is infinite. However, the reality is such that r_{ON} is never zero and r_{OFF} is never infinite [6][8]. Moreover, these values are not constant with respect to the change of terminal conditions. The parasitic


(a)

Fig. 4. Modeling of a switch: (a) model for a non-ideal switch (b) analysis while switch is on (c) final model of TG (CRC-Model).

capacitors are an important consideration in the application of analog circuits. The proposed reference fluctuation-attenuation circuit is based on the characteristics of a parasitic resistor and capacitor in a MOS switch. The general model of TG switch in ON state is shown in Fig. 4 (b). From Fig. 4 (b), the final model of TG switch is approximated by one r_{ON} and two capacitors (CRC-Model) in Fig. 4 (c).

3. Analysis of the Proposed Circuit

Fig. 5 shows the noise model of the DC reference with TG, where v_1 is defined to be the node voltage of a DC reference, and v_2 is defined with the input node voltage of comparator. Fig.5(a) introduces an equivalent model of small signal from v_1 node to v_2 node using the CRC-model. In this model, R_1 represents the resistor ladder. After a simple analysis shown in Fig.5(a), the final model is approximated to Fig.5(b) by using the Thevenin's theorem. Thus the v_2 node is operated like a 2nd order LPF by the model of the proposed circuit. Even with the fluctuation of the external noise, v_{ref_noise} node, the reference fluctuation is drastically attenuated by the proposed circuit.

(a)

(b)
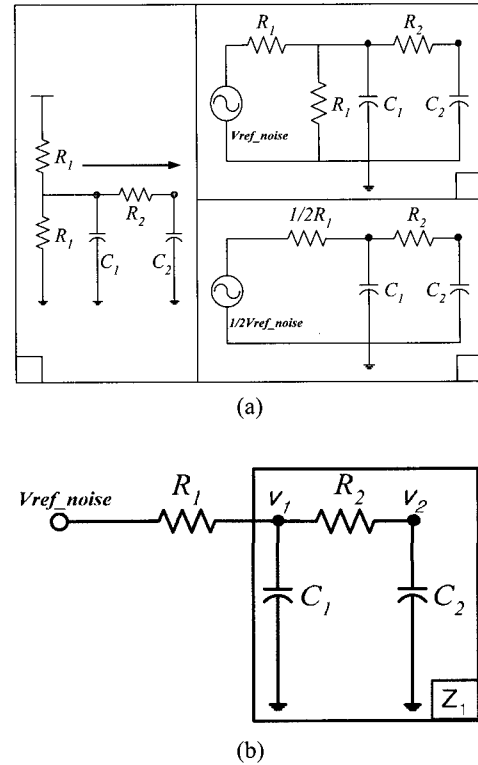
Fig. 5. Model for external noise: (a) modeling process from reference voltage to comparator input node (b) final model.

Quantitative analysis to reduce the reference fluctuation by external noise is as follows:

$$\frac{v_2}{v_{ref\_noise}} = \frac{1}{s^2 R_1 R_2 C_1 C_2 + s(R_1 C_1 + R_2 C_2 + R_1 C_2) + 1} \quad (1)$$

From (1), the transfer function (from v_1 to v_2) represents the 2nd order RC LPF. Thus most of the high frequency external noise is eliminated at the proposed circuit.

4. SPICE Results and Comparison of Layout Area

The performance and correspondence of the modeling of the proposed circuit are verified by SPICE simulation. As shown in Fig. 6, the CRC-Model results are compared with the performance of the proposed circuit. The CRC-Model gives 0.2mV and the proposed circuit gives 0.21mV at the clock frequency of 2GHz. Thus the equivalent CRC model is well fitted to the circuit of TG.

Fig. 7 shows the simulation results of both the simple capacitors and the proposed circuit. The reference fluctuation of the proposed circuit is reduced by 50%, compared to that of the simple capacitors. The layout
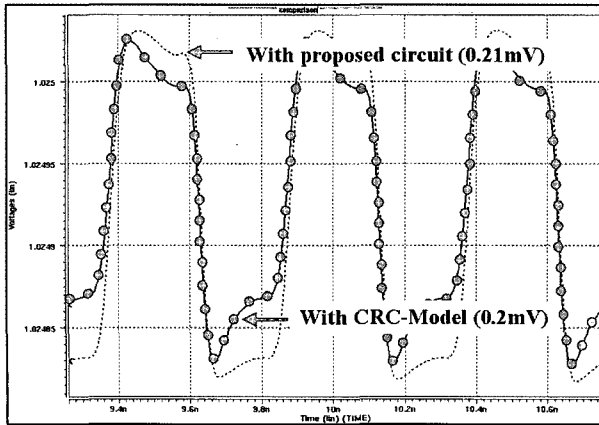
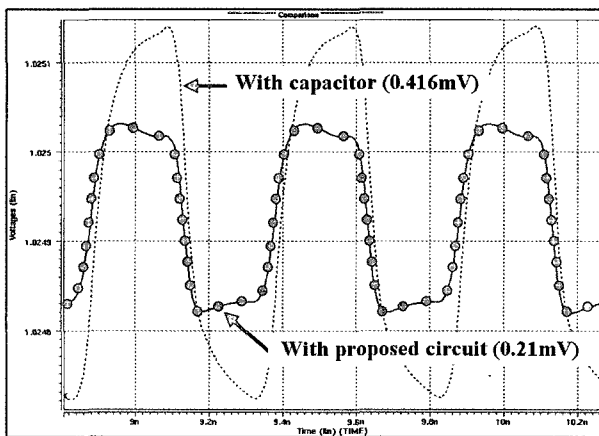**Fig. 6.** Simulation results of proposed circuit and CRC-Model at 2GHz.

Fig. 7. Simulation results of the proposed circuit and simple capacitor at 2ghz.

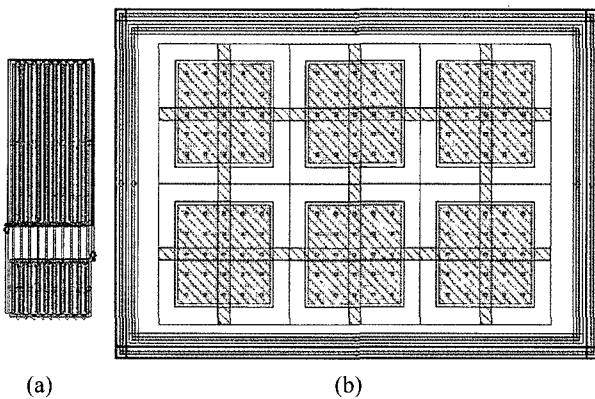(a)   (b)

Fig. 8. The comparison of layout: (a) proposed transmission gate (b) capacitor of 1pf.

comparison between the proposed circuit and a simple capacitor (1pF) is shown in Fig. 8. The layout of the proposed circuit is smaller by 17% than that of a simple capacitor with 1pF. Therefore, the proposed reference

fluctuation-attenuation circuit has a better performance and smaller chip area, compared to those of the conventional technique [9]-[12].

IV. EXPERIMENTAL RESULTS

1. Design of an A/D converter

The block diagram of the designed A/D converter is shown in Fig. 9(a). A PLL and a down converter are included in the chip. Fig. 9(b) represents the SPICE
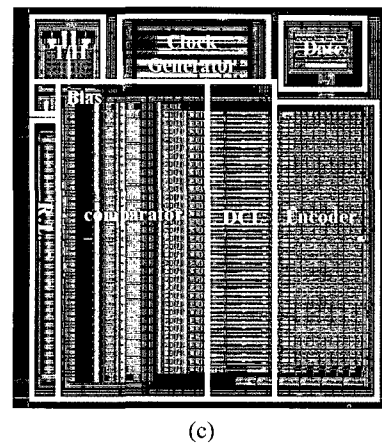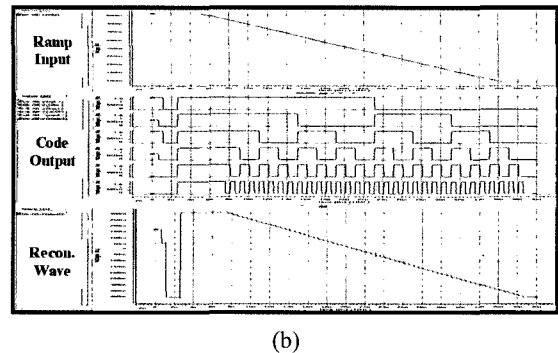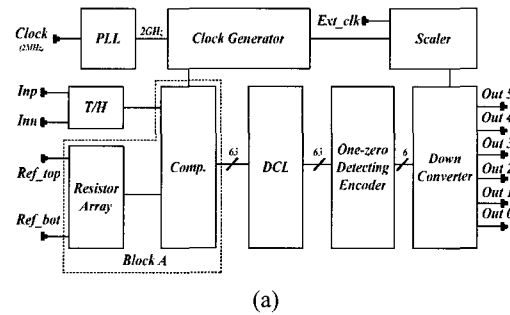

(a)

(b)

(c)

Fig. 9. A 6-b 2GSPS A/D converter: (a) block diagram of the A/D converter (b) spice simulation results (c) chip layout drawing.

results (digital output and reconstruction wave) with a full code in ramp signal input. Fig. 9(c) shows the layout drawing of the ADC. The analog power and digital power are separated for deducing the effect of power noise. Moreover, many wells and GND lines are used for protection of main signal. The effective chip area is 977um by 1040um.

2. Measured Results

The photograph of the packaged chip, instead of the internal microphotograph, is shown in Fig.10. The fabricated chip is measured by Compu-Scope 3200, a data-converter analyzer system.

The fluctuation of DC reference voltage by external noise is measured for verification of the proposed circuit. As shown in Fig. 11, the variation of reference voltage by external noise is about 40mV. Therefore, the reference voltage is fluctuated by an external noise above 5LSB, when we consider that 1LSB is about 7.8mV. In spite of this measurement condition, the performance of measured A/D converter is excellent from Fig. 12. Fig. 12(a) shows the digital output code and reconstruction wave, when the input frequency is 2MHz at the 2GHz sampling clock. Further, the measured INL and DNL of the ADC are within 0.5LSB from Fig. 12(b). The measured ENOB according to input frequency (at Fs=2GHz) is represented in Fig. 12(c). Therefore, we have a conclusion that the external noise is reduced by the operation of LPF at the proposed DC reference fluctuation-attenuation circuit.
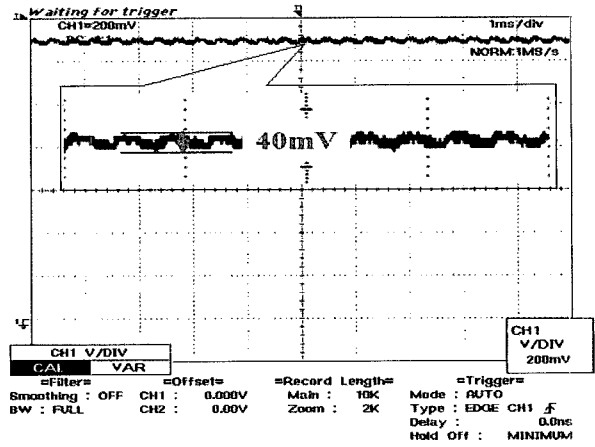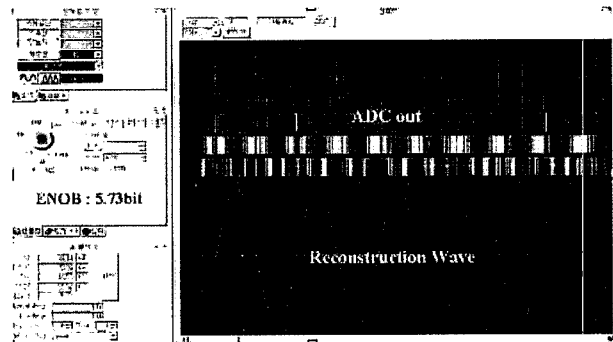

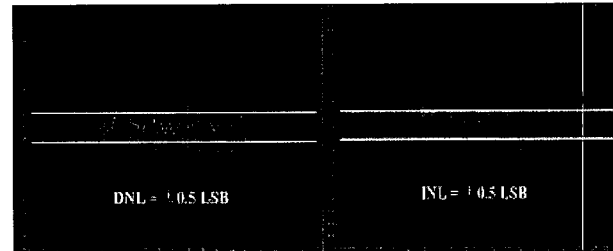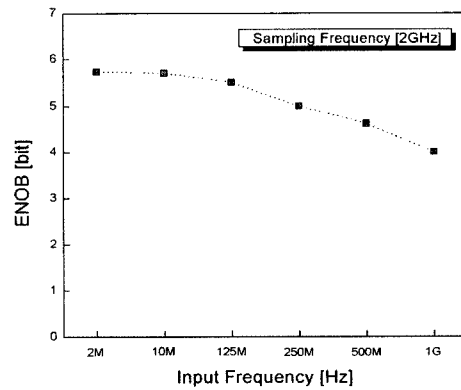**Fig. 11.** Reference fluctuation by external noise.

(a)

(b)

(c)

Fig. 10. Photograph of the packaged chip.

Fig. 12. Measured results: (a) digital output code and reconstruction wave (b) measured INL and DNL (c) measured ENOB.

V. CONCLUSIONS

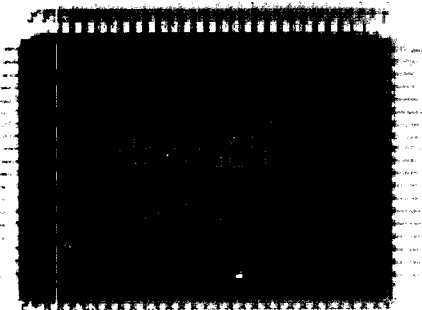A low-noise and small-size DC reference circuit was described for a high-speed CMOS A/D converter. From a small signal modeling and analysis, the external noise was reduced by the proposed circuit. Furthermore, it was verified that the proposed circuit with TG switch is better than the conventional one in the performance and chip area. The reference fluctuation was reduced by about 50% and the layout area was decreased by 17%, compared to those of the conventional one. Excellent measured results were demonstrated for a 6-bit 2GSPS CMOS A/D converter with the proposed circuit, even though an intentional external noise was injected. Therefore, the proposed DC reference fluctuation-attenuation circuit reduced the fluctuation noise efficiently in high-speed A/D converter. The performance was summarized in Table 1.

Table 1. Performance summary of the measured ADC.

Resolution	6bits
Input Freq.	Nyquist
Sampling Freq.	2GSPS
Power Supply	1.8V (Analog + Digital)
Analog Input Range	Diff. 1Vpp
DNL / INL	< 0.5LSB
SNDR	36.25dB (Fin=2MHz, Fs=2GHz)
Power Dissipation	145mW
Core Area	977um X 1040um
Process	Hynix 0.18um 1 poly 6 metal N-well CMOS

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Sanghoon Hwang received the B.S., and M.S. degrees in Semiconductor Science from Dongguk University, Korea in 2001, and 2004, respectively. From 2004, he is working toward to obtain Ph.D. degree at Department of Semiconductor Science, Dongguk University. His major interest is design of CMOS analog circuits, mixed-mode circuits, and low power circuits.

Minkyu Song was born in Seoul, Korea, in 1963. He received the B.S., M.S., and Ph.D. degrees in Electronics Engineering from Seoul National University, Korea in 1986, 1988, and 1993, respectively. From 1993 to 1994, he was a researcher at University of Tokyo, Japan where he worked in the area of low power VLSI design. From 1995 to 1996, he was a researcher in the CMOS Analog Circuit Design Team of Samsung Electronics, Korea. Since 1997, he has been a professor at University of Dongguk, Korea. He is a member of IEEE, IEICE, and IEEK. His major interest is design of CMOS analog circuits, mixed-mode circuits, and low power digital circuits.