A CMOS 5-bit 5GSample/Sec Analog-to-digital Converter in 0.13um CMOS

I-Hsin Wang and Shen-Iuan Liu

Abstract—**This paper presents a high-speed flash analog-to-digital converter (ADC) for ultra wide band (UWB) receivers. In this flash ADC, the interpolating technique is adopted to reduce the number of the amplifiers and a linear and wide-bandwidth interpolating amplifier is presented. For this ADC, the transistor size for the cascaded stages is inversely scaled to improve the trade-off in bandwidth and power consumption. The active inductor peaking technique is also employed in the pre-amplifiers of comparators and the track-and-hold circuit to enhance the bandwidth. Furthermore, a digital-to-analog converter (DAC) is embedded for the sake of measurements. This chip has been fabricated in 0.13μm 1P8M CMOS process and the total power consumption is 113mW with 1V supply voltage. The ADC achieves 4-bit effective number of bits (ENOB) for input signal of 200MHz at 5-GSample/sec.**

Index Terms—**CMOS, Analog-to-digital converter (ADC), track-and-hold circuit, digital-to-analog converter (DAC)**

I. INTRODUCTION

The high-speed low resolution analog-to-digital converters (ADCs) become more and more important in high-speed analog interface applications such as hard disk read channel, radar, digital receiver, IEEE 802.15.3a wireless personal area network (WPAN) [1] receiver and so on. Based on IEEE 802.15.3a WPAN UWB applications, the signals using multi-band orthogonal frequency division multiplexing (MB-OFDM) occupy a bandwidth of 528MHz for every band. It requires the conversion rate at least higher than 1.06GSample/sec with 4-bit resolution [2]. The flash ADCs published in recent years achieve from 1.1GSample/sec [3-5] up to 40GSample/sec [6]. These high-speed ADCs usually require the relatively high supply voltage and power consumption. However, due to the rapid advances in CMOS technology, the channel length of MOS transistors is reducing to nano-meter scale. To use the MOS transistors with the low breakdown voltage and prolong the battery operating time, it is highly desirable to reduce both the supply voltage and power consumption. Therefore, a 5-bit flash ADC in a standard 0.13μm CMOS technology is presented in this paper.

In this paper, the linear and wide-bandwidth interpolating amplifier for low supply voltage is presented. This proposed ADC uses the interpolating architecture and scales inversely the transistor size of the cascaded stages to enhance the bandwidth. The interpolation resistor network not only reduces the number of interpolating amplifiers but also averages the offset voltage of the pre-amplifiers [7-9]. The active inductor peaking technique is also employed in the pre-amplifiers of the comparators and track-and-hold (T/H) circuit to improve the trade-offs in bandwidth and power consumption. For the sake of the measurements, a digital-to-analog converter (DAC) is also embedded in this chip. The ADC achieves 4-bit ENOB at 5-GSample/sec and dissipates 102mW with a supply voltage of 1V. The DAC dissipates 11mW.

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II. CIRCUIT DESCRIPTION

1. Architecture

The proposed ADC is shown in Fig.1. It is composed of a T/H circuit, a reference ladder, interpolating amplifiers, the interpolation resistor network, comparators, a bubble correction circuit and a current-mode DAC.

In the multi-stage cascaded amplifiers, the gain-bandwidth product of the amplifier is proportional to gm/Ctot, where gm is the transconductance and Ctot is the total output capacitance. According to the assumption and calculation in [10], if the transistor size of the first stage is scaled down by a factor of 2 with respect to the second stage, the total capacitance is reduced by a factor of 1.43. This ADC applies this principle from the interpolating amplifiers to the bubble correction circuit to extend the signal bandwidth.

The total capacitance from the interpolating amplifiers to the pre-amplifiers of the comparators in our ADC is given as

$$C_{tot} = 18Cout + 35(C_{in} + C_p) \quad (1)$$

where C_{in} and C_{out} are the input capacitance of the pre-amplifier and the output capacitance of the interpolating amplifier, respectively. C_p is the interpolating resistors and wire parasitic capacitance.

Assume the interconnection wire parasitic capacitance C_p, the output capacitance C_{out} of the interpolating amplifier and the input capacitance C_{in} of the pre-amplifier of the comparator is equal to 20fF, 100fF, and 180fF, respectively. Then the equivalent total capacitance C_{tot} equals to 8.8pF.

If we scale down the input capacitance of the pre-amplifier of the comparator by a factor of 2, C_{tot} becomes about 5.65pF and the simulated bandwidth also extends by a factor of 56%.

In the digital part, the digital circuit operating speed are determined by the gate delay of transistor turn-on resistance and wire resistance multiply the loading capacitance. If the transistor turn-on resistance, wire resistance, and loading capacitance are 20ohm, 5ohm, and 16pF respectively, then the delay time is 0.4ns. When we apply the inverse scaling in digital circuit, the transistor turn-on resistance or the loading capacitance will reduce to 10ohm and 8pF. Therefore, the gate delay time will also reduce from 0.4ns to 0.24ns or 0.2ns.

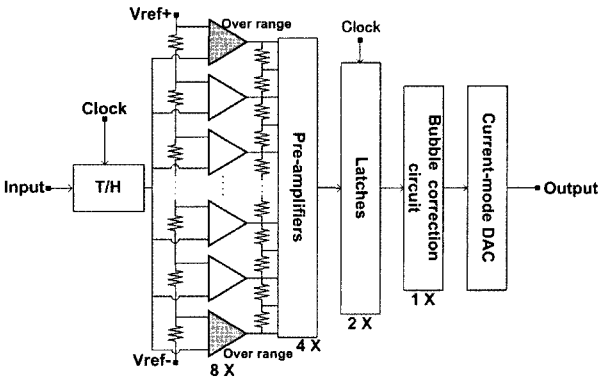


Fig. 1. The proposed ADC.

Thus, every cascaded stage is scaled down by two to achieve the wide bandwidth and enhance the speed of the proposed ADC.

2. Track-and-Hold Circuit

The proposed T/H circuit is shown in Fig. 2. It is composed of an input buffer and the fully differential

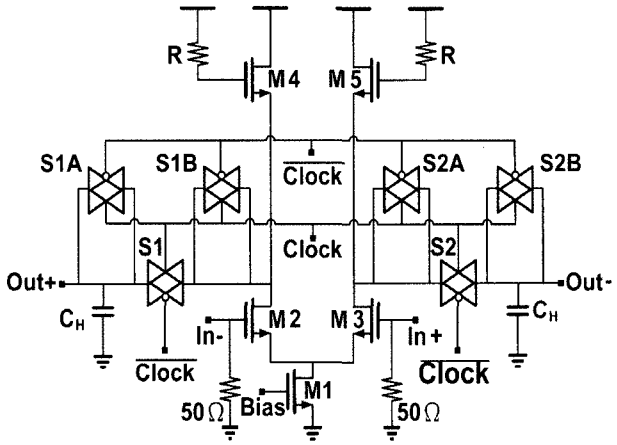


Fig. 2. The track-and-hold circuit.

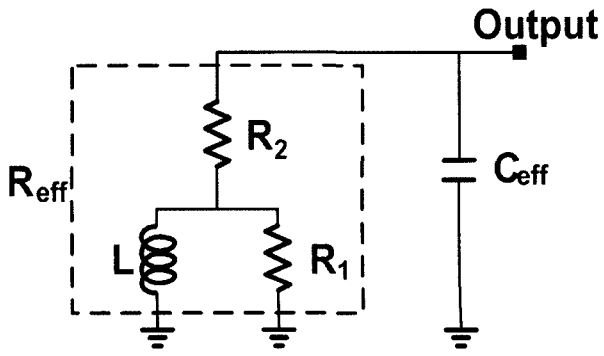


Fig. 3. The output equivalent model of the active inductor.

open-loop T/H circuit. Two resistors of 50ohm are used to have the wideband input impedance matching. The input buffer consists of the differential amplifier (M1-M3) and two active inductor loads (M4, M5 and resistors) [10]. The active inductor technique is aimed to boost the bandwidth and save the area without passive inductors.

This active inductor technique is also used in our pre-amplifier. At the output node of this source-coupled pair (M2 and M3), the equivalent output impedance is modeled as an R-C network, as shown in Fig. 3, and the bandwidth is determined by the time constant of $R_{eff} \times C_{eff}$. Assume the transconductance and gate-source capacitance of M4 and M5 are gm and C_{gs} respectively. In Fig. 3, R_1 equals to $R - 1/g_m$, R_2 equals to 1/gm, and L equals to $[C_{gs}(R - 1/g_m)]/g_m$, respectively.

Usually, R is larger than 1/gm, where gm is the transconductance of M4 and M5. The equivalent resistance and capacitance are given as

$$R_{eff} = \frac{\left[R/g_m - (1/g_m)^2\right]^2 + R^2(\omega L)^2}{R(\omega L)^2} \approx R \tag{2}$$

$$\begin{aligned} C_{eff} &= C_{load} - \frac{(R - 1/g_m)^2 L}{\left[R/g_m - (1/g_m)^2\right]^2 + R^2(\omega L)^2} \\ &\approx C_{load} - \frac{L}{(1/g_m)^2 + \omega L^2} \end{aligned} \tag{3}$$

where C_{load} is the load capacitance at the output of the source-coupled pair. According to eqs. (2) and (3), we can design the resistors and transconductance of MOS transistors to reduce the effective capacitance, C_{eff}, to extend the bandwidth.

When an NMOS transistor is used as a switch in T/H circuit, the voltage-dependent turn-on resistance induces the distortion. In this T/H circuit, for the sake of linearity considerations, the complementary transmission gates are used as the analog switches. Moreover, the intrinsic input capacitance of the interpolating amplifiers is utilized as the hold capacitor, CH. After the post-layout extraction, the input capacitance of the interpolating amplifiers, i.e., the hold capacitor is around 60fF.

In Fig. 2, for the analog switches, the size of the switches S1A and S1B (S2A and S2B) is chosen as half of that of S1 (S2). It is used to cancel the channel charge injection. The size of S1 (S2) is chosen as W/L=32μ/0.13μ and W/L=48μ/0.13μ for NMOS and PMOS transistors, respectively.

3. Interpolating Amplifier

In Fig. 1, at the boundaries of the interpolating resistor network, two dummy interpolating amplifiers are used for the over range termination. The interpolation factor is two in our ADC, so that the outputs of two interpolating amplifiers will generate an interpolated output. The conventional interpolating amplifiers are usually realized by source-coupled pairs with resistive loads. The slope of the transfer characteristic is equal to the transconductance multiplied by the load resistor. When input signal is small, the small-signal transconductance is given as

$$g_{ms} = \frac{I_S}{V_{GS} - V_{TH}} \tag{4}$$

where IS is the tail current of the source-coupled pair and $V_{GS} - V_{TH}$ is the overdrive voltage. When input signal is large, and the channel length modulation effect is considered, the transconductance becomes

$$g_{ml} = g_{ms}(1 + \lambda V_{DS}) \tag{5}$$

where λ is the channel-length modulation coefficient. It indicates that the transconductance has a variation factor of (1+λVDS) due to the channel length modulation so that large signals suffer from distortion by this gain error.

The interpolating amplifier does not require high gain. Its requirements are wide bandwidth and high linearity. To have the linear transfer characteristic, an interpolating amplifier is proposed as shown in Fig. 4. It uses two source-coupled pairs to compensate the non-linearity: one is with the positive transconductance and the source degeneration resistor; the other with the low negative transconductance. To operate in a low supply voltage, all transistors in this amplifier adopt the low threshold voltage (LVT) devices.

In Fig. 4, the degeneration resistor, RS, is equal to 10ohm and it is ignored in calculations. When input signal is small, the transconductance of the interpolating

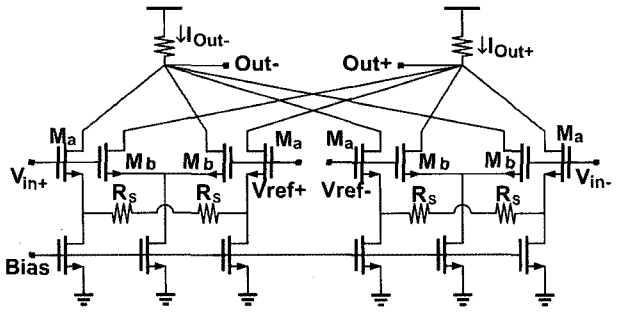


Fig.4. The proposed interpolating amplifier.

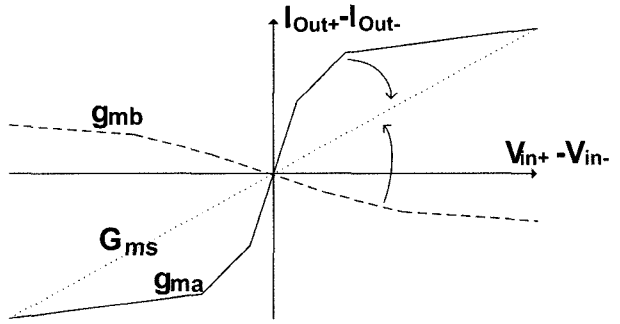


Fig. 5. The transfer characteristic of the output current in the proposed interpolating amplifier.

amplifier is

$$G_{ms} = g_{ma} - g_{mb} \tag{6}$$

where gma and gmb is the transconductance of Ma and Mb, respectively. The small signal is also linearly amplified. The transfer characteristic of the proposed interpolating amplifier is given in Fig. 5. The nonlinear characteristic of gma is compensated by gmb.

When input signal is large, consider the devices to have the same channel-length modulation coefficient. The transconductance of the interpolating amplifier is

$$G_{ml} = \left[g_{ma}(1 + \lambda V_{DSa}) - g_{mb}(1 + \lambda V_{DSb})\right] \tag{7}$$

where V_{DS} is the drain-to-source voltage. And, eq. (7) can be rewritten as

$$G_{ml} = G_{ms} + \lambda(g_{ma}V_{DSa} - g_{mb}V_{DSb}) \tag{8}$$

According to eqs. (5) and (8), the gain error is reduced by the term of gmbVDSb. Due to drain-source voltage, VDS, is a function of input signal, it can be approximated by a second-order polynomial

$$V_{DS}(V_{in}) \approx c_0 + c_1 V_{in} + c_2 V_{in}^2 \tag{9}$$

From eq. (5), the output current of the conventional interpolating amplifier is expressed as

$$I_{out} = g_{ms}(1 + \lambda c_0)V_{in} + g_{ms}c_1\lambda V_{in}^2 + g_{ms}c_2\lambda V_{in}^3 \tag{10}$$

Its nonlinearity introduces the harmonic distortion as

$$HD_{con} \approx \lambda(g_{ms}c_1 V_{in}^2 + g_{ms}c_2 V_{in}^3) \tag{11}$$

Similarly, from eq. (8), the harmonic distortion in our interpolating amplifier becomes as

$$HD_{new} \approx \lambda[(g_{ma}c_{1a} - g_{mb}c_{1b})V_{in}^2 + (g_{ma}c_{2a} - g_{mb}c_{2b})V_{in}^3] \tag{12}$$

Compared with eq. (11), the second-order and third-order harmonic distortions of the proposed interpolating amplifiers are reduced by the terms of gmbc1b and gmbc2b. According to the simulation, the total harmonic distortion is reduced from 8.04% to 4.64%.

4. Comparator

The comparator is shown in Fig. 6, where it is composed of the pre-amplifier, the latch, and the driver. The pre-amplifier is realized by a source-coupled pair with the active inductors [10]. The pre-amplifier provides the enough gain to reduce the kick-back noise. However, the active inductor has a disadvantage that the transistor threshold voltage limits output signal head room so that is difficult to drive digital signal. Therefore, the conventional differential latch with resistance loading is used in this comparator. The differential latch triggered by complementary clocks is used to store the digital output. The driver is realized by cascaded inverters. The transistor size of the inverters is inversely scaled down to improve the speed. The current sources in the pre-amplifier and the differential latch are realized by LVT devices for a low supply voltage.

For high speed operation, the logic circuits are implemented in source-coupled pair topology, so that requires the comparator output voltage larger than 1.41

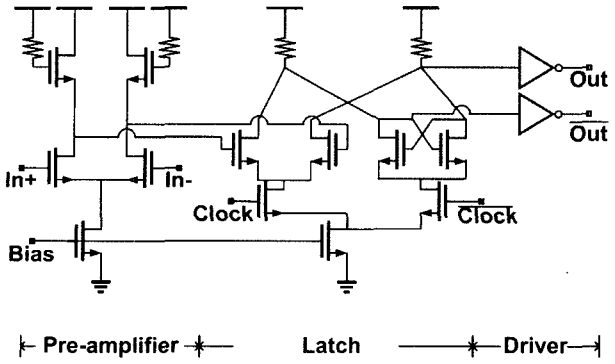


Fig. 6. Pre-amplifier & comparator schematic diagram.

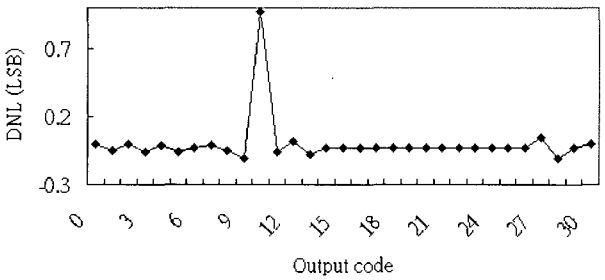
times overdrive voltage to switch the tail current. The latch regeneration time can be written as

$$T = \frac{\tau_0}{A-1}\ln\left(\frac{\sqrt{2}\Delta V}{V_{init}}\right) \tag{13}$$

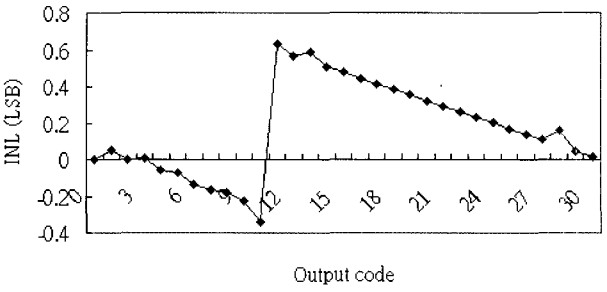
where $\tau 0$, A, ΔV, and $Vinit$ are output characteristic time constant, voltage gain, overdrive voltage, and initial output voltage difference, respectively. According to eq. (13), we can reduce the characteristic time constant and the overdrive voltage or increase the voltage gain to get smaller regeneration time. In our design, the regeneration time is only about 30ps.

5. Bubble Correction Circuit and DAC

For the sake of the measurements, the DAC is also embedded in this chip. The output thermometer codes of the comparators are corrected by the bubble correction circuit. This bubble correction circuit is realized by three input NAND gate arrays. The DAC is realized by the unity current sources. The corrected thermometer codes are used to switch the DAC and it converts the thermometer code into an analog signal.



(a) Differential nonlinearity



(b) Integrated nonlinearity

Fig. 7. DNL and INL performance.

The post-layout simulation results of the differential nonlinearity (DNL) and Integral nonlinearity (INL) are shown in Fig. 7(a) and Fig. 7(b), respectively. The simulated DNL and INL are 0.97LSB and 0.63LSB, respectively.

III. Experimental Results

The proposed ADC-DAC circuit has been fabricated in a 0.13μm 1P8M CMOS process. The die photo is shown in Fig. 8. The ADC and DAC occupy 1.08mm × 1.45mm and 0.32mm × 1.45mm, respectively. This chip dissipates 113mW with 1V supply voltage. In this chip, the ADC dissipates 102mW and the DAC dissipates 11mW.

The proposed ADC-DAC chip is measured in die-on-board assemblies. The transient response is measured by using Agilent N4901A pattern generator to generate the sampling clock. Agilent E4422B and Tektronix 694C are used to generate the analog

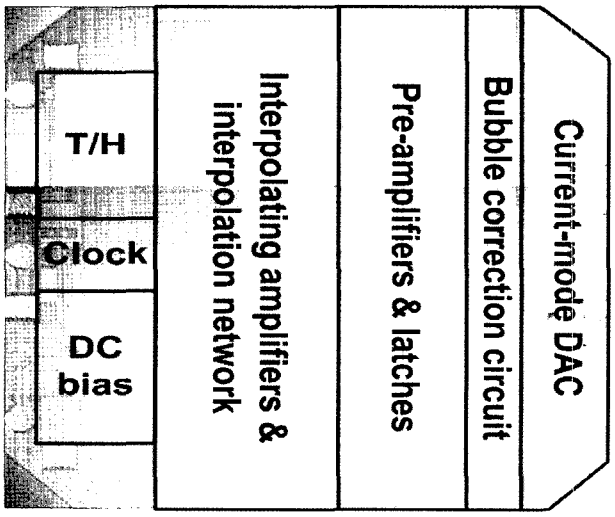


Fig. 8. Die photo.

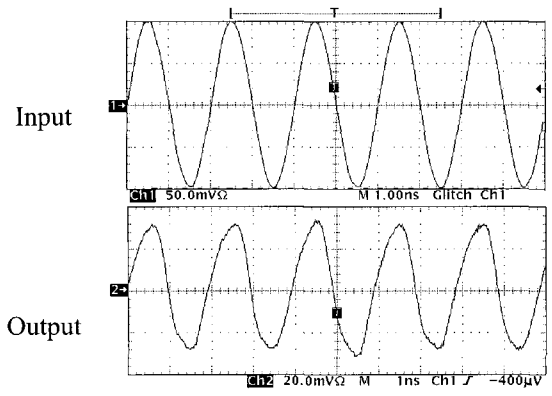


Fig. 9. Measured input and output waveforms of 500MHz.

input signal and measure the transient result, respectively. The output spectrum is measured by Agilent E4404B spectrum analyzer. The frequency of the analog sinusoidal signal is varied from 200MHz to 2.5GHz. The upper waveform in Fig. 9 gives the input of 500MHz and the lower one gives the measured output at 5GSample/sec.

Fig. 10 shows its measured spectrum. The measured spurious-free dynamic range (SFDR), signal-to-noise-distortion ratio (SNDR), second-order harmonic (HD2), and third-order harmonic (HD3) with the input frequency varied from 200MHz to 2.5GHz at 5GSample/sec is given in Fig.11. For an input signal of 200MHz, the measured SNDR at 5GSample/sec is 25.93dB and ENOB is 4.0-bit. When the input frequency is 528MHz, the measured output SNDR is 23.38dB and ENOB equals to 3.6-bit. When the input frequency arrives at Nyquist rate, the measured output SNDR is 9.62dB and ENOB reduces to 1.31-bit. The performance drops when the sampling rate closes to Nyquist rate. It is due to the bandwidth limitation in T/H circuit. In UWB receiver application, the signal bandwidth only requires

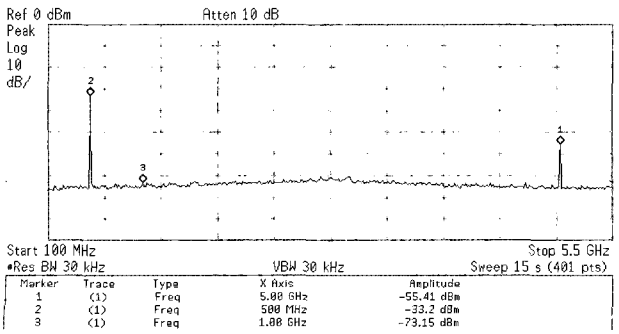


Fig. 10. Measured output spectrum.

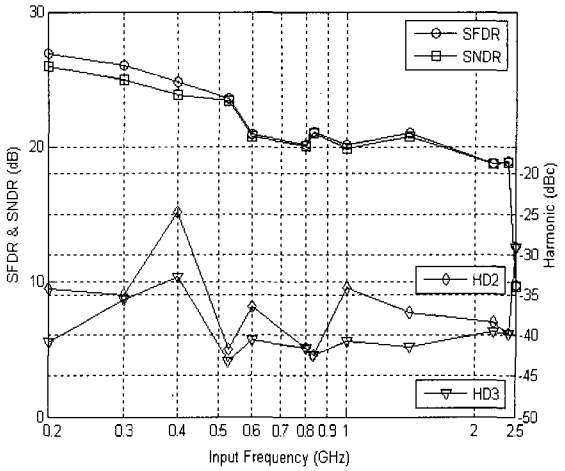


Fig.11. Measured SFDR and SNDR.

528MHz.

In our design, the T/H circuit has -3dB bandwidth about 2.7GHz. When input signal frequency is close to Nyquist rate, the signal strength is decreased so that the performance drops when the sampling rate is close to Nyquist rate. Usually, a common figure of merit (FOM) is given as follows to compare the ADC performances.

$$FOM \equiv \frac{Power}{2^{ENOB} \times F_S} \tag{14}$$

According to eq. (14), the lower FOM achieves a higher performance. A performance summary of the proposed ADC and others in literature is listed in Table 1.

Table 1. Performance Summary.

Item	[4]	[5]	[6]	[9]	This
Process	0.35μm CMOS	0.18μm CMOS	120nm SiGe	0.18μm CMOS	0.13μm CMOS
Sampling Freq.	1.3GS/s	1.6GS/s	40GS/s	4GS/s	5GS/s
SFDR	44dB	---	20dB	30dB	27dB
ENOB	5.0-bit	5.7-bit	3.0-bit	3.9-bit	4.0-bit
Supply voltage	3.3V	2.35V	---	1.8V	1V
Area (mm^2)	0.8	0.12	3.96	0.88	1.57
Power	545mW	340mW	3.8W	89mW	102mW
FOM	0.0131	0.0041	0.0119	0.0015	0.0013

IV. CONCLUSIONS

A 5-bit 5GSample/sec flash ADC has been realized in 0.13μm 1P8M CMOS technology. A linear interpolating

amplifier is proposed and analyzed. The bandwidth of the proposed ADC is extended efficiently by inversely scaling the transistor size for all cascaded stages and by using the active inductor peaking technique. This ADC-DAC chip dissipates 113mW from a single 1V supply voltage and it is suitable for UWB receiver applications.

ACKNOWLEDGMENTS

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