A Design Guide of 3-stage CMOS Operational Amplifier with Nested Gm-C Frequency Compensation

Jae-Seung Lee, Jun Hyun Bae, Ho-Young Kim, Ji-Yong Um, Jae-Yoon Sim, and Hong June Park

Abstract—**An analytic design guide was formulated for the design of 3-stage CMOS OP amp with the nested Gm-C(NGCC) frequency compensation. The proposed design guide generates straight-forwardly the design parameters such as the W/L ratio and current of each transistor from the given design specifications, such as, gain-bandwidth, phase margin, the ratio of compensation capacitance to load capacitance. The applications of this design guide to the two cases of 10pF and 100pF load capacitances, shows that the designed OP amp work with a reasonable performance in both cases, for the range of compensation capacitance from 10% to 100% of load capacitance.**

Index Terms—**Low voltage OP amp, design guide, frequency compensation, nested Gm-C**

I. INTRODUCTION

As the minimum feature size of CMOS integrated circuits has been scaled down to nano-meter regime in recent years, the power supply voltage continues to scale down. However, the threshold voltage is not scaled down proportionally to the supply voltage due to the sub-threshold leakage problem. Therefore, the design of analog circuits is becoming more difficult and challenging. The operational amplifier (OP amp), which is an important analog building block, is a good example to demonstrate the challenges in design of analog circuit with the nano-meter CMOS process [1]. Since, the conventional cascode structure of the high-gain OP amp requires multiple stacks of transistors between power supply and ground; it is difficult to design in low-voltage environment. As the solution to the design limits of cascode structure in low-voltage environment, the multistage amplifiers (cascade structure), which achieve the high gain by cascading multiple gain stages, have been researched. The multistage amplifier is more suitable to low-voltage applications, because the required number of stacks is less than cascode structure. However, since the multistage amplifier consists of multiple gain stages, it requires a complex frequency compensation scheme to ensure stability.

There are two representative frequency compensation techniques: Nested Miller Compensation (NMC) and Nested Gm-C Compensation (NGCC) [2]. Most of the frequency compensation techniques are based on two major fundamental principles: pole-splitting and pole-zero cancellation [3]. In the case of NMC, due to the stability problem caused by the positive real zero, a series resistance to the miller capacitance is used in general for CMOS OP amps[4]. The transfer function, stability, and phase margin conditions of multistage NMC amplifier are complicated to apply analytic design methodology. However, for multistage NGCC amplifier, a zero removal with feedforward path is applied, which makes the transfer function, stability, and phase margin conditions relatively simple to apply analytic design methodology.

The design guide of multistage NGCC amplifier, proposed in previous paper [1], is not a completely systematic design guide. In this paper, a systematic design guide of 3-stage NGCC amplifier, which enables

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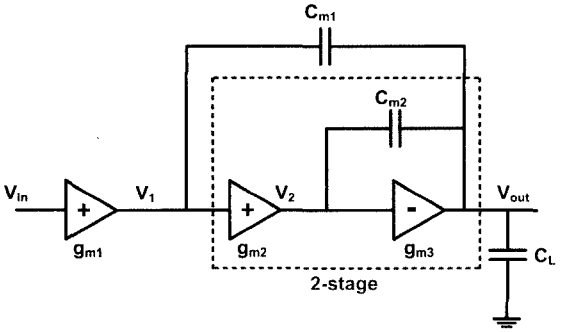
the systematic design of 3-stage NGCC amplifier with given design specifications, is proposed. The comparison between NMC with series resistance and NGCC will be presented in section II. The proposed systematic design guide of 3-stage NGCC amplifier will be described in section III. In section IV, the simulation results of 3-stage NGCC amplifier designed by the proposed design guide will be shown.

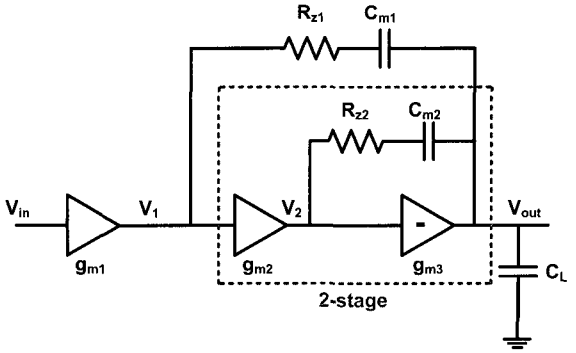
II. FREQUENCY COMPENSATION TECHNIQUES

In this section, two major frequency compensation techniques: NMC and NGCC will be briefly introduced, and also the comparison of characteristics for both techniques will be described. Fig.3 shows three frequency compensation techniques for 3-stage OP amps, where the dashed-line block represents the 2 stage OP amp version of each technique. The frequency compensation for 2-stage amplifier is performed by using a Miller capacitance. The feedforward current path through the Miller capacitance will generate the right-half-plane (RHP) zero [3], which degrades the phase margin. The RHP zero is removed by using a series resistance($R_{Z2} = 1/g_{m3}$) to the compensation capacitance, as shown in Fig. 1. (b). Also, the GmC frequency compensation technique was developed to remove the RHP zero, as shown in Fig. 1. (c), by controlling the current through the feedforward transconductance stage(g_{mf2}) to be the same as the current through the Miller capacitance ($g_{mf2} = g_{m2}$) [3].

Table.1 shows the transfer functions of both 2-stage and 3-stage amplifiers with the NMC with R_Z (Fig.1(b)) and NGCC(Fig.1(c)). The stability conditions are listed in Table. 2. Table 3 shows the 63.4° phase margin



(a)



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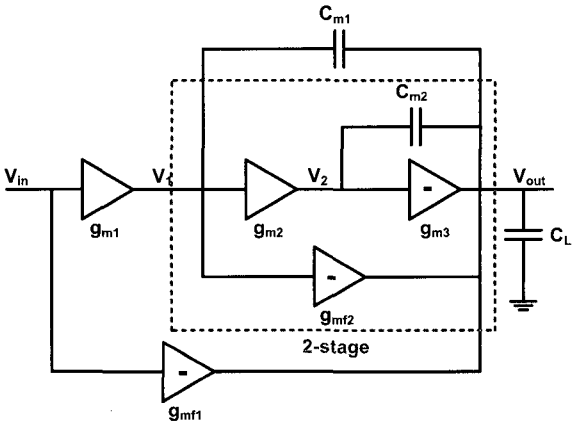

(c)

Fig. 1. 3-stage frequency compensation topologies: (a) NMC (b) NMC with series resistor (c) NGCC.

Table. 1. Transfer functions of 2-stage and 3-stage amplifiers with NMC and NGCC.

	Transfer Function
NMC with R_Z (2-stage)	$H(s) = -\dfrac{g_{m1}g_{m2}(1+s\frac{C_m}{g_{m2}})}{g_{o1}g_{o2}+sC_mg_{m2}+s^2C_m(C_L+C_m)+s^3\frac{C_m^2C_L}{g_{m2}}}$ Condition : $R_Z = \dfrac{1}{g_{m2}}$
NMC with R_Z (3-stage)	$H(s) = -\dfrac{g_{m1}g_{m2}g_{m3}+s(C_{m1}g_{m1}g_{m3}+C_{m2}g_{m1}g_{m2})}{g_{o1}g_{o2}g_{o3}+sC_{m1}g_{m2}g_{m3}+s^2C_{m1}C_{m2}(g_{m2}+g_{m3})+s^3C_{m1}C_{m2}C_L}$ Condition : $R_{z1} = \dfrac{1}{g_{m2}}$, $R_{z2} = \dfrac{1}{g_{m3}} + \dfrac{1}{g_{m2}g_{m3}R_{z1}}$
NGCC (2-stage)	$H(s) = -\dfrac{g_{m1}g_{m2}}{g_{o1}g_{o2}+sC_mg_{m2}+s^2C_LC_m}$ Condition : $g_{mf} = g_{m1}$
NGCC (3-stage)	$H(s) = -\dfrac{g_{m1}g_{m2}g_{m3}}{g_{o1}g_{o2}g_{o3}+sC_{m1}g_{m2}g_{m3}+s^2C_{m1}C_{m2}g_{m3}+s^3C_LC_{m1}C_{m2}}$ Condition : $g_{mfi} = g_{mi}\,(i=1,2)$

conditions. For the 3-stage NMC with R_Z, it is difficult to satisfy the stability condition. However, the 3-stage NGCC amplifier has a relatively simple stability

Table. 2. Stability conditions of 2-stage and 3-stage amplifiers with NMC and NGCC ($C_{m3} = C_L$).

	Stability Condition
NMC with R_Z (2-stage)	always stable
NMC with R_Z (3-stage)	$\left(\frac{1}{\omega_1}+k_1\frac{1}{\omega_2}+k_2\frac{1}{\omega_3}\right)\left(\frac{1}{\omega_2}+k_2\frac{1}{\omega_3}\right)>\frac{1}{\omega_2\omega_3}$ where $\omega_i=\frac{g_{mi}}{C_{mi}}$ $(i=1,2,3)$, $k_i=\frac{C_{mi}}{C_{m(i+1)}}$ $(i=1,2,3)$
NGCC (2-stage)	always stable
NGCC (3-stage)	$\omega_3 > \omega_1$ where $\omega_i=\frac{g_{mi}}{C_{mi}}$ $(i=1,3)$

Table. 3. Phase margin conditions (63.4°) of 2-stage and 3-stage amplifiers with NMC and NGCC.

	Phase Margin Condition (to achieve 63.4°)
NMC with R_Z (2-stage)	$C_m=\frac{2g_{m1}}{g_{m2}}C_L$
NMC with R_Z (3-stage)	too complex to calculate
NGCC (2-stage)	$C_m=\frac{2g_{m1}}{g_{m2}}C_L$
NGCC (3-stage)	$C_{m1}=k\frac{g_{m1}}{g_{m3}}C_L$, $C_{m2}=\frac{k^2}{1+2k}\frac{g_{m2}}{g_{m3}}C_L$, where $k>1$

condition($\omega_3 > \omega_1$), which can be satisfied rather easily. The feedforward transconductance of NGCC amplifier can be implemented by a single transistor, so the overhead due to the feedforward path is insignificant [1]. The 63.4° phase margin condition is very complex in the NMC with R_Z, while it is relatively simple in the NGCC. From these factors, we can see that the NGCC technique is easier to implement in 3-stage amplifiers than the NMC with R_Z.

III. Design Guide of 3-stage NGCC Amplifier

In this section, a systematic design guide is derived for the 3-stage OP amp using the NGCC frequency compensation technique. The design specifications include the gain-bandwidth product(GB), the ratio(k) of the high frequency pole(ω_3) to GB, the phase margin(PM), the output loading(C_L), and the input common-mode voltage range(ICMR).

1. Stability and Phase Margin

Assuming a dominant pole, the transfer function of 3-stage NGCC OP amp in Table 1 can be written as

$$H(s)=\frac{-A_0}{\left(1+\frac{A_0}{\omega_1}s\right)\left(1+\frac{1}{\omega_2}s+\frac{1}{\omega_2\omega_3}s^2\right)} \quad (1)$$

where A_0 is DC gain and ω_i is equal to g_{mi}/C_{mi} for i =1, 2, 3. Since ω_1/A_0 in (1) represents the dominant pole, ω_1 is the gain-bandwidth product (GB), which is equivalent to product of the DC gain and the dominant pole. The dominant pole is generated by the 1st gain stage and C_{m1}. The stability condition of 3-stage NGCC OP amp, given in Table 2, indicates that the pole(ω_3), generated by the loading capacitance (C_L) and the 3rd gain stage, should be higher than ω_1. The frequency relation based on the stability condition can be written as

$$\omega_3 = k\omega_1 \quad (2)$$

where k must be greater than 1 for stability. As indicated in (2), k represents the ratio of the highest frequency pole to GB, and it is given as the design specification.

From (1), the phase margin in the unity-gain configuration can be written as

$$PM = 90^\circ - \tan^{-1}\left(\frac{\frac{1}{\omega_2}\cdot GB}{1-\frac{1}{\omega_2\omega_3}\cdot GB^2}\right) \quad (3)$$

where GB is the gain-bandwidth product which is equal to ω_1. In order to satisfy the phase margin condition of 63.4°, the term given to $\tan^{-1}$ should be 1/2. Therefore, the resulting expression of substituting (2) to (3) can be written as

$$\omega_2 = \frac{1+2k}{k}\omega_1 \quad (4)$$

(2) and (4) indicate that the poles ω_2 and ω_3 should be higher than ω_1 to achieve both stability and the 63.4° phase margin. In general, the inequality of $\omega_1 < \omega_2 < \omega_3$ holds.

2. Transconductance of Each Stage

In previous subsections, the values of ω_1, ω_2, ω_3, which determine the transfer function of 3-stage NGCC amplifier, were calculated using the design specification of GB, stability, and phase margin. In this subsection, the value of transconductance(g_{mi}) for each stage will be calculated from ω_1, ω_2, ω_3. Since the loading capacitance(C_L) is given as a specification, g_{m3} can be calculated from ω_3 by using $\omega_3 = g_{m3}/C_L$. In order to determine the values of g_{m1} and g_{m2}, the condition of minimizing the sum of products from W/L ratio and current of 1st and 2nd stage is used as a constraint, which can be written as

$$H = \left(\frac{W}{L}\right)_1 I_{D1} + \left(\frac{W}{L}\right)_2 I_{D2} = \frac{g_{m1}^2}{2\mu_p C_{ox}} + \frac{g_{m2}^2}{2\mu_n C_{ox}} \quad (5)$$

Another constraint is required to calculate the proper values of g_{m1} and g_{m2}. Since, the sum of compensation capacitors is maintained to be less than or equal to the loading capacitance(C_L) in general, the second constraint can be written as

$$C_{m1} + C_{m2} = \alpha C_L \quad (6)$$

where α is less than or equal to 1. The value of α is given as a design specification. Using (2) and (4), (6) can be rewritten as

$$g_{m1} + \frac{k}{1+2k} g_{m2} = \frac{\alpha}{k} g_{m3} \quad (7)$$

Since the value of g_{m3} was already obtained, the values of g_{m1} and g_{m2} can be determined from (5) and (7).

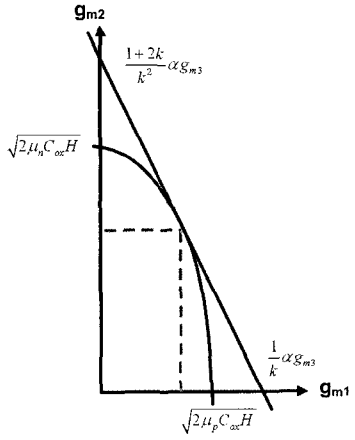

Fig. 2. The graph of two constraints((5) and (7)) to determine g_{m1} and g_{m2}.

To get the optimum values of g_{m1} and g_{m2}, which minimize the cost function of H in (5), (5) and (7) are plotted in Fig. 2, as an ellipse and a straight line, respectively

In Fig. 2, when the straight line becomes the tangential line to the ellipse, the point of tangency marked as dotted line, is the optimum values of g_{m1} and g_{m2} that minimize the cost function H, which can be written as

$$g_{m1} = \frac{\alpha(1+2k)^2}{k\left(\frac{\mu_n}{\mu_p}k^2 + (1+2k)^2\right)} g_{m3} \quad (8.a)$$

$$g_{m2} = \frac{\alpha(1+2k)}{k^2 + \frac{\mu_p}{\mu_n}(1+2k)^2} g_{m3} \quad (8.b)$$

3. Current and W/L Ratio of Each Stage

In order to calculate the current and W/L ratio of each stage from the transconductance(g_{mi}) values acquired from previous subsection, the V_{DSAT} values of transistors are determined from the specification of the input common-mode voltage range(ICMR). The W/L ratios of input transistors in the 1st gain stage should be large enough to enhance the equivalent input noise voltage. Thus, V_{DSAT} values of the input transistors in the 1st gain stage were set to half of the V_{DSAT} values of the transistors, composing the active load of input

differential pair and current sources. Besides, the V_{DSAT} values of all the gain-path transistors($g_{mi}, i=1,2,3$) are set to be the same as V_{DSAT} of the input transistor of 1st gain stage. Then, the ICMR of PMOS differential pair with NMOS active load is given by

$$ICMR = V_{DD} - 5V_{DSAT} - V_{TH} \tag{9}$$

where V_{DSAT} is the V_{DSAT} value of the input transistor in the 1st gain stage. The circuit schematic of OP amp is shown in Fig.5. To guarantee that the ICMR is greater than 1/3 of supply voltage, the following condition should be satisfied.

$$V_{DSAT} \le \frac{1}{5}\left(\frac{2}{3}V_{DD} - V_{TH}\right) \tag{10}$$

The drain current and W/L of each transistor can be calculated from $I_{D.j} = 0.5\, g_{m.j}\, V_{DSAT.j}$ and $(W/L)_j = 2\, I_{D.j} / (\mu C_{ox} \cdot V_{DSAT.j}^2)$.

4. Compensation Capacitor

Using (2) and (4), the compensation capacitances can be derived from

$$C_{m1} = k\frac{g_{m1}}{g_{m3}}C_L \tag{11.a}$$

$$C_{m2} = \frac{k^2}{1+2k}\frac{g_{m2}}{g_{m3}}C_L \tag{11.b}$$

5. Summary of the Proposed Design Guide

In Table. 4, the proposed design guide is summarized and the calculated values of parameters with a given specification are presented as a design example.

IV. Simulation Results

The NGCC 3-stage amplifier shown in Fig. 3 was designed using a 0.18μm CMOS process. Power supply voltage was set to 1.2V. The design specification was as follows ; k = 4, GB=10MHz, PM=63.4°, ICMR= 0.4V, and C_L=①10pF, ②100pF. The gate lengths of all MOSFETs were set to 0.5um, about 3 times the minimum feature size. Fig. 4 shows the simulated frequency response when the value of C_L and α were set to 10pF and 0.3, respectively. The unity gain bandwidth, the phase margin, and the settling time of the designed NGCC 3-stage amplifier were 10MHz, 59°, and 120nsec, respectively. Fig. 5 shows the simulated step responses for the two cases of load capacitances (C_L=10pF, C_L=100pF) when α was set to 0.3.

Table 5 shows the performance comparison of the designed OP amp for different values of α with 10pF

Table. 4. The summary of the proposed design guide.

Step	Equations	Example GB = 10MHz, k=4, PM=63.4°, C_L=10pF, ICMR≥VDD/3, α=0.3
Determine ω_1 from GB.	$\omega_1 = 2\pi \times GB$	$\omega_1 = 2\pi \times 10 Mrad/\sec$
Calculate ω_2 and ω_3.	$\omega_2 = \frac{1+2k}{k}\omega_1$, $\omega_3 = k\omega_1$	$\omega_2 = 2\pi \times 22.5 Mrad/\sec$ $\omega_3 = 2\pi \times 40 Mrad/\sec$
Calculate g_{m3}.	$g_{m3} = \omega_3 \cdot C_L$	$g_{m3} = 2.5mS$
Calculate g_{m1} and g_{m2}.	$g_{m1} = \frac{\alpha(1+2k)^2}{k\left(\frac{\mu_n}{\mu_p}k^2 + (1+2k)^2\right)} g_{m3}$ $g_{m2} = \frac{\alpha(1+2k)}{k^2 + \frac{\mu_p}{\mu_n}(1+2k)^2} g_{m3}$	$g_{m1} = 0.105mS$ $g_{m2} = 0.186mS$
Determine V_{DSAT}.	$V_{DSAT} \le \frac{1}{5}\left(\frac{2}{3}V_{DD} - V_{TH}\right)$	$V_{DSAT} = 80mV$
Calculate I_{Di}.	$I_{Di} = \frac{g_{mi} \cdot V_{DSAT}}{2}$ $(i=1,2,3)$	$I_{D1} = 4.2\mu A$ $I_{D2} = 7.4\mu A$ $I_{D3} = 100\mu A$
Calculate $\left(\frac{W}{L}\right)_i$.	$\left(\frac{W}{L}\right)_i = \frac{g_{mi}^2}{2\mu\, C_{ox} I_{Di}}$ $(i=1,2,3)$	$(W/L)_1 = 20$ $(W/L)_2 = 8$ $(W/L)_3 = 105$
Calculate C_{m1} and C_{m2}.	$C_{m1} = k\frac{g_{m1}}{g_{m3}}C_L$ $C_{m2} = \frac{k^2}{1+2k}\frac{g_{m2}}{g_{m3}}C_L$	$C_{m1} = 1.68pF$ $C_{m2} = 1.32pF$

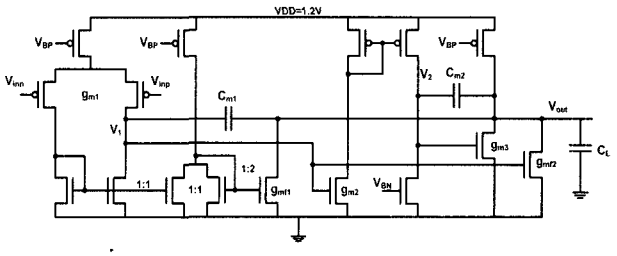

Fig. 3. Circuit diagram of 3-stage NGCC amplifier.

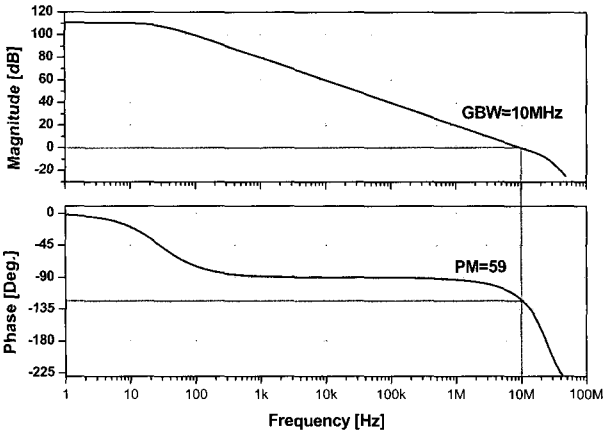

Fig. 4. Simulated frequency response (CL=10pF and $\alpha = 0.3$).

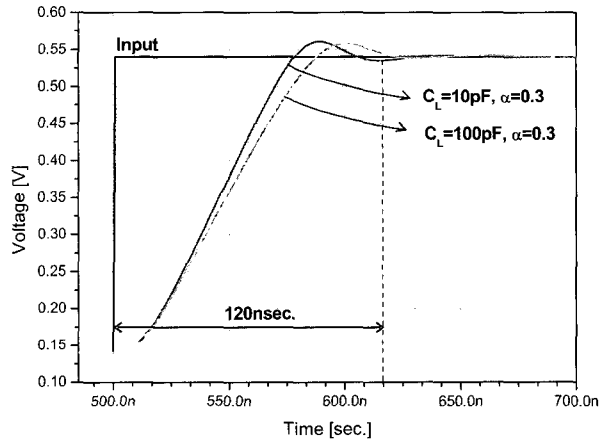

Fig. 5. Simulated step response (CL=10pF, CL=100pF and $\alpha = 0.3$).

C_L. Table. 6 shows the same comparison with 100pF C_L. When the value of α is much less than 1, the effect of parasitic capacitance becomes significant and it degrades the phase margin and increases the settling time. If the value of α is large close to 1, the W/L value of MOSFET in each gain stage will be larger as the values of g_{m1} and g_{m2} increase. In addition, power consumption increases, as the amount of current required for each gain stage increases, and the chip area will be larger due to the larger compensation capacitors. Therefore, in the design process of the OP amp, α should be determined carefully to optimize the design.

V. CONCLUSIONS

In this paper, an analytic design guide of 3-stage NGCC OP amp for low-voltage application was proposed. The proposed design guide generates straight-forwardly the design parameters such as W/L ratio and current of each transistor, with the given OP amp design specification of gain-bandwidth(GB), the ratio of the highest frequency pole to GB, phase margin(PM), output loading(C_L), and input common-mode range(ICMR), and the ratio of compensation capacitors(α) to the load capacitor. A 3-stage NGCC OP amp was designed by using the proposed design guide. A 0.18μm CMOS process with 1.2V supply voltage was used in the design. The performance variation of the OP amps, depending on the ratio of compensation capacitors(α) to the load capacitor, was observed. It was shown that the designed OP amp work with a reasonable performance for the range of α from 0.1 to 1.0. When the output loading is 10pF and α is 0.3, the designed OP amp gave 111dB DC gain, 10MHz gain-bandwidth, 59° phase margin, and 120nsec settling time.

Table. 5. Summary of simulation results(C_L=10pF).

Specifications: C_L=10pF, k=4, GBW=10MHz, PM=63.4°, ICMR= 0.4V				
α	0.1	0.3	0.5	1
DC gain [dB]	113	111	109	107
Phase margin [Deg.]	53	59	59	60
GBW [MHz]	10.4	10	9.85	9.8
1% settling time [nsec]	165	120	102	100
Power [uW]	242	297	368	517
g_{m1} [mS] (C/S)*	0.035/0.031	0.105/0.1	0.176/0.16	0.351/0.33
g_{m2} [mS] (C/S)*	0.062/0.58	0.187/0.175	0.312/0.3	0.624/0.59
g_{m3} [mS] (C/S)*	2.5/2.3	2.5/2.3	2.5/2.3	2.5/2.3
C_{m1} [pF]	0.559	1.676	2.793	5.586
C_{m2} [pF]	0.441	1.324	2.207	4.414
sum(W x L) [um^2]	218	255	282	376

*C : calculation, S:simulation

Table. 6. Summary of simulation results (C_L=100pF).

Specifications: C_L=100pF, k=4, GBW=10MHz, PM=63.4°, ICMR= 0.4V				
α	0.1	0.3	0.5	1
DC gain [dB]	111	110	106	108
Phase margin [Deg.]	56	60	62	60
GBW [MHz]	9.9	9.27	8.64	9.8
1% settling time [nsec]	165	117	147	131
Power [uW]	2024	2490	5380	4800
g_{m1} [mS] (C/S)*	0.35/0.36	1.1/0.9	1.8/1.65	3.5/3.2
g_{m2} [mS] (C/S)*	0.62/0.57	1.8/1.6	3.1/2.7	6.2/6
g_{m3} [mS] (C/S)*	25.1/24	25.1/24	25.1/24	25.1/24
C_{m1} [pF]	5.586	16.759	27.931	55.862
C_{m2} [pF]	4.414	13.241	22.069	44.138
sum (W x L) [um^2]	1245	1694	1361	3438

*C : calculation, S:simulation

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