Circuit Design of DRAM for Mobile Generation

Jae-Yoon Sim

Abstract—**In recent few years, low-power electronics has been a leading drive for technology developments nourished by rapidly growing market share. Mobile DRAM, as a fundamental block of hand-held devices, is now becoming a product developed by limitless competition. To support application specific mobile features, various new power-reduction schemes have been proposed and adopted by standardization. Tightened power budget in battery-operated systems makes conventional schemes not acceptable and increases difficulty of the circuit design. The mobile DRAM has successfully moved down to 1.5V era, and now it is about to move to 1.2V. Further voltage scaling, however, presents critical problems which must be overcome. This paper reviews critical issues in mobile DRAM design and various circuit schemes to solve the problems. Focused on analog circuits, bit-line sensing, IO line sensing, refresh-related schemes, DC bias generation, and schemes for higher data rate are covered.**

Index Terms—**Low-power DRAM, refresh, tempera ture sensor, sense amplifier**

I. INTRODUCTION

Rapid increase in market share by mobile devices such as 3G/4G and WCDMA phones, and various hand-held personal electronic devices has driven low-power trend of individual system components. Tightened power and thermal budgets in battery-operated systems have increased the importance of the low-power, and now it is becoming no less than that of the speed performance.

As a fundamental block of a system, memory should support various power-reduction plots of mobile system designers. Application-specific low-power DRAM with current-saving features is one that has been a most dramatically improved memory by taking challenges seeking new enabling circuit schemes. The low-power DRAM, or mobile DRAM, has successfully moved down to 1.5V era, and now it is about to move to 1.2V. Further voltage scaling, however, presents critical problems which must be overcome.

Fig. 1 illustrates limitation factors in low-voltage and low-power DRAM design. In a low-voltage DRAM, performance degradation is mainly caused by the small current driving capability of the cell access transistor. Since threshold voltage of the cell access transistor cannot be scaled with the operating voltage due to the subthreshold leakage constraints, an efficient pumping scheme to generate higher Vpp with low supply voltage is essential.

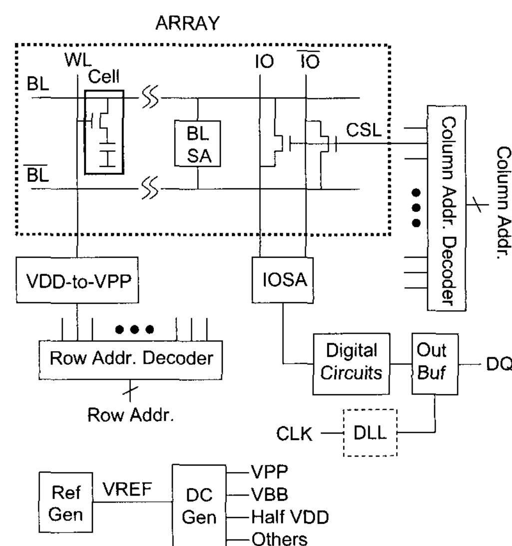


Fig. 1. Primary blocks of DRAM.

Manuscript received Sep. 10, 2006; revised Feb. 2, 2007.
Dept. EE, Pohang University of Science and Technology, Pohang, Korea.
E-mail : jysim@postech.ac.kr

While the number of pumping stages can be increased to generate sufficiently high Vpp, repetitive charge transfers between stages result in degradation of pumping efficiency[1]-[5]. As the target Vpp increases, the efficiency of the pump is significantly reduced due to the large portion of the current consumed at the charge transferring phase compared with the pumping phase.

To convert the bit-line data to a CMOS level, voltage-mode or current-mode sensing can be used for the IO line sense amplifier(IOSA)[4]-[9]. Due to the small current driving capability of the bit-line sense amplifier(BLSA), operation speed of IOSA has been a bottleneck limiting READ performance. Since IOSA consumes more than 30% of the total operating current, its design optimization is important in reduction of power consumption.

One of the most important criteria especially in mobile DRAM is the small data retention current in power-down modes because the power consumption in the self-refresh mode mainly determines the battery lifetime. To reduce power consumption in the self-refresh mode, various circuit schemes have been proposed. They are temperature-compensated self-refresh(TCSR)[4][10], partial-array self-refresh(PASR), negative word-line(NWL)[11]-[14], and the use of error-correction code(ECC).

Generation of DC bias with low supply voltage also presents difficult challenges. Since bias generation is performed by analog circuits, voltage down-scaling is limited. In addition, as threshold voltage decreases, large variability of device parameters causes increase of percent error in bias voltages.

As mobile DRAM is about to adopt DDR2, DDR3 and complicated I/O protocols to support higher data rate, use of DLL and parallel termination schemes should be considered to meet tightened timing constraints at the cost of current consumption in active operation mode. Since parallel termination is serious burden in terms of power management, the intra-chip communicating multi-chip packaging without termination has been also sought to achieve better signal integrity as well as one-chip integration of a system.

This paper reviews critical issues in mobile DRAM design and various circuit schemes to solve the problems. Section II introduces issues in low-voltage bit-line sensing. IO line sensing schemes are followed in Section III. Refresh characteristics and various current saving features in self-refresh mode are described in Section IV. Section V describes some critical bias generation circuits in low-voltage operation. Schemes for higher data rate are briefly described in Section VI, and Section VII concludes this paper.

II. BIT-LINE SENSING

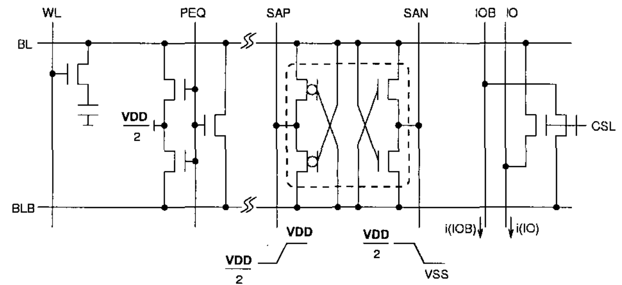


Fig. 2. Bit-line sensing circuit.

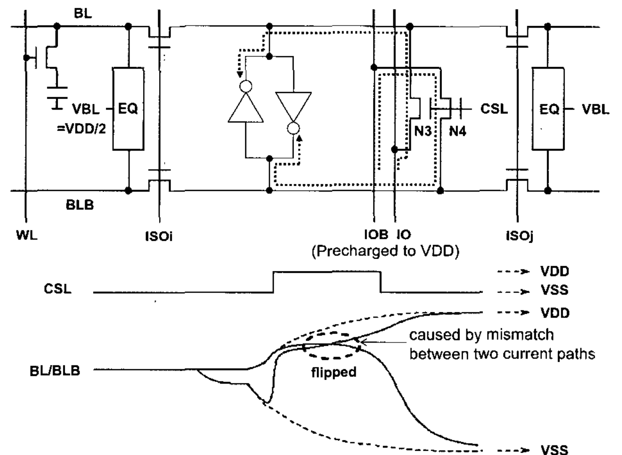


Fig. 3. Circuit and timing diagram of how BL flipping error is caused by mismatches in BL-to-IO line paths.

Fig. 2 shows BL sensing circuits. SAP and SAN are sensing enable signals and precharged to half-VDD in BL-precharge phase. During the sensing phase, SAP and SAN provide power for the BL development.

Fig. 3 shows BL flipping error[14] affected by VDD-precharged IO lines. This BL flipping error occurs when CSL gates open too fast after the sensing start under the circumstances of process/design-induced skews, such as mismatch in threshold voltages of N3 and N4, or difference in resistance between BL-to-IO and BLB-to-IOB paths. To be free from the BL flipping, CSL turn-on

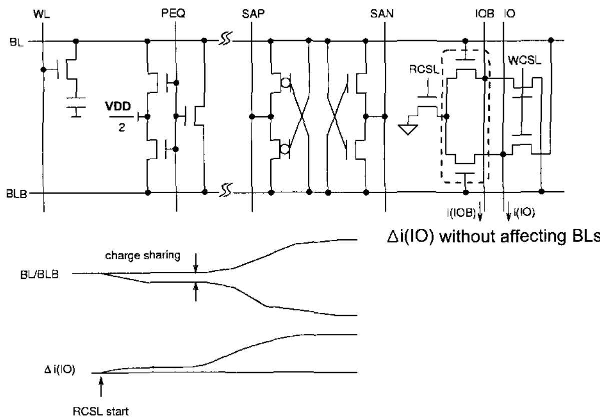


Fig. 4. Circuit and timing diagram of direct BL sensing.

time should be delayed until BL/BLB development becomes sufficiently large. This performance degradation is aggravated at low voltage due to the reduced driving strength of the BL sense amplifier.

Direct current sensing scheme improves the sensing performance by using an NMOS differential pair to generate the differential current output without affecting BLs[15]-[18]. Fig. 4 shows a circuit schematic of a direct sensing scheme. RCSL and WCSL represent CSL signals for READ and WRITE operations, respectively. Since BLs are not hurt by IO lines, CSL gates can be enabled even at the start of the charge sharing phase to improve the minimum RAS-to-CAS delay performance. But low voltage sensing operation may require multi-stage amplification even in the direct sensing[18] due to the reduced current output, Δi(IO).

III. IO LINE SENSING

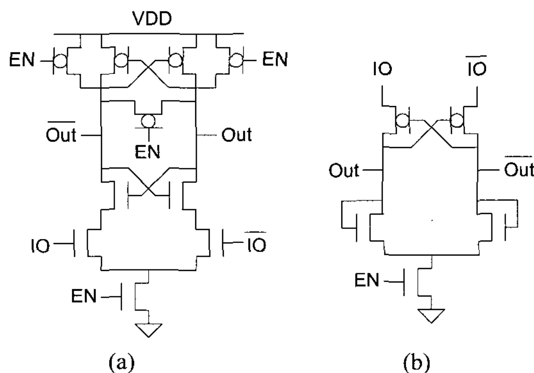


Fig. 5. First stage of voltage-mode(a) and current-mode(b) IOSA.

Fig. 5 shows the first stage of the IO line sensing. The voltage-mode SA forms a regenerative latch when EN goes high, so it shows a best speed performance to get the sensed result. In burst-mode operation, however, the polarity of IO lines should be changed in very short period of time since different CSL lines open at every clock cycles. In this case, fast IO line precharge to VDD level between every clock cycles is more important than the sensing speed itself because it determines the maximum operating frequency, i.e. the throughput performance.

Current-mode SA(CSA)[4]-[9] has been used for IOSA due to its inherent precharging feature. Fast operation can be achieved by sensing the long and capacitive IO lines with very small voltage swing around the precharged level. Fig. 6 shows the principle of the current sensing. Load transistor acts as a moderate voltage source and a current source at the same time with finite source resistance, so it provides both the V-I conversion and precharging of IO lines. The input resistance of the CSA shown in Fig. 5(b) is given by

$$\frac{gm_N - gm_P}{gm_N \cdot gm_P}$$

where gm_N and gm_P represent transconductance of NMOS and PMOS, respectively. As the input resistance approaches to zero, the differential current input is maximally accepted, but the input resistance should be greater than zero to guarantee stability. So optimization is required so that gm_N should be slightly larger than gm_P at any skew condition. With IO lines precharged to almost VDD level, the simple four-transistor structure of CSA successfully achieves both the high-speed and low-power performance, but the series-stacked structure apparently limits the low-voltage margin.

For low-voltage operation, Fig. 7 shows a hybrid N/P-folded CSA[4] which additionally uses pull-up PMOS diodes and pull-down current sources. When the supply voltage is larger than |Vtp|+Vtn, NMOS diodes become dominant and the hybrid CSA is similar to Fig.5(b). As the supply voltage decreases, the folded structure becomes dominant, improving the low-voltage margin.

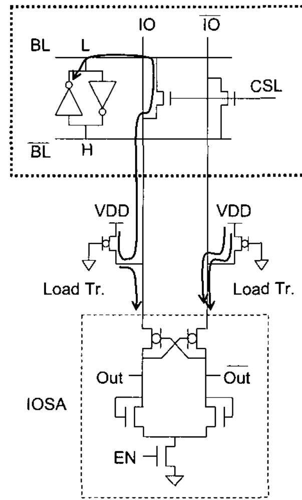


Fig. 6. Current-mode IO line sensing.

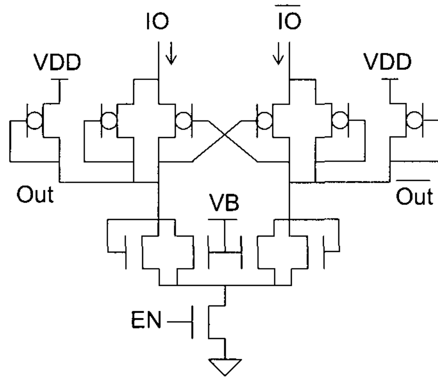


Fig. 7. Hybrid N/P folded CSA[4].

IV. REFRESH CHARACTERISTICS

1. Cell Leakage

The key to success in the scaling-down of process technology is to maintain retention characteristics. As supply voltage or channel length decreases, retention time also decreases. Fig. 8 shows two major leakage paths from the cell. Depending on the operation modes, two different refresh characteristics are concerned. In active mode, BL is developed by BLSA, and the transistor sees the lowest |Vgs|, i.e. 0V, when BL is at 'low' state. In this case, the channel leakage is dominant. To improve the dynamic refresh, Vth should be raised for the better cut-off characteristics. But it is not acceptable due to the degradation of the static refresh characteristics and difficulty in high VPP generation.

Static refresh is governed by the junction leakage. In

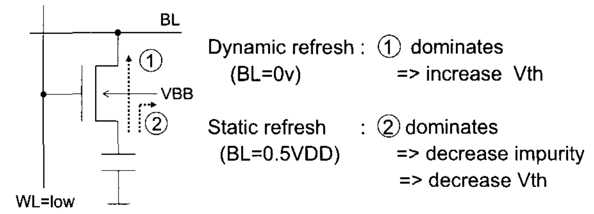
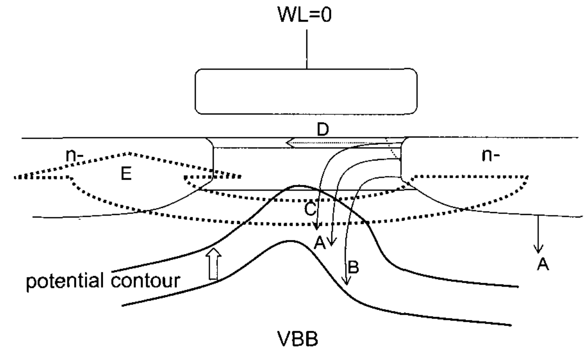


Fig. 8. Leakage paths affecting refresh characteristics.



A : Junction Leakage
B : "Gate Induced" Junction Leakage
C : Gate Induced Drain Leakage
D : Surface Punch-Through
E : Bulk Punch-Through

Fig. 9. Leakage sources in negative WL scheme.

stand-by mode, BL is precharged to half-VDD. Then channel leakage becomes negligible since the transistor sees negative Vgs. In this case, junction leakage dominates. To reduce the junction leakage, impurity dose should be decreased, meaning decrease of Vth. But sufficient reduction of Vth is not acceptable since it degrades the dynamic refresh characteristics.

To reduce both leakage sources, negative word-line schemes[11]-[14] have been proposed. By precharging WL to a negative potential, channel leakage can be greatly reduced. So Vth can be lowered by decreasing the impurity level. Even though the negative WL gives an alternative circuit-based solution to the refresh problem, it should overcome some outstanding factors which would not be critical in the grounded WL scheme. Fig. 9 shows leakage sources in the negative WL scheme. By the reduction of impurity level, the junction leakage, A, can be reduced. However, the negative potential contour shifts toward the channel region, resulting in increase of electric field at the drain junction. So B, C, and D increase undermining improvements by the use of the negative WL.

2. Temperature Compensated Self Refresh

Since the retention time of DRAM cells is strongly dependent on the temperature as shown in Fig. 10, a temperature sensor can be used to control the refresh period to profile the data retaining activities that are just needed for the ambient condition[4][19][20].

Most of temperature sensing schemes are based on band-gap reference(BGR) circuit[4][19]-[20] since BGR generates quite linear quantities with respect to the temperature. Fig. 11 shows a conceptual illustration of how temperature is sensed. All the BGR circuits have two fundamental branches, one is the series connection of a resistor and a p-n diode and the other is a diode only. Addition of a bias circuit which supplies the same current to both branches with keeping the two node voltages(V1 and V2) to be the same forms a BGR circuit. Then the current is proportional to the absolute temperature(PTAT) and the voltage is inversely proportional to the absolute temperature(IPTAT). By appropriate transformation to the same quantity, i.e. V or I, a comparison scheme can be achieved.

The temperature sensor, however, significantly suffers from process variations due to the small temperature coefficient. Hence, chip-by-chip testing and trimming are inevitable. This difficulty resulting in long test time for the temperature sensor should be solved by an efficient test scheme[4][21].

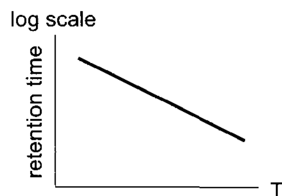


Fig. 10. Temperature dependency of retention time.

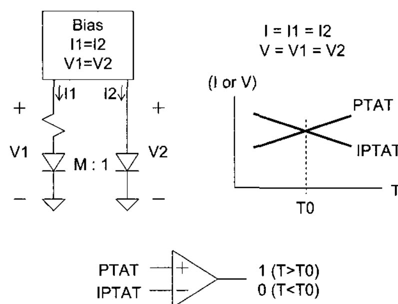


Fig. 11. Principle of BGR-based temperature sensor.

3. Partial Array Self Refresh

Partial array self-refresh(PASR) scheme is yet another mobile specific feature for the futher reduction of the self-refresh current. If the size of the data to be stored in power-down mode is not large, system collects the data and stores in a pre-defined small memory space before the entering into self-refresh mode. Then, DRAM periodically refreshes the cells only in the pre-defined block. The array size can be chosen to be 1/2, 1/4, 1/8, or 1/16 of the total array by an external control. With PASR, the self-refresh current can be greatly reduced to less than 100μA including minimal current to maintain DC bias voltages.

4. Error Correction Code

Recently, encoding approches have been actively researched for the reduction of self-refresh current at the cost of area overhead. Based on the hamming code, 1-bit error can be corrected by adding 4 parity bits to the maximum of 11-bit data. Due to the preference of byte operation, 4 parity bits are inserted to every 8-bit data when it is to be stoared. With the error correction scheme, defect bits limiting the retention time and soft errors can be corrected. Thus the self-refresh period can be dramatically increased, hence the reduction of self-refresh current. Total area overhead is around 30 percent due to the extra 50 percent increase of cell arrays for the parity bits.

V. DC GENERATION

Since DC bias circuits are analog, the generation of some DC bias voltages with low supply voltage is becoming a most difficult task limiting further voltage down-scaling. Among them, issues arising from critical DC circuits such as VPP, VREF, and initializing pulse generator during power-up are introduced in this Section.

1. VPP

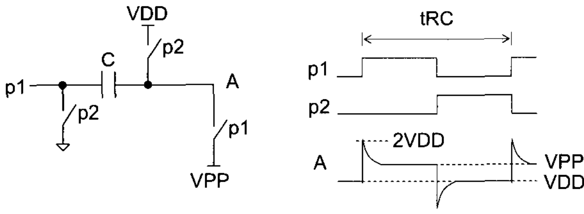


Fig. 12. Single stage pumping (VPP ~ 1.5VDD).

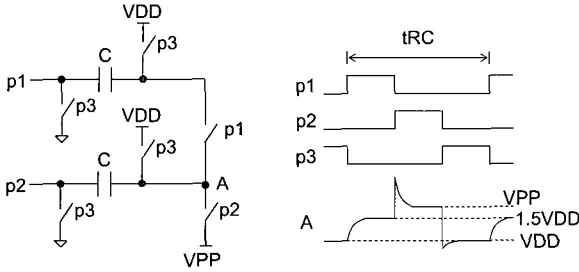


Fig. 13. Double pumping (VPP < 2VDD).

Fig. 12 shows a general single-stage charge pumping scheme with two phases, pumping(p1) and precharge(p2). tRC represents the row cycle time which corresponds to one cycle time of the word-line activation and precharge. Since the maximum boosted voltage on the node A is limited to 2VDD, this scheme is used when VPP target is upto around 1.5VDD to make sure reasonable driving capability.

For higher voltage generation, multi-stage pumping schemes should be used. Fig. 13 shows a double pumping which boosts the node A to 2.5VDD. This double pumping scheme can be used when the target VPP is less than 2VDD. One tRC is divided into 3 phases and the time for the charge transfers is reduced by 33-percent compared with the case of the simple 2-phase pumping shown in Fig. 12. So careful optimization of capacitance and transistor size is required for the sufficient charge sharing.

Since typical VPP target of mobile DRAM is larger than 2VDD, more complicated pumping scheme is needed. Fig. 14, Fig. 15 and Fig. 16 show pumping schemes which boost the node A to 3VDD. As an extended version from the double puming shown in Fig. 13, a simple triple pumping scheme can be achieved as shown in Fig. 14. This triple pumping, however, further reduces timing margin because the fixed tRC should be shared by four phases. Furthermore, if the VPP target is larger than 2VDD, the remain charge at node A after p3 is wasted since the node A is to be precharged to VDD level in p4, the precharge phase. This degrades the pumping efficiency resulting in larger current consumption.

Fig. 15 shows a hidden precharged triple pumping scheme which has only three phases[5]. Upper three capacitors are precharged during the charge transferring phase, p2, while the node A remains unprecharged. This also eliminates the degradation of the pumping efficiency as shown in Fig 14.

As an alternative, Fig. 16 shows a double boosing pump[4]. After the two capacitors are precharged in parallel during p1 phase, they are connected in series during the pumping phase, p2. Then the node A is abruptly boosted from VDD to 3VDD without current consumption. The stored charge at the node A is then transferred to VPP during p2. Since there is only two phases, timing constraints are greatly released. Effective capacitance in the pumping phase, however, is reduced by half due to the series connection.

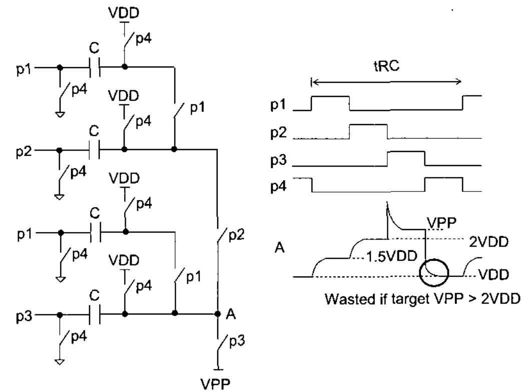


Fig. 14. Triple pumping (VPP > 2VDD).

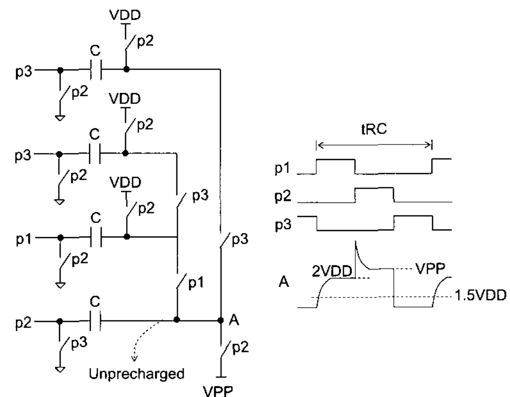


Fig. 15. Triple pumping with hidden precharge (VPP > 2VDD).

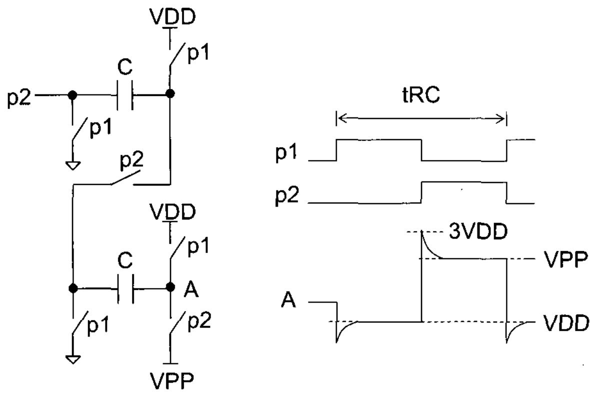


Fig. 16. Double boosting pump (VPP > 2VDD).

2. Reference Generation

DC bias voltages are generated by proportional relations to a fixed reference voltage, and the reference voltage should be process/supply/temperature(PVT) insensitive. As shown in Fig. 17, the temperature dependency can be eliminated by the summation of a proportional and an inversely proportional terms using a BGR circuit. Since the BGR refers p-n junction diodes, the generated reference voltage is always around the silicon bandgap voltage(~1.15V) if it is optimized to be PVT-insensitive. The BGR is free from process and supply variation since the bandgap voltage is fixed and does not change. However, the BGR circuit fails to generate an appropriate reference voltage in sub-1V DRAM, so the reference generation is seriously problematic in design of low-voltage DRAM.

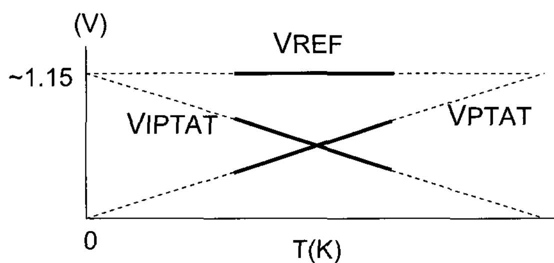


Fig. 17. BGR-based reference generation.

Fig. 18 shows a CMOS VREF circuit to generate lower reference voltage than BGR. M1 has large W/L ratio to make sure that M1 should operate in weak inversion region while other transistors operate in strong inversion region. Since v1 and v2 have opposite gradient with respect to the temperature variation, the temperature dependency can be cancelled out.

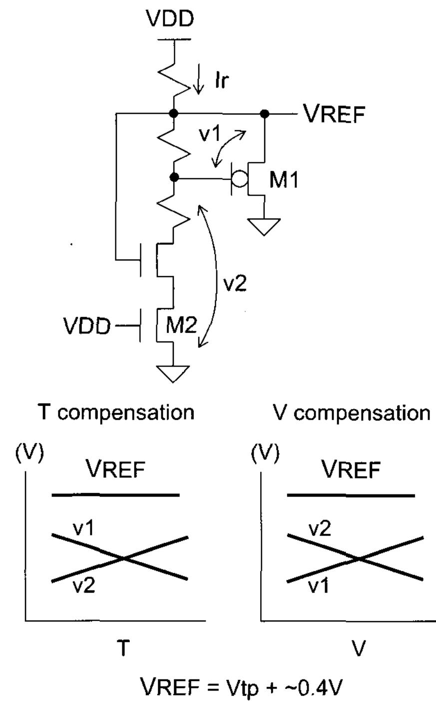


Fig. 18. CMOS VREF.

To eliminate the supply dependency, M2 operates as a variable resistor. For example, as VDD increases, Ir increases linearly. Since most of the increased current flows through M1, v1 slightly increases. But v2 decreases by the reduction of the turn-on resistance of M2 as VDD increases. Optimal VREF is around Vtp + ~0.4V. The 0.4V serves as a buffer voltage to compensate for the v1 change. Though CMOS VREF circuit can be used for the lower reference generation than BGR, VREF is subject to process variation. So a die-to-die post-fabrication trimming is required.

3. Initialization During Power-Up

During power-up, internal nodes of some latches should be initialized appropriately before the start of the normal operation. A power-up pulse generator is used for this purpose. Fig. 19 shows a widely used power-up pulse generator with a setup voltage(Vset) of 2Vtn. Assume that VDD increases from zero during the power-up phase. When VDD reaches the threshold voltage of P0, Vset goes low. The low state of Vset enables current paths initializing internal nodes of latches. The low state lasts until VDD crosses 2Vtn. When VDD is higher than

Fig. 19. Power-up pulse generator.

2Vtn, Vset goes high turning off all the initializing current paths to prepare for the normal operation. Since the temperature variation of the setup voltage, 2Vtn, is about 0.4V over the temperature range of 100°C, the initialization during power-up is yet another critical problem in sub-1.0V DRAM.

VI. HIGH-SPEED INTERFACE

Performance of a system is determined by the data rate of inter-chip communication as well as the on-chip operating speed. To achieve higher throughput in DRAM operation, expansion of the organization from x16 to x32 can be considered to alleviate circuit complexity and tightened timing constraints. The increase in parallelism, however, presents serious simultaneous switching noise on the internal power lines for the output drivers.

Mobile DRAM is about to support DDR2 and DDR3 I/O features for higher data rate. With minimizing extra power consumption, the use of DLL and termination schemes should be considered to meet tightened timing constraints.

1. Termination

Fig. 20 shows three voltage-mode termination schemes. Fig. 20(a) is a series termination with source resistance matched to the characteristic impedance of the transmission line. A series connection of the turn-on resistance of pull-up/pull-down MOS and a resistor is used to improve linearity. Since the series termination does not consume static current, it has been widely

Fig. 20. Voltage-mode termination schemes.

adopted in mobile DRAM for the data rate of less than 1 Gps. This scheme gives an additional advantage that a simple inverter can be used for the input buffer.

To achieve the data rate of giga-bps, parallel termination schemes have been considered to improve signal integrity. Fig. 20(b) shows a typically used voltage-mode parallel termination. The voltage swing on transmission line is reduced by half with the static current consumption of (3VDDQ)/(8Ro) regardless of data pattern.

Shown in Fig. 20(c) is the pseudo open-drain scheme to achieve lower power as well as the parallel termination. Since this structure is basically a parallel termination, voltage swing on transmission line is half of VDDQ. But driving current flows only when data is driven low. Average current of 33-percent can be reduced compared with the conventional parallel termination shown in Fig. 20(b). So the pseudo open-

drain scheme is being considered positively as an optimal solution to achieve the better signal integrity with lower power consumption.

2. Fast-Locking Low-Power DLL

Until now DLL has not been used in mobile DRAM due to the power consumption and complicated operation modes which should be supported for the mobile features. As the data rate increases, the use of an output DLL is expected to be essential to meet tightened timing specification. Since the mobile DRAM has various power-down modes, DLL should be switched off in power-down mode and a fast-locking is required when DRAM is switched to active operationg mode. Thus, in order to use a DLL, a digitally controlled fast-locking scheme should be implemented as well as low-power.

VII. CONCLUSIONS

In this paper, critical issues and various circuit schemes suitable for the design of mobile DRAM are discussed with focused on analog circuits such as bit-line sensing, IO line sensing, refresh-related schemes, DC bias generation, and high-speed interface schemes. Since performance degradation is mainly caused by the small current driving capability of the cell access transistor, an efficient multi-stage pumping scheme to generate higher Vpp with low supply voltage is essential. For the sensing schemes to convert the bit-line data to a CMOS level, issues arising in the low-voltage BLSA and IOSA are discussed. To reduce a most important criteria in mobile DRAM, the self-refresh current, temperature-compensated self-refresh, partial-array self-refresh, negative word-line, and the use of error-correction code(ECC) have been proposed. For the high-speed off-chip interface, the use of the fast-locking DLL and parallel termination schemes is being considered to meet tightened timing constraints.

REFERENCES

[1] C. Lauterback, W. Weber, and D. Romer, "Charge-sharing concept and new clocking scheme for power efficiency and electromagnetic emission improvement of boosted charge pumps," *IEEE J. Solid State Circuits,* vol.35, pp.719-723, May. 2000.

[2] T. Tanzawa and S. Atsumi, "Optimization of word-line booster circuits for low-voltage flash memories, " *IEEE J. Solid State Circuits,* vol.34, pp.1091-1098, Aug. 1999.

[3] T. Hamamoto, Y. Morooka, T. Amano, and H. Ozaki, "An efficient charge recycle and transfer pump circuit for low operating voltage DRAMs, " *Symposium on VLSI Circuits,* pp.110-111, 1996.

[4] J. Y. Sim, H. Yoon, K. C. Chun, H. S. Lee, S. P. Hong, S. Y. Kim, M. S. Kim, K. C. Lee, J. H. Yoo, D. I. Seo, and S. I. Cho, "Double boosting pump, hybrid current sense amplifier, and binary weighted temperature sensor adjustment schemes for 1.8V 128Mb mobile DRAMs, " *Symposium on VLSI Circuits*, pp.294-297, 2002.

[5] K. C. Chun, J. Y. Sim, H. Yoon, H. S. Lee, S. P. Hong, K. C. Lee, J. H. Yoo, and D. I. Seo, "A 1.8V 128 Mb mobile DRAM with hidden-precharged triple pumping scheme and dual-path hybrid current sense amplifier, " *Current Applied Physics,* vol. 4, pp.25-29, Feb. 2004.

[6] E. Seevinck, P. Beers, and H. Ontrop, "Current-mode techniques for high-speed VLSI circuits with application to current sense amplifier for CMOS SRAMs," *IEEE J. Solid State Circuits,* vol.26, pp.525-536, Apr. 1991.

[7] S. Tanoi, Y. Tanaka, T. Tanabe, A. Kita, T. Inada, R. Hamazaki, Y. Ohtsuki, and M. Uesugi, "A 32-bank 256-Mb DRAM with cache and TAG," *IEEE J. Solid State Circuits,* vol.29, pp.1330-1335, Nov. 1994.

[8] K. Seno, K. Knorpp, L. L. Shu, N. Teshima, H. Kihara, H. Sato, F. Miyaji, M. Takeda, M. Sasaki, Y. Tomo, P. T. Chuang, and K. Kobayashi, "A 9-ns 16-Mb CMOS SRAM with offset-compensated current sense amplifier," *IEEE J. Solid State Circuits,* vol.28, pp.1119-1124, Nov. 1993.

[9] N. Shibata, "Current sense amplifiers for low-voltage memories," *IEICE Trans. on Electronics,* pp.1120-1130, 1996.

[10] Y. Kagenishi, H. Hirano, A. Shibayama, H.

Kotani, N. Moriwaki, M. Kojima, and T. Sumi, "Low-power self-refresh mode DRAM with temperature detecting circuit," *Symposium on VLSI Circuits*, pp.43-44, 1993.

[11] H. Tanaka, M. Aoki, T. Sakata, S. Kimura, N. Sakashita, H. Hidaka, T. Tachibana, and K. Kimura, "A precise on-chip voltage generator for a gigascale DRAM with a negative word-line scheme," *IEEE J. Solid State Circuits*, Vol. 34, pp.1084-1090, Aug. 1999.

[12] H. Yamauchi, T. Iwata, A. Uno, M. Funkmoto, and T. Fujita, "A circuit technology for self-refresh 16Mb DRAM with less than 0.5 uA/MB data-retention current," *IEEE J. Solid State Circuits*, vol. 30, pp.1174-1182, Nov. 1995.

[13] T. Yamagata, S. Tomishima, M. Tsukude, T. Tsuruda, Y. Hashizume, and K. Arimoto, "Low voltage circuit design techniques for battery-operated and/or giga-scale DRAM's," *IEEE J. Solid State Circuits*, vol. 30, pp.1183-1188, Nov. 1995.

[14] J. Y. Sim, K. W. Kwon, and K. C. Chun, "Charge-transferred presensing, negatively precharged word-line, and temperature-insensitive power-up schemes for low-voltage DRAMs," *IEEE J. Solid State Circuits,* vol.39, pp.694-703, Apr. 2004.

[15] Y. Sato, T. Suzuki, T. Aikawa, S. Y. Fujioka, W. Fujieda, H. Kobayashi, H. Ikeda, T. Nagasawa, A. Funyu, Y. Fujii, K. I. Kawasaki, M. Yamazaki, and M. Taguchi, "Fast cycle RAM(FCRAM); a 20-ns random row access pipe-lined operating DRAM," *Symposium on VLSI Circuits*, pp.22-25, 1998.

[16] Y. Yokoyama, Y. Yokoyama, N. Itoh, M. Hasegawa, M. Katayama, H. Akasaki, M. Kaneda, T. Ueda, Y. Tanaka, E. Yamasaki, M. Todokoro, K. Toriyama, H. Miki, M. Yagyu, K. Takashima, T. Kobayashi, S. Miyaoka, and N. Tamba, "A 1.8-V embedded 18-Mb DRAM Macro with a 9-ns RAS access time and memory-cell area efficiency of 33%," *IEEE J. Solid State Circuits*, vol. 36, pp.503-509, Mar. 2001.

[17] T. Nagai, K. Numata, M. Ogihara, M. Shimizu, K. Imai, T. Hara, M. Yoshida, Y. Saito, Y. Asao, S. Sawada, and S. Fujii, "A 17-ns 4-Mb CMOS DRAM," *IEEE J. Solid State Circuits*, vol. 26, pp.1538-1543, Nov. 1991.

[18] J. Y. Sim, K. W. Kwon, K. C. Chun, and D. I. Seo, "Offset- compensated direct sensing and charge-recycled precharge schemes for sub-1.0V high-speed DRAM's," *IEICE Trans. on Electronics*, vol. E87-C, pp.801-808, May, 2004.

[19] A. P. Brokaw, "A temperature sensor with single resistor set-point programming," *International Solid-State Circuit Conf.*, pp.334-335, 1996.

[20] A. Bakker and J. H. Huijsing, "Micropower CMOS temperature sensor with digital output," *IEEE J. Solid State Circuits,* vol.31, pp.933-937, Jul. 1996.

[21] M. A. P. Pertijs, A. Niederkorn, X. Ma, B. McKillop, A. Bakker, and J. H. Huijsing, "A CMOS smart temperature sensor with a 3σ inaccuracy of ±0.5°C from -50°C to 120°C," *IEEE J. Solid State Circuits,* vol.40, pp.454-461, Feb. 2005.

Jae-Yoon Sim received the B.S., M.S., and Ph.D. degrees in Electronic and Electrical Engineering from Pohang University of Science and Technology, Korea, in 1993, 1995, and 1999, respectively. From 1999 to 2005, he was a Senior Engineer at Samsung Electronics, Korea. From 2003, to 2005, he was a post-doctoral student with the University of Southern California, Los Angeles. In 2005, he joined the Faculty of Electronic and Electrical Engineering, Pohang University of Science and Technology, Korea, where he is currently an Assistant Professor. His research interests include PLL/DLL, high-speed links, memory circuits, and ultra low-power analog.