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LNA를 위한 새로운 프로그램 가능 고주파 검사용 설계회로

(New Programmable RF DFT Circuit for Low Noise Amplifiers)

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요 약

본 논문에서는 저잡음 증폭기 (LNA)를 위한 새로운 구조의 프로그램 가능한 고주파 검사용 설계회로 (RF DFT)를 제안한다. 개발된 RF DFT 회로는 DC 측정만을 이용하여 LNA의 RF 변수를 측정할 수 있으며, 최근의 RFIC 소자에 매우 유용하다. DFT 회로는 프로그램 가능한 커패시터 뱅크 (programmable capacitor banks)와 RF 피크 검출기를 가진 test amplifier를 포함하며, 측정된 출력 DC 전압을 이용하여 입력 임피던스와 전압이득과 같은 LNA 사양을 계산할 수 있다. 이러한 온 칩 DFT 회로는 GSM, Bluetooth 및 IEEE802g 표준에 이용할 수 있는 3가지 주파수 대역, 즉 1.8GHz, 2.4GHz, 5.25GHz용 LNA에서 사용할 수 있도록 자체적으로 프로그램 할 수 있다. 이 회로는 간단하면서도 저렴하다

Abstract

This paper presents a programmable RF DFT (Radio Frequency Design-for-Testability) circuit for low noise amplifiers. We have developed a new on-chip RF DFT circuit that measures RF parameters of low noise amplifier (LNA) using only DC measurements [1, 2]. This circuit is extremely useful for today's RFIC devices in a complete RF transceiver environment. The DFT circuit contains test amplifier with programmable capacitor banks and RF peak detectors. The test circuit utilizes output DC voltage measurements and these measured values are translated into the LNA specifications such as input impedance and gain using the mathematical equations. Our on-chip DFT circuit can be self programmed for 1.8GHz, 2.4GHz and 5.25GHz low noise amplifiers for GSM, Bluetooth and IEEE802.11g standards. The circuit is simple and inexpensive.

Keywords : *Programmable RF DFT, low noise amplifier, DC measurement*

I. Introduction

A rapid growth in radio frequency (RF) integrated circuit devices demands high density, high speed and low-cost RF systems. To realize these recent trends, system-on-chip (SoC) has become a new solution in today's RFIC industry. However, the suitable test technique and reduction of test cost for SoC still remain to be the major bottleneck to make affordable wireless systems. To solve these problems, the test technique using DFT (Design-for-Testability) circuit in the RF and mixed-signal domain is applied as a suitable test structure on SoC[1-8].

To design an effective RF DFT structure, proper identifications of catastrophic faults and parametric variations in RF system play an integral part of the design. Analog systems have only a few inputs and outputs, and their internal states exhibit low time constants compared to digital circuits[9-11]. A test resulting in a high coverage for catastrophic faults is possible using the standard approach based on current

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test stimulus and frequency domain measurements. However, according to Pleskacz et. al., the standard approach based on current test stimulus covers only linear circuits[12]. This approach is difficult when used to detect and diagnose spot defects that severely result in non-linear RF circuits implemented as CMOS or BiCMOS ICs[5]. The frequency domain measurement technique requires more test cost.

To test point-to-point transceiver, loop-back technique using spectral signature analysis is generally used with lower effort and very small test overhead[3-5]. However, this test technique has disadvantages such as lower test coverage due to the fact that the complete transceiver is tested as a whole and the need of an additional DSP due to the higher complexity of the test signature generation[4]. Voorakaranam *et. al.*[6] showed gain, noise figure and IIP3 tests of 900MHz LNA using signature test with optimized test stimulus. Their technique also requires additional off-chip signature response evaluator such as FASTest RF runtime system.

Ⅱ. Approach

Conventional way of testing LNA involves measurements of S-parameters, noise figures, signal-to noise ratios and sensitivities using variety of different RF test equipment. It is highly labor intensive and requires expensive measurement equipment. Our proposed technique utilizes on-chip DFT circuit to measure important LNA specifications without major external test equipment. Our new RF DFT circuit provides DC output voltages, hence, making the overall test set-up simple, inexpensive and automatic. These DC output voltages are converted to units of decibels and ohms by using the equations we developed for the LNA specifications. The following describes details of our approach.

Figure 1 shows test set-up for low noise amplifier. It contains LNA and DFT circuit all on a single chip. Our proposed DFT circuit provides DC outputs so that all of the measurements can be done by on-chip data converter within the SoC. The test structure can be

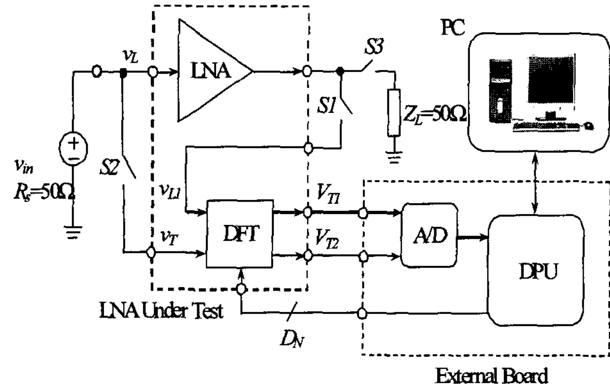


그림 1. RF 저잡음 증폭기를 위한 측정 구성
Fig. 1. Measurement set-up for RF low noise amplifier.

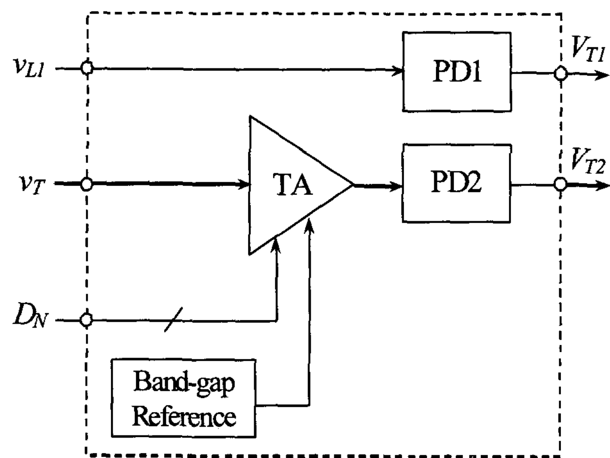


그림 2. RF DFT 하드웨어의 블록도
Fig. 2. Block diagram of RF DFT hardware.

automatically configured by the external data acquisition hardware. The complete test-bed contains RF source (v_{in}) with source resistance (R_s), RF relays (S1, S2 and S3), load impedance (Z_L), and a data converter board.

The measurement set-up contains low loss RF relays and input transmission matching to the LNA and DFT circuits. The positions of the relays are controlled to measure the output DC voltages, V_{T1} and V_{T2}, through the DFT circuit. These relays are controlled by DeMux chip on external board. The RF DFT hardware consists of test amplifier (TA), band-gap reference and two RF peak detectors (PD1 and PD2) as shown in Figure 2. The test amplifier has programmable capacitor banks for operating frequencies of 1.8GHz, 2.4GHz and 5.25GHz by having digital bit streams (D_N) from the digital processor unit (DPU). The DFT hardware occupies approximately

10% of the total chip area and it helps to measure LNA performance without expensive external equipment. In our testing approach, we assumed a unilateral LNA at 1.8GHz, 2.4GHz and 5.25GHz as discussed in [13].

In this paper, we consider measurements of input impedance, gain, voltage standing wave ratio, input return loss and output signal-to-noise ratio of the LNA. We consider fault-free and faulty cases and the following sections will present mathematical expressions that are developed to translate from the output DC measurements to the actual LNA parameters.

2.1. Input Impedance

Figure 3 shows the equivalent circuit for the inputs of the LNA and test amplifier. Z_1 and Z_2 represent the input impedance of the LNA and test amplifier, respectively. These impedances have real and imaginary parts.

The input impedance measurement is performed with the switches S2 and S3 in closed position and the switch S1 in open position from Figure. 1. The overall test technique is to find any deviations between the source impedance (R_s) and the input impedances (Z_1 and Z_2). For example, the test amplifier of Figure.3 looks for changes in input impedance of the LNA for any mismatch with the source resistance. In case of a mismatch due to a defect or a process variation, the DC voltage at the output of RF DFT circuit is presented.

Let's consider fault-free LNA with good input

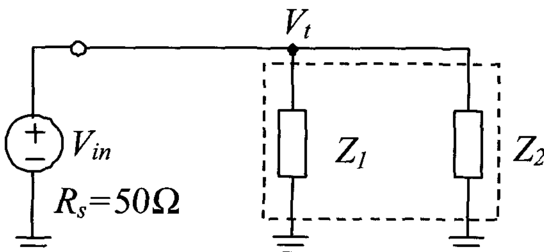


그림 3. 저잡음 증폭기와 검사용 증폭기의 입력 등가회로

Fig. 3. Equivalent circuit for the inputs of the LNA and test amplifier.

matching condition. The Equation (1.1) represents the theoretical values for the voltage across the input impedances of the LNA and TA. The TA is designed with the input and output matching impedances of 50 Ω, and a flat gain of $K_2 \approx 3$ to increase test output voltage to the original input voltage level $|V_{in}|$ as indicated in Equation (1.2). The DFT circuit monitors the DC voltage V_{T2} as shown in Fig. 1. Equations (1.1) and (1.2) represent important expressions that are developed to derive input impedance of the LNA.

$$|V_t| = \left|\frac{Z_1 // Z_2}{[R_s + (Z_1 // Z_2)]}\right| |V_{in}| = \left|\frac{Z_1}{2Z_1 + R_s}\right| |V_{in}| \quad (1.1)$$

$$V_{T2} = |v_{TAout}| + V_{02} = |V_t| K_2 + V_{02} = \left|\frac{Z_1}{2Z_1 + R_s} V_{in}\right| K_2 + V_{02} \quad (1.2)$$

where $|Z_1|$ and $|Z_2|$ are magnitudes of input impedances of LNA and TA, respectively, K_2 is voltage gain of TA and V_{02} is offset voltage of the peak detector circuit, PD2. Since the complex impedances of the LNA and the test amplifier can be said to have $\mathrm{Re}(Z_1) >> \mathrm{Im}(Z_1)$ and $\mathrm{Re}(Z_2) >> \mathrm{Im}(Z_2)$, their magnitudes $|Z_1|$ and $|Z_2|$ are respectively expressed by

$$|Z_1| = \sqrt{[\mathrm{Re}(Z_1)]^2 + [\mathrm{Im}(Z_1)]^2} \approx \mathrm{Re}(Z_1) \quad (1.3)$$

$$|Z_2| = \sqrt{[\mathrm{Re}(Z_2)]^2 + [\mathrm{Im}(Z_2)]^2} \approx \mathrm{Re}(Z_2) \quad (1.4)$$

Using the measured V_{T2} voltage, Equation (2) is obtained to calculate the fault-free LNA impedance, Z_1

$$|Z_1| = f(V_{T2}) = R_s \frac{K_1}{1 - \left(1 + \frac{R_s}{|Z_2|}\right) K_1} [\Omega] \quad (2)$$

where $K_1 = \frac{K_{02}}{K_2}$, K_{02} is the voltage gain expressed as $K_{02} = \frac{V_{T2} - V_{02}}{V_{\in}}$.

Under a faulty condition, the LNA can have catastrophic faults such as resistive short and open faults due to the spot defects and parametric faults such as unusual thermal variations and unusual process variations[4]. In this case, there is a certain variation in magnitude of input impedance of LNA because of change in its input matching condition. This condition provides a new value in V_{T2}, which is the output DC voltage for faulty LNA. The input impedance of the LNA under a faulty condition can be expressed as

$$\overline{|Z_1|} = f(\overline{V_{T2}}) = R_s \frac{\overline{K_1}}{1-\left(1+\frac{R_s}{|Z_2|}\right)\overline{K_1}} [\Omega] \quad (3)$$

where $\overline{K_1} = \frac{\overline{K_{02}}}{K_2}$ and $\overline{K_{02}}$ is the voltage gain expressed as $\overline{K_{02}} = \frac{\overline{V_{T2}} - V_{02}}{V_{in}}$ under a faulty condition. The bar represents the parameters under faulty conditions.

2.2. Voltage Gain

The voltage gain measurement is performed with the switch S1 in closed position and the switches S2 and S3 in open position from Figure. 1. The voltage gain measurement is based on monitoring the DC voltage of the first peak detector, PD1. The DFT circuit monitors the DC voltage V_{T1} as shown in Figure. 1.

$$V_{T1} = K|V_L| + V_{01} \quad (4)$$

where K is LNA voltage gain and V_{01} is the offset voltage for the peak detector circuit, PD1.

From Figure. 1, Equation (5) is obtained.

$$|V_L| = \frac{|Z_1|}{R_s + |Z_1|}|V_{in}| \quad (5)$$

Using the measured V_{T1} and V_{T2} voltages, new expression for Equation (6) to calculate the fault-free LNA gain, K is used.

$$K = f(V_{T1}, V_{T2}) = \left(1+\frac{R_s}{|Z_1|}\right)K_{01} \quad (6)$$

where K_{01} is the voltage gain expressed as $K_{01} = \frac{V_{T1} - V_{01}}{V_{in}}$.

Under a faulty condition, the DFT circuit provides a new value in V_{T1}, which is the output DC voltage for faulty LNA. The voltage gain of the LNA under a faulty condition can be expressed as

$$\overline{K} = f(\overline{V_{T1}}, \overline{V_{T2}}) = \left(1+\frac{R_s}{\overline{|Z_1|}}\right)\overline{K_{01}} \quad (7)$$

where $\overline{K_{01}}$ represents the voltage gain expressed as $\overline{K_{01}} = \frac{\overline{V_{T1}} - V_{01}}{V_{in}}$ under the case of a fault.

2.3. Input Return Loss

The input return loss (RL_{in}) is an important parameter in LNA. Using unilateral LNA assumption [13], we obtained input return loss of the LNA.

$$RL_{in} = f(V_{T2}) = 20\log\left|\frac{|Z_1| - Z_0}{|Z_1| + Z_0}\right| \quad (8)$$

where Z_0 is the characteristic impedance of the LNA.

Under the case of a fault, input return loss can be expressed as Equation (9).

$$\overline{RL_{in}} = f(\overline{V_{T2}}) = 20\log\left|\frac{\overline{|Z_1|} - Z_0}{\overline{|Z_1|} + Z_0}\right| \quad (9)$$

2.4. Input Voltage Standing Wave Ratio

The input voltage standing wave ratio ($VSWR_{in}$) is also an important parameter in LNA. The value for VSWR should be minimized to avoid high insertion loss in LNA. From our DFT structure, we have developed an expression for the fault-free VSWR, which is shown in Equation (10).

$$VSWR_{in} = f(V_{T2}) = \frac{1+|\Gamma_{in}|}{1-|\Gamma_{in}|} \quad (10)$$

where Γ_{in} is the reflection coefficient expressed as $\Gamma_{in} = \frac{|Z_1| - Z_0}{|Z_1| + Z_0}$ and Z_0 is the characteristic impedance of the LNA.

Under the case of a fault, $VSWR_{in}$ can be expressed as Equation (11).

$$VSWR_{in} = f(\overline{V_{T1}}) = \frac{1+\overline{|\Gamma_{in}|}}{1-\overline{|\Gamma_{in}|}} \quad (11)$$

The bars represent defective parameters under faulty conditions.

2.5. Output Signal-to-Noise Ratio

The noise figure has been defined in a number of different ways. The most commonly accepted definition[16] is

$$NF = \frac{SNR_{in}}{SNR_{out}} \quad (12)$$

where SNR_{in} and SNR_{out} are the signal-to-noise ratios (SNR) measured at the input and output, respectively. SNR_{in} must be measured for the reference resistance noise.

Using open literature[16], the SNR_{in} measured at the input can be expressed as Equation (13).

$$SNR_{in} = \frac{\left(|Z_1|V_{in}^2\right)/2\left(R_s+|Z_1|\right)^2}{\left(4kTBR_s/4|Z_1|\right)} = \frac{\left(|Z_1|V_{in}\right)^2}{2R_s\left(R_s+|Z_1|\right)^2 kTB} \quad (13)$$

where V_{in} is RMS voltage of the input signal, kT is -174 dBm/Hz and B is signal bandwidth.

From Equations (12) to (13), the SNR_{out} at the output using DFT circuit is

$$SNR_{out} = f(V_{T1}, V_{T2}) = \frac{\left(|Z_1|V_{in}\right)^2}{2R_s\left(R_s+|Z_1|\right)^2 kTB} \cdot \frac{1}{NF} \quad (14)$$

Under the case of a fault, Equation (14) can be expressed as Equation (15).

$$\overline{SNR_{out}} = f(\overline{V_{T1}}, \overline{V_{T2}}) = \frac{\left(\overline{|Z_1|}V_{in}\right)^2}{2R_s\left(R_s+\overline{|Z_1|}\right)^2 kTB} \cdot \frac{1}{\overline{NF}} \quad (15)$$

Ⅲ. Fault Models

Both catastrophic faults and parametric faults are considered for BJTs, CMOS and passive components [1,2,8]. Spot defects that can severely degrade the performance or result in chip malfunction are considered[5]. We designed the LNA using 0.18㎛ BiCMOS technology. We considered physical defects in both BJTs and N-MOSFETs. Resistors and inductors with open faults are selected to have approximately 10 times the given values, and resistors and inductors with short faults are selected to have approximately 0.1 times the given values. For capacitor defects, open faults have approximately 0.1 times the given values, and short faults have approximately 10 times the given values[1,2,8]. We considered ±10% to ±50% variations in resistors, capacitors and inductors, and ±25% and ±50% for number of emitters, emitter width and length variations in BJTs for parametric faults. We also considered ±25% and ±50% for channel width variations in N-MOSFETs for parametric faults. For 5.25GHz LNA a total of 173 different fault models are considered. Amongst them are a fault-free model, 28 different catastrophic fault models and 144 different parametric fault models. For 1.8GHz LNA a total of 111 different fault models are considered. Amongst them are a fault-free model, 22 different catastrophic fault models and 88 different parametric fault models. For 2.4GHz LNA a total of 111 different fault models are also considered. Amongst them are a fault-free model, 22 different catastrophic fault models and 88 different parametric fault models.

Ⅳ. Analysis

To verify performance of our proposed DFT circuit, we have designed three different RF LNAs with

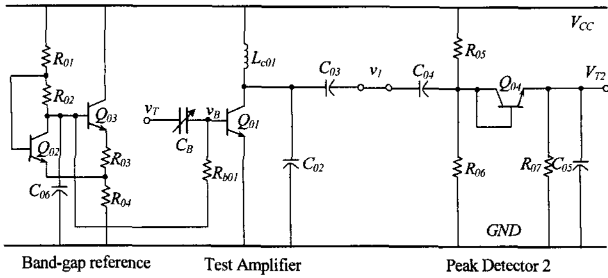


그림 4. RF DFT의 회로도
Fig. 4. Schematic diagram of RF DFT.

operating frequencies of 1.8GHz, 2.4GHz and 5.25GHz using 0.18㎛ SiGe technology. The proposed DFT circuit is shown in Figure. 4. It consists of test amplifier with programmable capacitor banks, C_B and peak detector circuit stages. The RF peak-detectors are used for converting from RF signal to DC voltage.

The bias stage utilizes band-gap reference circuit for a low supply voltage and low power dissipation. The inductor (L_{c01}) is used for input and output impedance matching. The bias resistors (R_{05} and R_{06}) shown in Figure. 4 are used to keep transistor Q_{04} in the active region so that the transistor acts as a rectifier. The diode connections have advantages of resulting in keeping the base-collector junction at zero bias. The smallest amount of minority charge storage during forward biased condition will be highly beneficial to rectification of RF signals[15]. To reduce the output ripple voltage, R_{07} and C_{05} are chosen with large values. We also performed process variation simulations on the LNA and DFT circuits. The variable capacitor, C_B, is used for different LNAs.

The DFT circuit can handle different frequencies by adjusting the value of the capacitance (C_B) as shown in Figure 5. We have designed 1.8GHz, 2.4GHz and 5.25GHz low noise amplifiers for GSM, Bluetooth and IEEE802.11g standards with DFT circuit on a single chip using 0.18㎛ SiGe technology to demonstrate this idea. It has 3-bit programmable capacitor banks to operate at different RF frequencies. The capacitor banks are controlled by using digital signals, ($D_1D_2D_3$), from the DPU. The input data streams of ($D_3D_2D_1$) = (001) for 5.25GHz, (011) for 2.4GHz and (111) for 1.8GHz have been used for three different LNA frequencies. It is powered by 1.8volts supply voltage.

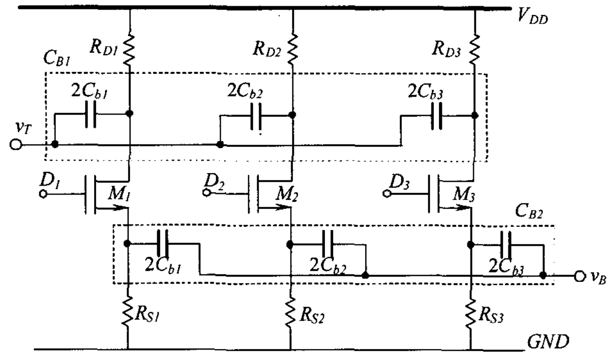


그림 5. 커패시터 뱅크 CB의 회로도
Fig. 5. Schematic Diagram of Capacitor Banks, CB.

The transistors M_1, M_2 and M_3 are designed for operating in deep triode region so that they exhibit no dc shift between the input and output voltages[16].

The resistors (R_{D1}, R_{D2}, R_{D3}, R_{S1}, R_{S2} and R_{S3}) are used to control DC bias voltage of MOS switches. To handle three different frequency ranges and to reduce total occupied chip area for capacitors, the capacitor banks, C_{b1}, C_{b2} and C_{b3} are selected with three different values.

Figure 6 shows high-frequency small-signal model for the test amplifier and peak detector[14-15]. Simultaneous matching is performed, and the effect of the load impedance is taken into account in the simplified small-signal BJT and inductor models shown in Figure. 6. To verify and compare the accuracy of the designed DFT circuit, accurate modeling is performed. The transistor is replaced with hybrid-π model, and the inductor is replaced with series resistance R and its inductance L. From an analytical analysis of DFT circuit, the input impedance, voltage gain and transfer functions are obtained. The output resistance r_{o01} of the transistor Q_{01} due to its high value is neglected.

The magnitude of input impedance of the test

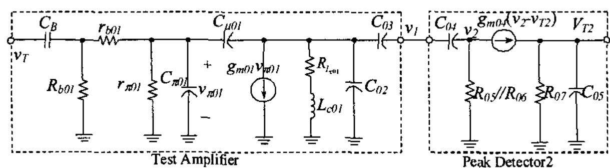


그림 6. DFT 회로에 대한 고주파 소신호 모델
Fig. 6. High-frequency small-signal model for DFT circuit.

amplifier from Figure. 6 can be expressed as

$$|Z_2| \approx \frac{A(\omega)+B(\omega)}{\omega^2 R_{b01} C_{01}[Z_{L01} C_{\mu 01}(1/r_{\pi 01} - \omega^2 g_{m01} Z_{L01} C_{\mu 01}) - (C_{\mu 01} + C_{\pi 01})]} \quad (16.1)$$

where

$$A(\omega) = 1 + (R_{b01} + 2r_{b01})(1/r_{\pi 01} - \omega^2 g_{m01} Z_{L01} C_{\mu 01} + r_{b01}(R_{b01} + r_{b01})(1/r_{\pi 01} - \omega^2 g_{m01} Z_{L01} C_{\mu 01})^2 \quad (16.2)$$

$$B(\omega) = \left(1 + \frac{R_{b01}}{r_{b01}}\right) [Z_{L01} C_{\mu 01} + r_{b01}(C_{\mu 01} + C_{\pi 01})] \left[Z_{L01} C_{\mu 01} + r_{b01}(C_{\mu 01} + C_{\pi 01}) - \frac{R_{b01} Z_{L01} C_{\mu 01}}{r_{b01}}\right] \quad (16.3)$$

$$Z_{L01} = \frac{L_{c01}[(1 - \omega C_{03} \mathrm{Im}(Z_{PD2})] + R_{L_{c01}} C_{03} \mathrm{Re}(Z_{PD2})}{R_{L_{c01}}[(C_{02} + C_{03}) - \omega C_{02} C_{03} \mathrm{Im}(Z_{PD2})] + C_{03} \mathrm{Re}(Z_{PD2})(1 - \omega^2 L_{c01} C_{02})} \quad (16.4)$$

$$\mathrm{Re}(Z_{PD2}) = \frac{(a_1 b_1 - a_0 b_2 \omega^2 + a_2 b_2 \omega^4)}{\omega^2 (b_1^2 + b_2^2 \omega^2)} \quad (16.5)$$

$$\mathrm{Im}(Z_{PD2}) = \frac{-a_0 b_1 + (a_2 b_1 - a_1 b_2)\omega^2}{\omega^2 (b_1^2 + b_2^2 \omega^2)} \quad (16.6)$$

$$\begin{aligned} a_0 &= g_{m04} R_{05} R_{06} + (R_{05} + R_{06})(1 + g_{m04} R_{07}) \\ a_1 &= g_{m04} R_{05} R_{06} R_{07} C_{05} + (R_{05} + R_{06}) R_{07} C_{05} + R_{05} R_{06}(1 + g_{m04} R_{07}) C_{04} \\ a_2 &= R_{05} R_{06} R_{07} C_{04} C_{05} \\ b_1 &= a_0 C_{04} \\ b_2 &= [a_1 - R_{05} R_{06}(1 + g_{m04} R_{07})] C_{04} \end{aligned} \quad (16.7)$$

The equations related to voltage gain of test amplifier are listed in Equations (17.1) to (17.3).

$$K_2 = \frac{N(w)}{D(w)} \quad (17.1)$$

where

$$N(\omega) = (1 - g_{m01} Z_{F01})(j\omega C_{03}) Z_{PD2} \quad (17.2)$$

$$D(\omega) = [1 + (j\omega C_{03}) Z_{PD2}] \cdot \left\{ \begin{aligned} &\left(1 + \frac{Z_{F01}}{Z_{c01}}(1 + j\omega C_{02} Z_{c01})\right) \left[\left(1 + \frac{Z_B}{R_{b01}} + \frac{r_{b01}}{Z_{F01}}\left(1 + \frac{Z_B}{R_{b01}} + \frac{Z_B}{r_{b01}}\right)\right) + \left(1 + \frac{Z_B}{R_{b01}} + \frac{Z_B}{r_{b01}}\right)\right] \\ &- \frac{r_{b01}}{Z_{F01}}\left(1 + \frac{Z_B}{R_{b01}} + \frac{Z_B}{r_{b01}}\right)(1 - g_{m01} Z_{F01}) \end{aligned} \right\} \quad (17.3)$$

From direct transfer function analysis for peak detectors, PD2 and PD1, we obtained equations listed in Equations (18.1) to (18.2).

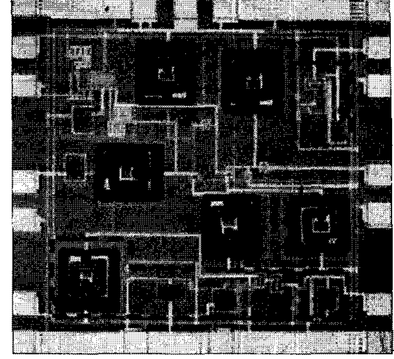


그림 7. DFT 회로가 있는 LNA 칩 사진
Fig. 7. Chip micrograph of LNA with DFT circuit.

$$H_{PD2}(s) = \frac{s g_{m04} R_{05} R_{06} R_{07} C_{04}}{[(1 + g_{m04} R_{07}) + s R_{07} C_{05}][(R_{05} + R_{06}) + s R_{05} R_{06} C_{04}]} \quad (18.1)$$

$$H_{PD1}(s) = \frac{s g_{m04}' R_{05}' R_{06}' R_{07}' C_{04}'}{[(1 + g_{m04}' R_{07}') + s R_{07}' C_{05}'][(R_{05}' + R_{06}') + s R_{05}' R_{06}' C_{04}']} \quad (18.2)$$

where prime mark represents each component for the peak detector, PD1.

For details for DC and high frequency small-signal analysis of the capacitor banks, refer to APPENDIX A.

Figure. 7 shows chip micrograph of the LNA with DFT circuit. The DFT block is indicated in dotted lines. The physical chip area is approximately 1.45mm × 1.45mm.

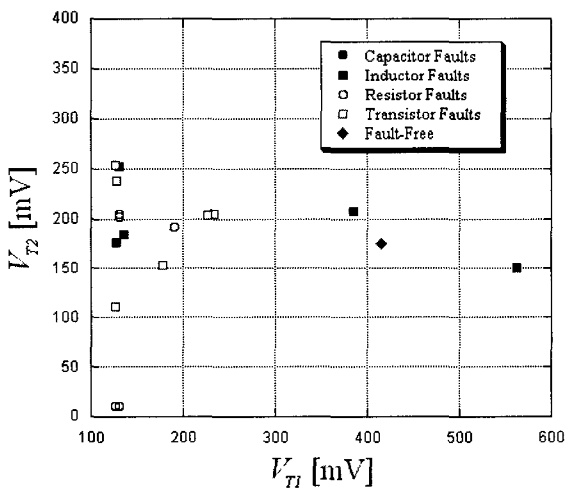
V. Results

A typical testing of LNA involves expensive measurement equipment. Our RF DFT circuit provides DC voltages (V_{T1} and V_{T2}), which can be used to find LNA specifications through the mathematical expressions shown in previous section. We now present the results of LNA measurements. For details for results of 5.25GHz LNA, refer to [2,8]

A) Defect vs. Outputs

Figures 8(a) and 8(b) show the scatter plots of DC

output voltages for various faults for catastrophic and parametric variations in 2.4GHz low noise amplifier using proposed test structure shown in Figure 1. These figures show the scatter plots of DC voltages for various faults including open, short and parametric variations in low noise amplifiers. These DC voltages are measured after 40 nanoseconds settling time of the peak detectors to ensure steady-state DC value. The output RC time constant of the peak detector contributed to the settling time constant. As can be seen from Figure 8(a), most of the catastrophic faults are in the lower end of V_{T1} with varying V_{T2}. For resistor and transistor faults shown, the observed output voltages V_{T1} remain in far left side as compared to a fault-free value. These results reveal that lower



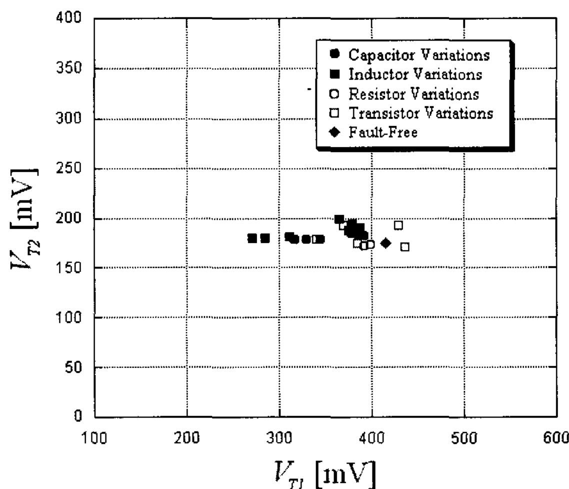


그림 8. 2.4GHz LNA에 대한 (a) 거폭 결함 및 (b) 미세 변동 그림

Fig. 8. Scatter plots of (a) catastrophic and (b) parametric variations for 2.4GHz LNA.

voltages of V_{T1} indicate faults in resistors and transistors. These results show that the proposed DFT structure is suitable to detect variety of faults for go-no go screening at the wafer level. Figure 8(b) shows the scatter plot for parametric variations. It shows that the parametric faults are concentrated near the fault-free case. We used RF input source from 100mV to 180mV at 1.4 - 6.0GHz for all three different LNAs, which showed similar results as shown in Figures 8(a) and (b).

Tables 1 and 2 show list of partial values of input impedances, gains, voltage standing wave ratios, input return losses and output signal-to-noise ratios of the 1.8GHz and 2.4GHz low noise amplifiers, respectively. We used Equations (2) to (15) to calculate fault-free and faulty values. These values are compared with real measurement values. As can be seen from the tables, the required specifications that are measured by the DFT circuit were very close to the external equipment measurements. These results reveal that our proposed

표 1. 1.8GHz LNA에 대한 RF DFT 검사와 종래의 검사 비교

Table 1. Comparisons between RF DFT testing and conventional testing for 1.8GHz LNA.

Test / Faults	External Equipment Test					Proposed On-Chip DFT Test				
	$\|Z_1\|$[Ω]	K[dB]	$VSWR_{in}$	RL_{in}[dB]	SNR_{out}[dB]	$\|Z_1\|$ [Ω]	K [dB]	$VSWR_{in}$	RL_{in}[dB]	SNR_{out}[dB]
Fault-free	51.69	15.30	1.0338	-35.6	98.94	47.62	15.35	1.0500	-32.3	98.42
M_l Gate Open	4780	-84.55	95.594	-0.19	24.52	614.2	-89.78	12.285	-1.42	31.70
M_l G-S Short	100.1	-46.21	18.627	-0.94	58.96	258.7	-48.92	5.1740	-3.40	68.01
M_l S-D Short	22.61	-3.845	3.7660	-4.73	77.63	30.01	-1.114	1.6670	-10.5	83.84
L_l + 30%	59.54	14.84	1.6000	-12.7	99.61	58.54	13.95	1.1710	-22.1	99.30
L_l + 40%	64.24	14.59	1.8600	-10.4	99.99	63.18	13.57	1.2640	-18.7	99.65
L_l + 50%	69.67	14.31	2.1500	-8.76	100.3	69.79	13.08	1.3960	-15.6	100.0

표 2. 2.4GHz LNA에 대한 RF DFT 검사와 종래의 검사 비교

Table 2. Comparisons between RF DFT testing and conventional testing for 2.4GHz LNA.

Test / Faults	External Equipment Test					Proposed On-Chip DFT Test				
	$\|Z_1\|$[Ω]	K[dB]	$VSWR_{in}$	RL_{in}[dB]	SNR_{out}[dB]	$\|Z_1\|$ [Ω]	K [dB]	$VSWR_{in}$	RL_{in}[dB]	SNR_{out}[dB]
Fault-free	48.81	15.69	1.0245	-38.4	98.61	46.69	15.53	1.0710	-29.3	98.29
M_{01} Gate Open	4116	-84.48	82.333	-0.21	22.82	416.5	-89.47	8.3298	-2.10	60.22
M_{01} G-S Short	100.0	-39.66	2.000	-9.54	69.55	198.3	-42.49	3.9658	-4.48	87.61
M_{01} S-D Short	32.17	0.445	1.5543	-13.3	83.67	32.95	2.116	1.5174	-13.7	88.92
L_{01} + 30%	60.72	15.08	1.2144	-20.3	99.51	60.78	14.33	1.2156	-20.2	99.34
L_{01} + 40%	66.34	14.78	1.3267	-17.1	99.84	67.44	13.81	1.3488	-16.6	99.70
L_{01} + 50%	72.48	14.46	1.4496	-14.7	100.1	72.58	13.43	1.4516	-14.7	99.88

on-chip DFT scheme is suitable for go-no go test of the LNA. We noticed that conventional testing provided significant differences between fault-free and faulty LNA. On the other hand, the proposed DFT testing provided with the similar differences between the two. Therefore, the proposed DFT structure provided the same fault coverage with significantly less cost. The fault detection of the LNA can be made by looking at the gain, impedance or input return loss variations. We tried similar experiments for the 5.25GHz frequency LNA and it provided with similar results [2,8]. The proposed on-chip DFT scheme showed fault coverage of 100% for catastrophic faults and approximately 90% for process variations. There was very small deviation between the conventional and proposed on-chip DFT scheme for fault-free case as indicated in Tables 1 and 2.

B) Frequency vs. DFT Performance

We were able to adjust the input capacitance (C_B) of the RF DFT circuit by providing a combination of digital codes to the capacitor banks. This feature provided us with capability to use the same DFT circuit to different frequency LNAs. Hence, a complete programmable DFT circuit is incorporated to the designs of the low noise amplifiers. Table 3 provides the test amplifier gains and input impedances. These results are used to obtain magnitudes of input impedances of the 1.8GHz and 2.4GHz LNAs. The gain of the test amplifier is designed for 3 at the specific frequency and the system calibrates it before the testing begins. As shown in the table, the measured

표 3. 검사용 증폭기의 이득과 입력 임피던스

Table 3. Gains and input impedances of the test amplifier.

($D_3D_2D_1$)	Frequency [GHz]	S-Parameter Results		Modeling	
		K_2	$\|Z_2\|$ [Ω]	K_2	$\|Z_2\|$ [Ω]
(111)	1.6	2.925	52.49	2.923	52.35
	1.7	2.994	51.40	2.992	51.31
	1.8	3.025	50.24	3.021	50.12
	1.9	3.040	49.11	3.036	49.02
	2.0	3.045	48.01	3.042	47.93
(011)	2.2	2.910	51.20	2.909	51.09
	2.3	2.979	50.11	2.978	49.99
	2.4	3.010	48.95	3.009	48.84
	2.5	3.025	47.82	3.023	47.71
	2.6	3.030	46.72	3.029	46.61

S-parameters provided very close results with modeling at frequency range.

We also considered parametric variations from ±10% to ±25% of all the passives on the DFT circuit to verify accuracy of designed DFT circuit. The parametric variations on the inductor L_{c01} shown in Figure. 4 was most sensitive to the gain of the LNA. The maximum change in the gain of the LNA due to the DFT circuit was less than 0.02dB for all of the three LNAs. Therefore, the value can be neglected for the measurement error.

With the DFT circuit, we tested low noise amplifiers in different RF ranges. Tables 4 and 5 list comparisons for the input impedances, gains, input voltage standing wave ratios, input return losses and output signal-to-noise ratios of LNAs with 1.8GHz and 2.4GHz operating frequencies, respectively. As can be seen in the tables, our proposed DFT test results are very close to external equipment measurements. These results reveal that our proposed on-chip DFT scheme is suitable for functional test of the LNA at the packaged level. The proposed DFT structure provided similar results with significantly less cost. We tried similar experiments for the 5.25GHz frequency LNA and it provided with similar results [2,8].

표 4. 1.8GHz LNA에 대한 성능 비교

Table 4. Comparisons of functional results for 1.8GHz LNA.

Frequency [GHz]	External Equipment Test					Proposed On-Chip DFT Test				
	$\|Z_1\|$ [Ω]	K[dB]	$VSWR_{in}$	RL_{in}[dB]	SNR_{out}[dB]	$\|Z_1\|$ [Ω]	K[dB]	$VSWR_{in}$	RL_{in}[dB]	SNR_{out}[dB]
1.6	57.057	12.799	1.1411	-23.62	99.631	55.967	12.600	1.1194	-24.99	99.435
1.7	51.058	14.594	1.0212	-39.60	98.912	46.493	15.136	1.0754	-28.79	98.368
1.8	51.688	15.301	1.0388	-35.60	98.938	47.616	15.348	1.0500	-32.25	98.421
1.9	57.457	14.360	1.1492	-23.17	99.512	53.755	13.959	1.0751	-28.83	98.912
2.0	62.292	12.431	1.2458	-19.21	99.868	58.762	11.830	1.1752	-21.88	99.225

표 5. 2.4GHz LNA에 대한 성능 비교

Table 5. Comparisons of functional results for 2.4GHz LNA.

Frequency [GHz]	External Equipment Test					Proposed On-Chip DFT Test				
	$\|Z_1\|$ [Ω]	K[dB]	$VSWR_{in}$	RL_{in}[dB]	SNR_{out}[dB]	$\|Z_1\|$ [Ω]	K[dB]	$VSWR_{in}$	RL_{in}[dB]	SNR_{out}[dB]
2.2	46.889	13.430	1.0664	-29.87	98.574	44.603	14.282	1.1210	-24.88	98.082
2.3	45.818	14.992	1.0913	-27.20	98.329	42.891	15.625	1.1658	-22.32	97.766
2.4	48.804	15.688	1.0245	-38.34	98.614	46.685	15.530	1.0710	-29.30	98.291
2.5	54.626	14.984	1.0925	-27.09	99.179	56.599	13.977	1.1320	-24.17	99.186
2.6	59.537	13.283	1.1947	-21.04	99.530	61.744	12.483	1.2355	-19.55	99.578

VI. Conclusions

This paper presented a new programmable RF Design-for-Testability circuit. We proved that our programmable RF DFT circuit can help to sort out good and bad RFIC chips in the wafer level as well as providing all of the functional testing. Utilizing our new DFT circuit, we measured input impedance, gain, input return loss, input voltage standing wave ratio and output signal-to-noise ratio. The new programmable RF DFT circuit provided successful testing of LNA chips. Three different operating frequencies were self programmed in the DFT. The RF low noise amplifiers provided with complete testing by utilizing a novel DFT architecture and mathematical equations. We believe that this new capability will provide industry with a low-cost technique to test RFIC chips.

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APPENDIX A

Let's consider DC model shown in Figure A.1 to explain DC bias condition of the 1-bit capacitor bank.

When the digital input D1 shown in Figure A.1(a) is logic high state with 1.8volts, the MOS switch is closed since it is designed with $V_{DS1} \ll 2(V_{GS1} - V_{TH1})$ for operating in the deep triode region. On the other hand, when the D1 is

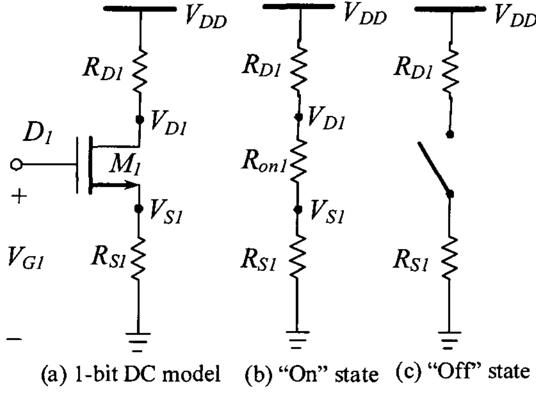

그림 A.1. 1-비트 커패시터 뱅크의 DC 모델
Fig. A.1. DC model of 1-bit capacitor bank.

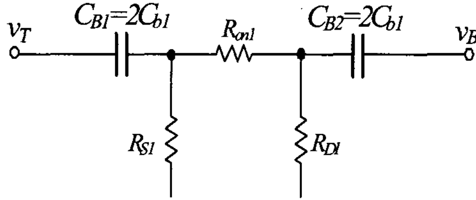

그림 A.2. 소신호 모델
Fig. A.2. Small-signal model.

logic low state with 0volt, the MOS switch is open. In this circuit, the on resistance of the MOS switch expressed in Equation (a.1) is designed with approximately 2 ohms. The other DC parameters are described in Equations (a.2) to (a.5).

$$\frac{V_{DS1(on)}}{I_{DS1(on)}} = R_{on1} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS1} - V_{TH1})} \quad \text{(a1)}$$

$$V_{S1} = V_{G1} - V_{GS1} = 1.8 - 0.7 = 1.1[V] \quad \text{(a2)}$$

$$I_{D1(on)} = 0.1[mA] \quad \text{(a3)}$$

$$R_{S1} = \frac{V_{G1} - V_{GS1}}{I_{D1(on)}} = \frac{1.1[V]}{0.1[mA]} = 11[k\Omega] \quad \text{(a4)}$$

$$R_{D1} = \frac{V_{DD} - V_{D1}}{I_{D1(on)}} = \frac{V_{DD} - V_{DS1(on)} - V_{S1}}{I_{D1(on)}} = \frac{0.6[V]}{0.1[mA]} = 6[k\Omega] \quad \text{(a5)}$$

Using this DC model, when ($D_3D_2D_1$) = (001), Figure 5 shown in Section IV can be modeled as Figure A.2.

Since $R_{D1} \gg \left|\frac{1}{w(2C_{b1})}\right| \gg R_{on1}$ and

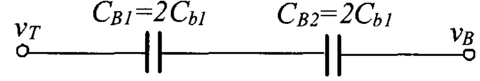

그림 A.3. 그림 A.2의 등가 모델
Fig. A.3. Equivalent model for Figure A.2.

$R_{S1} \gg \left|\frac{1}{w(2C_{b1})}\right| \gg R_{on1}$, we obtain equivalent model shown in Figure A.3.

From Figure A.3, we obtain Equation (a.6).

$$C_B = \frac{C_{B1}C_{B2}}{C_{B1} + C_{B2}} = C_{b1} \quad \text{(a6)}$$

This circuit is designed so that when ($D_3D_2D_1$) = (001), $C_B = C_{b1}$, hence making the test amplifier matched at 5.25GHz. When ($D_3D_2D_1$) = (011) and (111), C_B is expressed as Equations (a.7) and (a.8), hence making the test amplifier matched at 2.4GHz and 1.8GHz, respectively.

$$C_B = C_{b1} + C_{b2} \quad \text{(a7)}$$

$$C_B = C_{b1} + C_{b2} + C_{b3} \quad \text{(a8)}$$

Considering f_1=5.25GHz, f_2=2.4GHz and f_3=1.8GHz, to adjust input impedance of the test amplifier, we can make relationship expressed as Equations (a.9) to (a.11).

$$\omega_1 C_B = \omega_1 C_{b1} \quad \text{(a9)}$$

$$\omega_1 C_B = \omega_2 C_{b2} \quad \text{(a10)}$$

$$\omega_1 C_B = \omega_3 C_{b3} \quad \text{(a11)}$$

From these equations, C_{b1}, C_{b2} and C_{b3} can be expressed as

$$C_{b1} = \frac{\omega_1}{\omega_1} C_B = k_1 C_B = k_1 C_{b1} \quad \text{(a12)}$$

$$C_{b2} = \frac{\omega_1}{\omega_2} C_B = k_2 C_B = k_2 C_{b1} \quad \text{(a13)}$$

$$C_{b3} = \frac{\omega_1}{\omega_3} C_B = k_3 C_B = k_3 C_{b1} \quad \text{(a14)}$$

where k_1=5.25/5.25=1, k_2=5.25/2.4=2.1875 and k_3=5.25/1.8=2.9167.

Therefore, we obtain mathematical expression for C_B from Equations (a.7), (a.8) and (a.12) to (a.14).

$$C_B = k_1 D_1 C_{b1} + k_2 D_2 C_{b2} + k_3 D_3 C_{b3} = [k_1 D_1 + (k_2 - 1) D_2 + (k_3 - k_2) D_3] C_{b1} \quad \text{(a15)}$$

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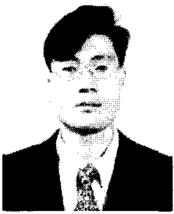

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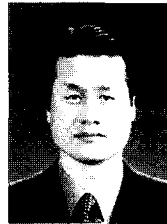

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