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Stress Dependence of Thermal Stability of Nickel Silicide for Nano MOSFETs

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Dependence of the thermal stability of nickel silicide on the film stress of inter layer dielectric (ILD) layer has been investigated in this study and silicon nitride (Si_3N_4) layer is used as an ILD layer. Nickel silicide was formed with a one-step rapid thermal process at 500 °C for 30 sec. 2000 Å thick Si_3N_4 layer was deposited using plasma enhanced chemical vapor deposition after the formation of Ni silicide and its stress was split from compressive stress to tensile stress by controlling the power of power sources. Stress level of each stress type was also split for thorough analysis. It is found that the thermal stability of nickel silicide strongly depends on the stress type as well as the stress level induced by the Si_3N_4 layer. In the case of high compressive stress, silicide agglomeration and its phase transformation from the low-resistivity nickel mono-silicide to the high-resistivity nickel di-silicide are retarded, and hence the thermal stability is obviously improved a lot. However, in the case of high tensile stress, the thermal stability shows the worst case among the stressed cases.

Keywords : Nickel silicide, Thermal stability, Silicon nitride, Mechanical stress, Nano MOSFETs

1. INTRODUCTION

Self-aligned-silicides (SALICIDEs) are inevitable for complementary metal oxide semiconductor field effect transistor (CMOSFET) to reduce the series resistance of gate, source and drain areas[1]. Recently, nickel mono-silicide (NiSi) has been considered as a viable candidate for contact material because of its low resistivity, relatively low formation temperature, no resistivity increase in narrow lines and smaller silicon consumption during silicidation[2]. However, poor thermal stability of the nickel silicide is a main weakness to be applied to nano-scale CMOSFET technology which needs high temperature processes after formation of the silicide[3]. To overcome this problem, many attempts such as ion implantation[4], application of alloying target materials [5-10] and deposition of capping layer[11,12] have been suggested.

As the device dimensions scale down to nano-scale regime, mobility variation induced by mechanical stress of various films has shown more pronounced effect on the device performance. Therefore, stress engineering or control of the mechanical stress of various films such as shallow trench isolation gap fill oxide layer, silicide blocking layer and inter layer dielectric (ILD) layer has attracted a lot of attention to improve the device performance of metal oxide semiconductor field effect transistors (MOSFET) and it is known that tensile stress improves n-type MOSFET and compressive stress improves p-type MOSFET, respectively[13]. Among the various oxide layers, stress of ILD layer has an effect on the silicide property because it is directly deposited on top of the silicide layer. Especially, Si_3N_4 layer on top of silicide is a must in a high density CMOS technology as an etch stop layer for formation of borderless contacts. Therefore, the stress of Si_3N_4 layer will directly affect the nickel silicide property as well as the device performance. However, there was little studies on the mechanical stress effect of ILD layer on the Ni silicide properties although the influences of stress on the

interfacial reactions of Ti and Ni metal thin films on Si [14] and stress evolution during silicide formation[15-17] have been studied.

In this paper, the dependence of the thermal stability of nickel silicide on the mechanical stress of Si_3N_4 layer is characterized in depth by varying the stress type from compressive to tensile stress. The stress level of each stress type is also split for thorough analysis of the dependence.

2. EXPERIMENTAL

A brief fabrication process flow is summarized in Fig. 1. P-type Si (100) wafer was cleaned and dipped in a HF solution to remove the native oxide. Then, 10 nm thick Ni layer was deposited by RF magnetron sputtering system with a base pressure of 5 × 10^{-7} Torr and a working pressure of 1 mTorr. For the formation of Ni silicide, a one-step rapid thermal process (RTP) was carried out at 500 °C for 30 sec. Un-reacted metal was selectively removed using a mixture of H_2SO_4 and H_2O_2 with the volume ratio of 4:1. Then, 2000 Å thick Si_3N_4 layer was deposited by plasma enhanced chemical vapor deposition (PECVD) using a standard recipe with a mixture of SiH_4 and NH_3. The film stress of Si_3N_4 was split from tensile to compressive stress by controlling the RF power of PECVD as will be detailed later. Reference sample without the Si_3N_4 layer was also fabricated for comparison. Finally, to evaluate the thermal stability of silicides, samples were furnace annealed in N_2 ambient at three different high temperatures for 30 min (post-silicidation annealing in short). Wet etching of the Si_3N_4 layer was carried out to measure the variation of sheet resistance of Ni silicide using H_3PO_4 solution at 150 °C.

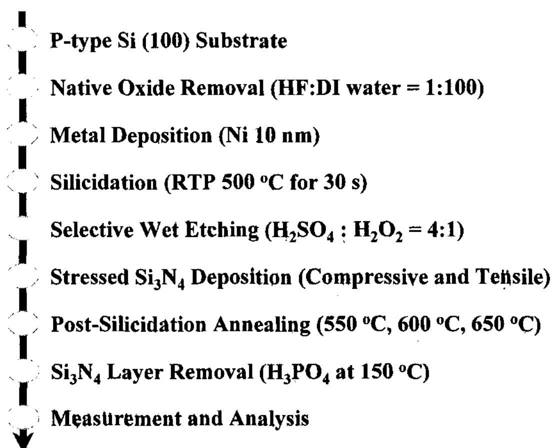

Fig. 1. Key process flow for experiments.

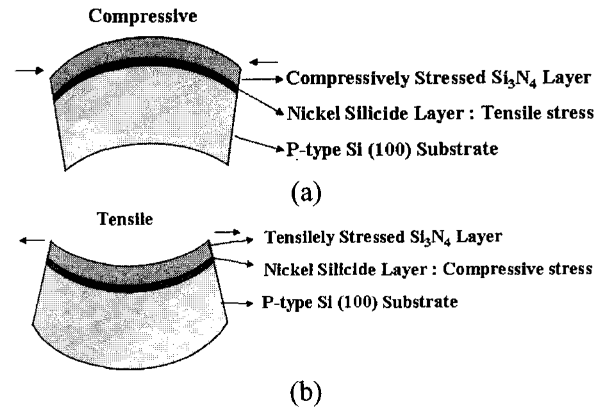

Fig. 2. Schematic diagrams of the (a) compressively and (b) tensilely stressed samples.

Table 1. The samples classification for experiments.

Sample	Stress Type	Stress Magnitude
A	Reference	-
B	High Compressive	-600 MPa
C	Low Compressive	-110 MPa
D	High Tensile	580 MPa
E	Low Tensile	25 MPa

Figure 2 shows the schematic diagrams of the samples with compressive and tensile stresses, respectively. Wafer curvature measurements were performed using FSM500TC (Frontier Semiconductor, Inc.), which utilizes a scanning laser technique. Film stress was calculated from curvature measurements using the well-known Stoney's equation[18] for biaxial film stress, σ_f: $\sigma_f = (k - k_0)\left[E_s/(1-v_s)\right]\left(t_s^2/6t_f\right)$, where k and k_0 are curvatures of the film-substrate system and bare substrate, respectively, E_s is the substrate Young's modulus, v_s is the substrate Poisson's ratio, and t is thickness with subscripts appropriate to the film, f, and substrate, s. The biaxial modulus, $E_s/(1-v_s)$, of (100) silicon is 180.5 GPa[19]. The stress type and magnitude of the Si_3N_4 films were varied with the control of the radio frequency (RF) operation power of high frequency (HF) power source with a frequency of 13.56 MHz and low frequency (LF) power source with a frequency of 250 kHz, respectively. The sum of operation powers of HF and LF power sources is kept to be 1000 Watt. As the operation power of LF power source was adjusted from 900 to 500 Watt and from 100 to 500 Watt of the HF power source, the magnitude of compressive stress was varied from 600 to 110 MPa. The tensile stress of Si_3N_4 film was split from 25 to 580 MPa with decreasing the RF power of LF power source from 400 to 0 Watt and increasing power of HF power source from 600 to 1000 Watt, respectively. The classification of samples with stress split is summarized in Table 1.

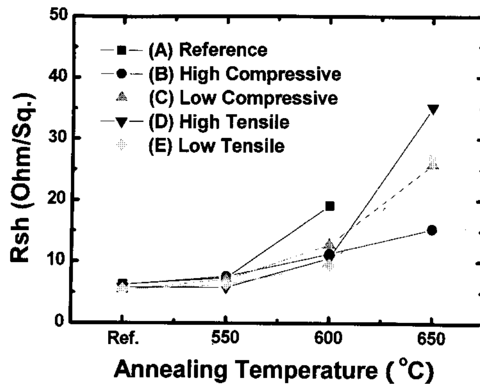

Fig. 3. Comparison of sheet resistance of silicide between with and without stressed Si_3N_4 layer as a function of post-silicidation annealing temperature.

Sheet resistance was measured using conventional four point probe method. The uniformity of the silicide was observed using field emission scanning electron microscopy (FESEM, Jeonju branch of Korea Basic Science Institute (KBSI), model: Hitach S-4700). Thin-film X-ray diffraction (XRD) and secondary ion mass spectrometer (SIMS) analyses were performed to investigate phase identification and depth profile of Ni, respectively.

3. RESULTS AND DISCUSSION

After post-silicidation annealing, the sheet resistance window as a function of post-silicidation annealing temperature is shown in Fig. 3. Little difference of sheet resistance between the stressed and reference samples is observed until 550 °C. However, the sheet resistance of sample A or reference sample increases abruptly from 600 °C and becomes immeasurable at 650 °C, while the other samples with stressed Si_3N_4 layer show more stable sheet resistance than the reference. Among the stressed samples, the compressive stress case shows smaller sheet resistance than the tensile stress one and the higher compressive stress results in the lower sheet resistance. Among the tensile stress cases, the higher tensile stress shows higher sheet resistance than the lower stress case.

Figure 4 presents cross-sectional FESEM images of samples after post-silicidation annealing at 650 °C for 30 min. Because the etching rate of Si_3N_4 layers with different stress type and level is not identical, the etching time of each sample is carefully controlled but some samples show thin remained Si_3N_4 layer, as can be seen in Figs. 4(b), (c) and (e). However, there was no problem in measuring sheet resistance. The best cross-sectional profile of silicide layer is found in the high compressively stressed silicide (sample B), as shown in Fig. 4(b), which is in good agreement with the low sheet resistance in Fig. 3. However, the agglomerations can be observed in sample A, C, D and E, as shown in Figs. 4(a), (c), (d) and (e). Silicide with lower compressive stress shows less agglomeration than tensilely stressed silicides. Therefore, it can be said that the lower sheet resistance and

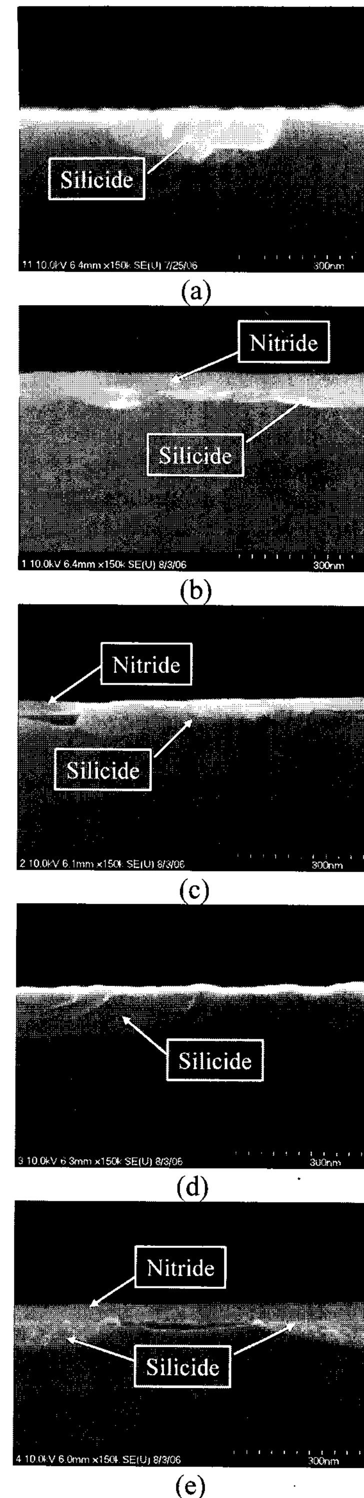

Fig. 4. FESEM images of nickel silicide (a) reference, (b) high compressive, (c) low compressive, (d) high tensile, and (e) low tensile cases after post-silicidation annealing at 650 °C for 30 min in N_2 ambient.

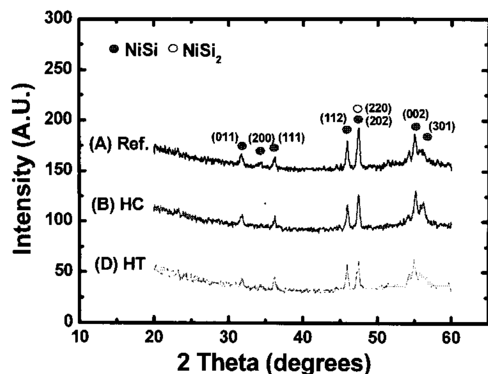

Fig. 5. XRD spectra of nickel silicide after post-silicidation annealing at 650 °C for 30 min in N_2 ambient.

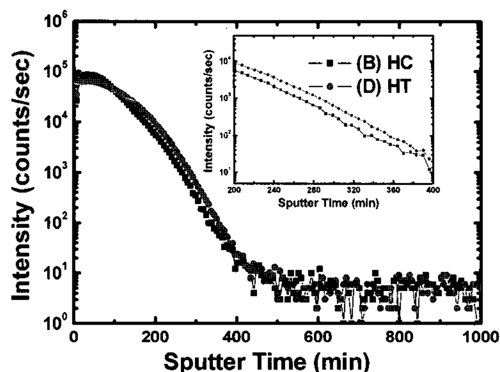

Fig. 6. SIMS depth profiles of Ni for sample B and D after post-silicidation annealing at 650 °C for 30 min in N_2 ambient. The inset shows the partial enlarged figure.

better cross-sectional profile of compressive case is owing to the retardation of agglomeration by the compressively stressed Si_3N_4 layer.

XRD analyses of samples after post-silicidation annealing at 650 °C were performed to characterize the phase change by the Si_3N_4 layer and the difference between samples, as shown in Fig. 5. The low-resistivity NiSi phase peaks of (011), (200), (111), (112), (202), (002) and (301) appear in all samples and there is little difference between samples. However, the high-resistivity $NiSi_2$ phase peak also appears in all samples even though there is some overlap between the NiSi (202) diffraction peak with the $NiSi_2$ (220) diffraction peak. By taking into account of sheet resistance and XRD analysis, it can not be said that the lowest sheet resistance of sample B is owing to the retardation of phase transformation from NiSi to $NiSi_2$.

The SIMS depth profiles of Ni for high compressively stressed sample B and high tensile stressed sample D after post-silicidation annealing at 650 °C are reported in Fig. 6. Although the remarkable difference between sample B and sample D has not been observed, sample B shows less diffusion of Ni into substrate than sample D, as clearly shown in the inset in Fig. 6. Therefore, it can be concluded that the improved thermal stability of high compressive case is mainly owing to the enhanced retardation of silicide agglomeration during the post-silicidation annealing.

4. CONCLUSION

Dependence of the thermal stability of nickel silicide on the stress of ILD Si_3N_4 layer is systematically analyzed with detailed split of film stress of Si_3N_4 layer. It is found that Ni silicide with compressive stress shows a lower sheet resistance and less agglomeration than silicide with tensile stress and higher compressive stress is desirable for the better silicide properties. It is also shown that the retardation of silicide agglomeration by the compressive stress results in a lower sheet resistance and uniform silicide profile. Therefore, stress of ILD layer should be carefully considered to prevent the degradation of Ni silicide for the nano-scale strained-Si CMOS technology.

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