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Pulse-Grouping Control Method for High power Density DC/DC Converters

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ABSTRACT

The proposed method offers an improved DC/DC converter scheme to increase power density. It is based on half-bridge topology with newly introduced pulse-grouping control method, which helps to reduce the transformer size and the volume of semiconductor devices maintaining high efficiency. Test results with 85W(18.5V/4.6A) design shows that the measured efficiency is 93.5% with power density of 36W/in^3.

Key Words : Half-bridge, DC/DC converter, Synchronous rectifier

1. INTRODUCTION

As the world population grows and the overall energy consumption increases, well-developed countries have become increasingly concerned with the future availability of energy and have made appropriate energy policies for energy use[1, 2]. One approach is reducing energy consumption by using more energy efficient electrical equipments. As the IT industry is drastically expanded, the devices such as notebook computer, cellular phone, and computer monitors that use various adaptors are popularized recently. Accordingly, developing high efficient adaptors gives an obvious opportunity for energy saving. In addition, as many consumers prefer small size devices with many functions, manufacturers require high power density adaptors[3]. Conventional adaptors have developed based on flyback topology but it is no longer a useful topology in the aspect of size and efficiency despite of its simple structure[4]. In this letter, a high power density DC/DC converter for adaptor applications is suggested. The proposed circuit is based on half-bridge topology with pulse-grouping control that output voltage can be regulated by adjusting the off-time between pulse groups, which makes it possible to improve the efficiency and power density. Test results with 85W(18.5V/4.6A) converter with 400V input voltage show that the measured efficiency is 93.5% with 36W/in^3 of power density including control circuitry and input bulk capacitor.

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2. PULSE-GROUPING CONTROL METHOD

To improve the power density and efficiency, there are several obstacles such as magnetic component size, semiconductor device loss, and their package size. The unregulated bus converter concept[4] suggests the optimization of the converter design under several restricted conditions such as fixed low input voltage, no control loop and fixed duty cycle of 50%. Using this concept, 500W/in^3 of power density is reported in 200W converter with fixed 60V input voltage. Although the output voltage is not regulated, this is good concept in the aspect of power density increase. To overcome this disadvantage while maintaining the unregulated bus converter concept, it is necessary to find some control variable. Fig. 1 shows the gating signal of newly suggested pulse-grouping control method based on half-bridge topology. This topology is predominant over other topologies except for full-bridge, that is most complex and not suitable for low power applications, in the aspect of transformer utilization, device voltage ratings and filter inductor design. Thus the proposed DC/DC converter

has been developed based on half-bridge topology. During gating pulses are generated, the converter operates with fixed duty of 50%, whose operational characteristics are similar to the unregulated bus converter and the output voltage can be regulated using off-time T_{off} between grouping pulses as control variable. Because the output rectifier voltage stress is managed to be constant voltage according to load variations, voltage-ratings of synchronous rectifiers can be optimized. In addition, operation frequency of transformer is several times higher than control frequency, so the transformer size that is a critical obstacle to increase the power density can be reduced. This pulse-grouping control method gives additional advantage that switching number of switches becomes to be reduced as the load becomes light. This may improve power consumption and efficiency in light load conditions.

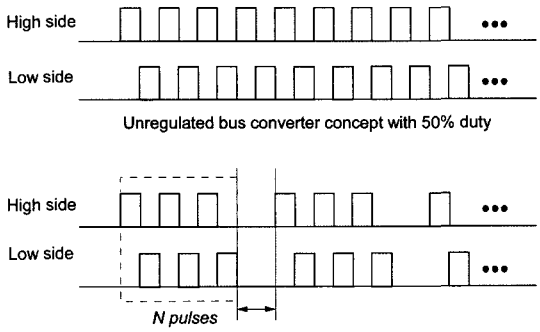

Fig. 1. Pulse grouping control method.

3. PROPOSED CONVERTER

Fig. 2 is the proposed DC/DC converter and Fig. 3 is its switching waveforms. The converter is based on

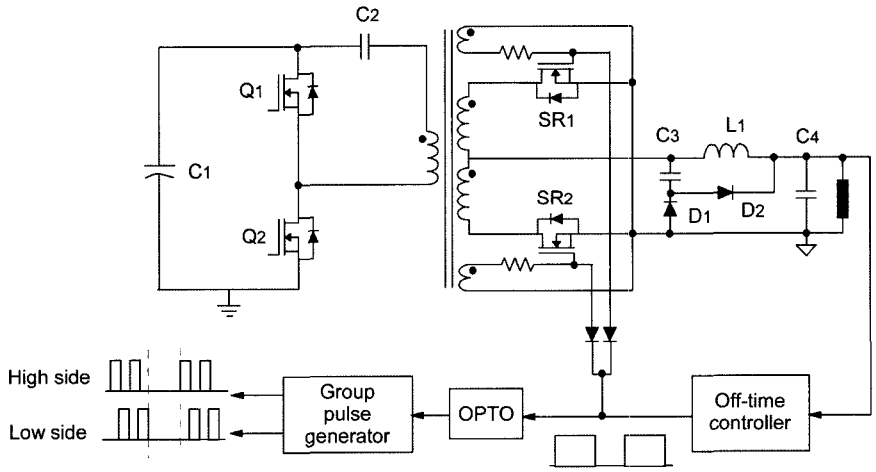

Fig. 2. Proposed converter with pulse-grouping control method.

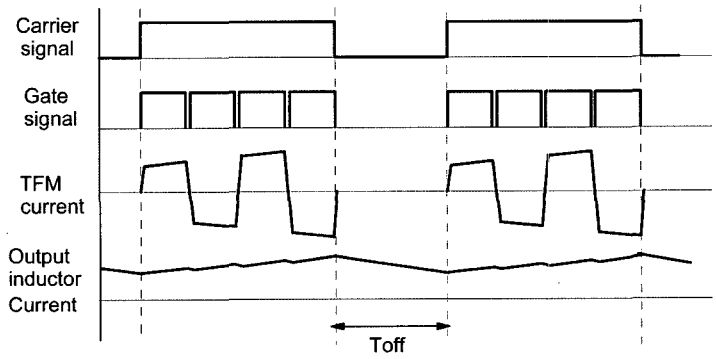

Fig. 3. Switching waveforms with 4 pulses in one group.

half-bridge topology with center-tapped transformer and DC-blocking capacitor to reduce the device count and volume. Voltage-driven synchronous rectifiers are used in the output stage. The SR voltage stress can be constantly maintained as V_i/n regardless of load condition because the operating duty is always 50% and it makes the DC-blocking capacitor voltage fixed as half of the input voltage. It results that low voltage-rating FETs with low R_{ON} and small package can be used for synchronous rectifiers, which increase the efficiency and power density. D_1, D_2, and C_3 located in the output stage are snubber circuit for alleviating the voltage ringing caused by transformer leakage inductance. Controller is composed of three blocks of off-time controller, optocoupler, and group pulse generator. Off-time controller generates carrier pulses to determine pulse number and off-time between pulse groups with output voltage information. This carrier signal transfers to the group pulse generator through optocoupler. The group pulse generator provides pulses with 50% duty to main FETs of Q_1 and Q_2. Synchronous rectifiers may be abnormally turned on during off-time due to the resonance of transformer leakage inductance and parasitic capacitances including FET output capacitance. Carrier signal can be used to avoid this abnormal operation during off-time by removing the gate signals of synchronous rectifiers as shown in Fig. 2. Fig. 3 is the switching waveform of transformer primary current and output inductor current by assuming one group has 4 pulses. T_{string} is the time during which pulses are generated. Because the converter is controlled by adjusting T_{off}, the effective duty D_{eff} can be defined by $T_{sting}/(T_{string}+T_{off})$ like PWM control. With this variable, the input-to-output relationship can be derived as follows:

$$V_o = \frac{V_{in}/2}{n}\frac{T_{srting}}{T_{srting}+T_{off}} \quad (1)$$

Too small pulse group is not desirable in the aspect of efficiency and EMI because the first pulse is always hard-switching operation. On the other hand, the output inductor is governed by the carrier signal frequency while operating frequency of transformer is pulse frequency. Thus it is necessary to compromise between switching loss and inductor size to determine pulse number.

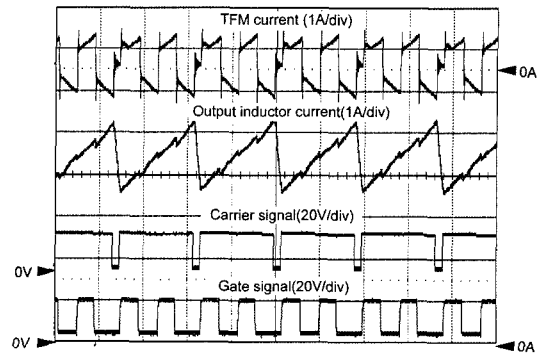

Fig. 4. Experimental waveforms.

4. EXPERIMENTAL RESULTS

The proposed converter has been verified with 85W(V_{in}=400V, V_o=18.5V) converter that is used as DC/DC stage of adaptor. SPD03N50 (560V/3.2A) is used for Q_1 and Q_2 and SR switches are implemented with IRF7855 (60V/9.4 mΩ). This FET has very small package of SO-8. Off-time controller is built with fixed on-time control IC of FAN5037 and 50% duty drive of IR2085 and floating gate driver of IR2117 are used for group pulse generator. The size of the prototype converter is 5cm×4cm×2cm (L×W×H) and the calculated power density is 36W/in^3. The operating frequency is designed as 120kHz and the grouping pulse number is four by compromising between efficiency and output inductor size. With the selected parameters, transformer and inductor can be implemented with PQ2016 and toroidal cores. Fig. 4 is the measured waveforms at full load output. With this designed converter, 85W AC/DC converter has been designed and tested by installing BCM Boost stage as PFC preregulator. The total size including input filter can be obtained as 7.5cm×7.5cm×2.5cm and the efficiency is 89.73% at 115V$_{rms}$ input. The measured efficiency including preregulator stage under load variation depicted in Fig. 5. Because the efficiency of preregulator is measured as 95%, that of the proposed converter has 93.5% at maximum load condition. It also show low no load power consump-

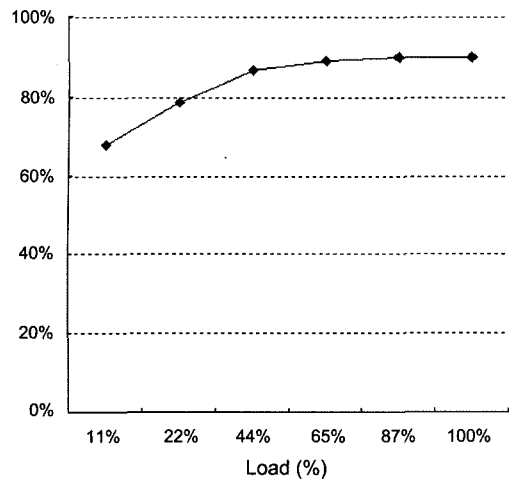

Fig. 5. Measured efficiency at $110V_{rms}$ grouping control method.

tion of about 0.5W with the help of pulse-grouping control method.

5. CONCLUSIONS

The proposed method offers a high power density DC/DC converter based on half-bridge topology with the pulse-grouping control method. Transformer size can be reduced, operating it with a higher frequency than control frequency and the fixed 50% duty operation improves the efficiency by making it possible to select semiconductor devices with optimal ratings. Test results with 85W design shows that the measured efficiency is 93.5% with $36W/in^3$ of power density. It shows the feasibility of the proposed converter as high power density adaptors.

Acknowledgement

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