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Control of Input Series Output Parallel Connected DC-DC Converters

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ABSTRACT

Equal rating DC-DC converter modules can be connected in series at the input for circuits requiring higher input voltages and in parallel at the output for circuits requiring higher output currents. Since the converter modules may not be practically identical, closed loop control has to ensure that each module equally shares the total input voltage and the load current. A control scheme consisting of a common output voltage loop, individual inner current loops and individual input voltage loops have been designed in this work to achieve input voltage and load current sharing as well as load voltage regulation under supply and load disturbances. The output voltage loop provides the basic reference for the inner current loops, which are also modified by the respective input voltage loops. The average of the converter input voltages, which is dynamically varying, is chosen as the reference for input voltage loops. This choice of reference eliminates interaction among different control loops. Type II compensators and Fuzzy Logic Controllers (FLCs) are designed and compared through MATLAB based simulation and FLC is found to be satisfactory. Hence TMS320F2407A DSP based FLC is implemented and the results are presented which prove the superiority of the FLC developed for this research.

Keywords: Fuzzy control, DC-DC converter,TMS320F207A DSP

1. Introduction

Power supply systems have to be easily reconfigured to support varying input-output specifications. In such architecture low voltage and low current rated DC-DC converters must be connected in any combination, series and/or parallel at the input as well as the output , to realize any input-output specifications[1-6]. Two identical DC-DC converters each rated for half the total load and half the input voltage are connected in series at the input and in parallel at the output in the present work as in Fig.1. A three-loop control scheme (Fig.2) is designed and verified through MATLAB based simulation and hardware implementation. The results are presented.

2. Three Loop Control Scheme

The control strategy developed [3,4] to ensure equal sharing of input voltage and output current has individual inner current loops, a common output voltage loop and individual inner voltage loops (Fig.2). For stable operation of the Input Series Output Parallel (ISOP) connected converters, the necessary requirement

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is the input voltage sharing controller. If the series connected converters use a common output voltage loop providing the current reference to both converters without the input voltage sharing controller, equal sharing of load current is not achieved as shown in the simulated waveforms in Fig.3 and sluggish settling of load voltage as in Fig.4 .

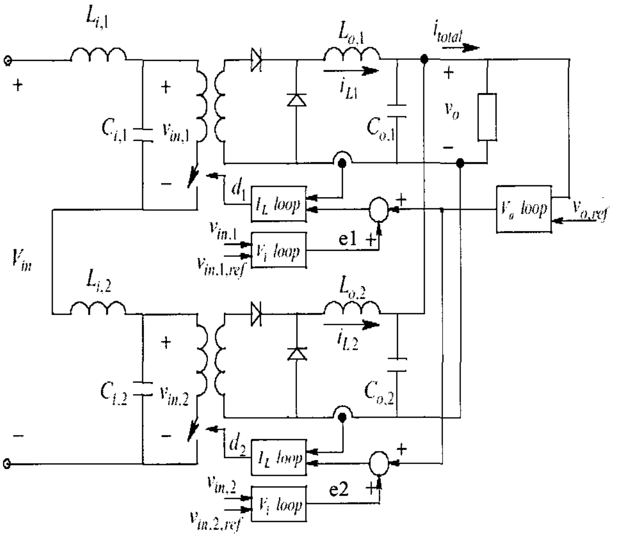

Fig. 1 Series parallel connection of two forward

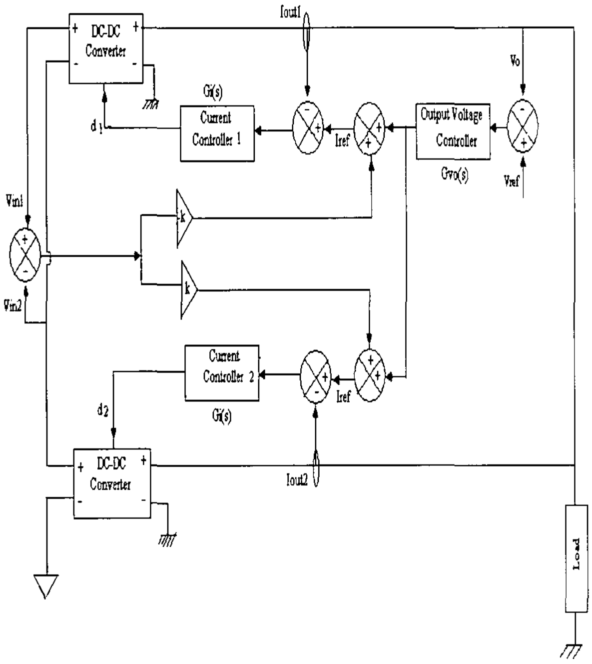

Fig. 2 Control scheme for ISOP connected DC-DC converters

In spite of the common current reference, *Iout1* approaches 8 Amps and *Iout2* approaches 0 Amps as seen in Fig.3. Hence, an input voltage sharing control loop adjusts the duty ratios (d_1,d_2) of the individual converters depending on the error in input voltage sharing, which automatically ensures load current sharing.Fig.5 shows the equally shared current output of each ISOP connected forward DC-DC converter with the input voltage sharing controller and with the fuzzy/compensator type current and voltage loop controllers. The inner voltage loop generates an error signal e_i $(i=1, 2)$ proportional to the difference between the actual input voltage across the respective converter and the reference voltage Vin_{ref} with

$$Vin_{ref} = \frac{Vin1 + Vin2}{2} \tag{1}$$

$$e_i = K(Vin1 - Vin2) \tag{2}$$

where $k = -0.5, 0.5$ are the gains of the proportional type inner voltage loops.

The outer voltage loop generates a signal based on the error in the output voltage. The signals from the above two voltage loops are added to form the current reference *Iref* to each current loop. In this work, *Gvo(s)* and *Gi(s)* are (i) type II compensators (Table 1) and (ii) fuzzy

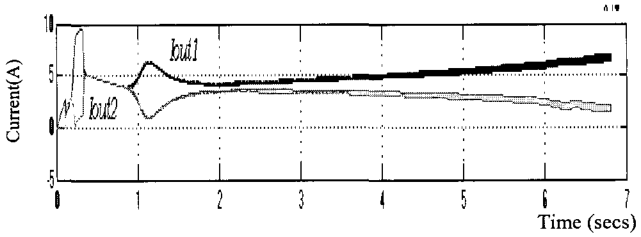

Fig. 3 Current output of each ISOP connected forward DC-DC converter without input voltage sharing controller and with fuzzy/compensator type current and voltage loop controllers

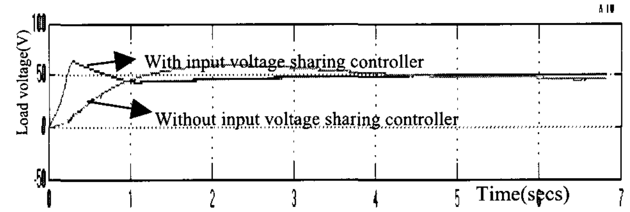

Fig. 4 Load voltage of ISOP connected forward converters

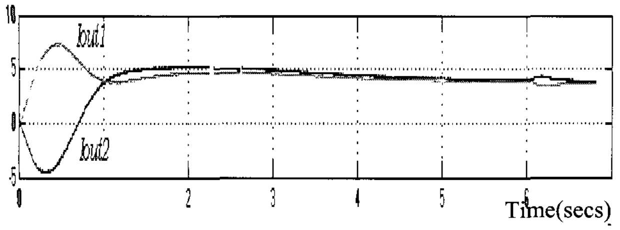

Fig. 5 Current output of each ISOP connected forward DC-DC converter with input voltage sharing controller and with fuzzy/compensator type current and voltage loop controllers

controllers (Table 2) for the outer voltage loop and inner current loops. Seven Mamdani type triangular input and output membership functions with centroid method of defuzzification are employed for PI like FLCs developed in this work. The inputs to the fuzzy controller are the error (e)and change in error (ce). ce can be defined as

$$ce = e_k - e_{k-1} \tag{3}$$

where subscript k denotes the sampling instants. The updated duty cycles d_{1k} , d_{2k} are the output of FLCs.The values of e, ce and d_{ik} are normalized to [-1,1].

3. Simulation Results

The transfer function model of the single forward DC-DC converter is obtained using small signal modeling and is used in the design of compensators and closed loop control scheme. MATLAB based simulation results of ISOP connected forward DC-DC converters are discussed below. Fig. 5 shows the current output of each converter with the input voltage sharing controller.

Fig.6 shows the block diagram of compensators/fuzzy logic controllers for a single forward converter.Fig.7 shows the current sharing among individual converters with compensators and FLCs under disturbances in supply V_{in1} from $80V$ to $75V$ at $t=0.05$ sec and load disturbance from 6Ω to 12Ω at $t=0.1sec$. Fig.8 shows the zoomed start-up transients of load current with compensator and fuzzy logic controller. From Fig.7 and Fig.8,it is found that supply disturbance is totally rejected by the fuzzy controller without any transient although the load current with this controller has highly oscillatory start-up transient.

Table 2 FAM table for ISOP connected forward DC-DC converters

ce / e	NB	NM	NS	ZE	PS	PM	PB
NB	NB	NB	NB	NB	NM	NS	ZE
NM	NB	NB	NM	NM	NS	ZE	PS
NS	NB	NM	NS	NS	ZE	PS	PM
ZE	NM	NM	NS	ZE	PS	PM	PB
PS	NM	NS	ZE	PS	PS	PM	PB
PM	NS	ZE	PS	PM	PM	PB	PB
PB	ZE	PS	PM	PB	PB	PB	PB

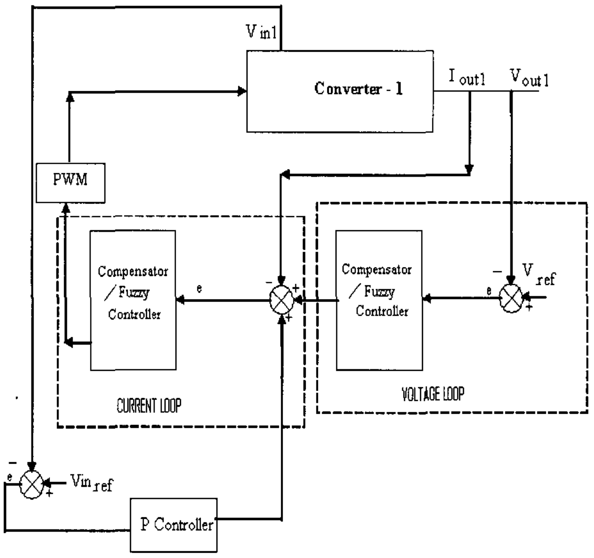

Fig. 6 Block diagram of compensators/fuzzy logic controllers for a single forward converter

Table 1 Type II compensators for ISOP connected DC-DC converters

Voltage compensator $Gv_o(s)$	Current compensator $G_i(s)$
$\frac{s+6.45e^4}{s^2+1.19e^5 s}$	$\frac{s+2.186e^5}{s^2+8.859e^4 s}$

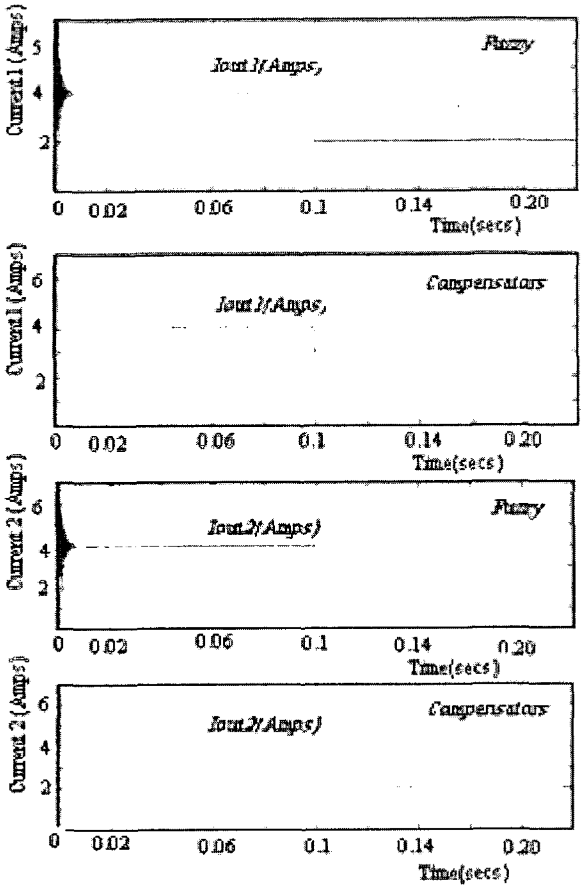

Fig. 7 Current sharing among each converter using FLCs and compensators under line and load disturbances

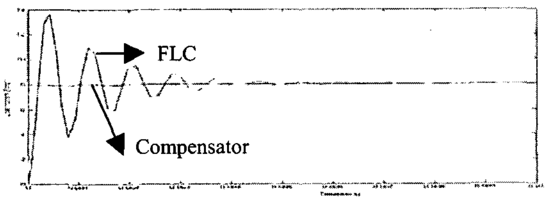

Fig. 8 Zoomed start-up transients of load current

Table 3 Results of ISOP connected DC-DC converters for gradual line disturbances with nominal load (R_L=5Ω) with FLC

V_{in} (volts)	V_{in1} (volts)	V_{in2} (volts)	I_{out1} (amps)	I_{out2} (amps)	V_{out} (volts)
25	12.42	12.53	0.48	0.48	5.02
27	13.42	13.56	0.47	0.47	5.02
30	14.9	15.06	0.47	0.47	5.02

Table 4 Results of ISOP connected DC-DC converters for gradual load disturbances with supply voltage V_{in} =27V with FLC

Load R_L (Ω)	V_{in1} (volts)	V_{in2} (volts)	I_{out1} (amps)	I_{out2} (amps)	V_{out} (volts)
1000	13.42	13.56	0.25	0.25	5.02
5	13.42	13.56	0.47	0.47	5.02

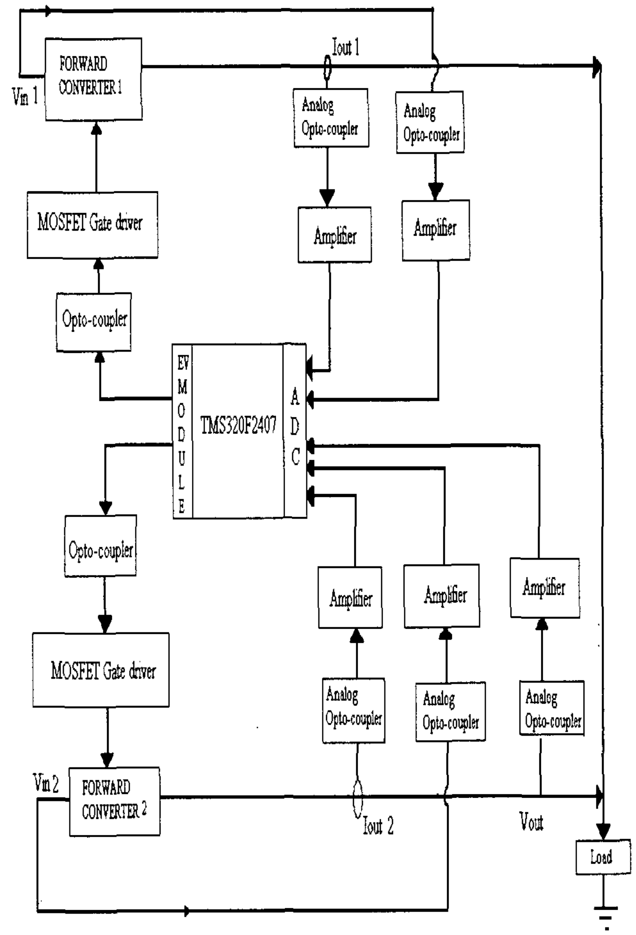

Fig. 9 Closed loop control scheme for ISOP connected forward converter using TMS320F2407A

4. TMS320F2407A DSP Based Control of ISOP Connected Forward Converters

Since it is inferred from previous sections that FLC performs satisfactorily for ISOP connected forward converters, it is implemented [2] using Texas Instrument's TMS320F2407A DSP. Since the DSP contains the core processor and the control-oriented peripherals integrated into a single chip, it is very compact and is a cost effective digital control system.

The conversion time of on-chip ADC which has a built-in sample and hold is 375 ns.The highly paralleled architecture and efficient instruction set provides speed of 40 Million Instruction Per Sec (MIPS). Hence this DSP is selected as a control tool for the present work. For total control of the series-parallel connection of forward converters using a DSP, two digital outputs and five analog inputs are required. The DSP provides two PWM signals (d_1, d_2) to the switching device of each converter. The driver IR2110 is used to strengthen the pulses to the gate of the MOSFET.DSP receives digitized information on output voltage *(Vout)*, input voltages *(Vin1* and *Vin2)* and output currents (*Iout1 and Iout2*) of each converter through ADC.Analog opto-couplers HCPL7840 isolate the DSP from the converters. The DSP compares the actual output voltage and converter currents with the respective reference voltage and reference current and computes the resultant error. This error (*e*) is processed by the fuzzy control algorithm in the DSP to suitably adjust the duty ratio d_1 and d_2 of the PWM signals applied to the gates of the MOSFETs. The range of *e,ce* (-1 to 0 to 1) is fixed as (0 -3EEH-7FEH) and range of δdi_k (-1 to 0 to 1) is fixed as (0-0FH-1EH) for DSP based FLC .Fig.9 shows the block diagram of real time implementation of TMS320F2407A DSP based P controllers for input voltage sharing and FLCs for load current sharing and voltage regulation of ISOP connected forward converters. The experimental results are observed on a 20MHz digital storage oscilloscope.

Fig.10 shows the steady state and transient behavior of output current of each converter under sudden load disturbance from 10Ω to 5Ω at *t=0.6 secs* and from 5Ω to 10Ω at *t=1.16secs* for 5V load voltage. Fig.11 shows the regulated output voltage for sudden change in supply from 27V to 30V at *t=0.6 secs* and vice versa change at *t=1.4 secs* and the next figure displays the output voltage for sudden load disturbances from 10Ω to 5Ω at *t=0.45* secs and from 5Ω to 10Ω at *t=1.25secs*.Tables 3 and 4 show the corresponding output voltage regulation and input voltage and load current sharing under gradual line and load disturbances. The above results validate the superiority of FLC developed for this research. V_{in} and V_{out} (after scaling down suitably the corresponding simulation values in view of laboratory constraints) for DSP based implementation are 27*V*, 5*V* respectively. Table 5 shows the specifications for one of the forward converters used in simulation.

5. Conclusion

Since it is inferred from simulation results that FLC performs satisfactorily, DSP based implementation of FLC alone is carried out in this work. Experimental results show that the proposed FLCs are capable of regulating the output voltage and providing equal sharing of input voltage and load current among identical converters under line and load disturbances. DSP based FLCs are found to perform satisfactorily with quick disturbance rejection. These experimental results prove the validity of DSP based fuzzy logic controllers.

Table 5 Specifications for one of the forward converters in simulation

Parameters	Values
Range of input voltage Vin	80V-100V
Nominal output voltage Vout	48V
Nominal converter current	4A
Switching frequency	170KHz
Inductor L	115μH
Capacitor C	150μF
Switching device	N-Channel MOSFET
Nominal load	6Ω

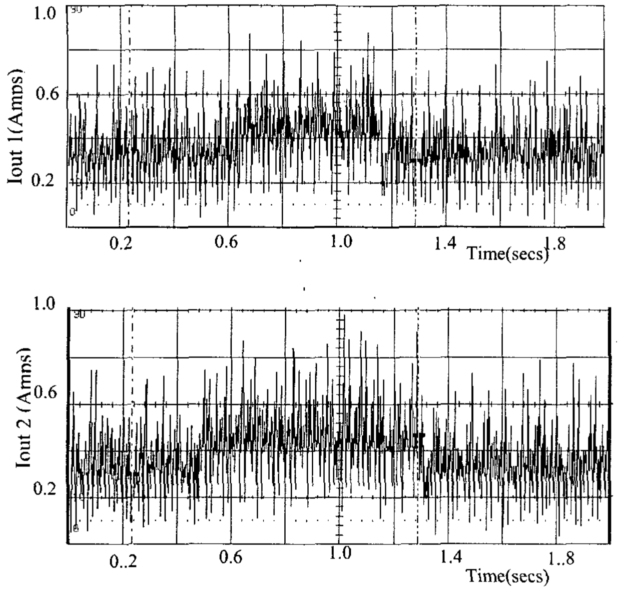

Fig. 10 Steady state and transient behaviours of the converter currents with sudden load disturbances

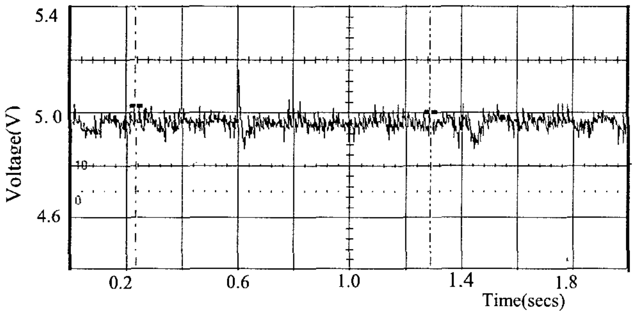

Fig. 11 Output voltage under sudden line disturbances

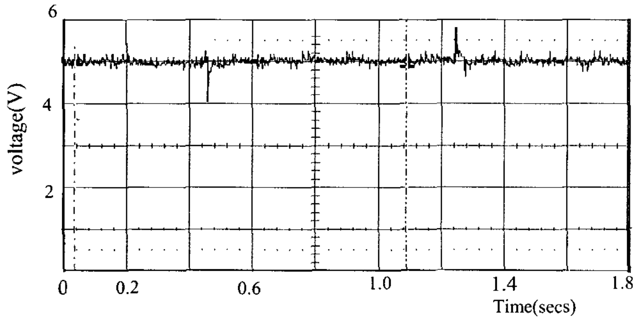

Fig. 12 Output voltage under sudden load disturbances

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