A High Performance Harmonic Mixer Using a plastic packaged device

Jae-hyun Kim* · Min-ho Go* · Hyo-dal Park* · Hyun-sik Shin**

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ABSTRACT

In this paper, a third-order harmonic mixer is designed using frequency multiplier theory for the Ka-band. The gate bias voltage is selected by frequency multiplier theory to maximize the third-order harmonic element ofthe fundamental LO frequency in the proposed mixer. The designed mixer has a gate mixer structure composed of a gate terminal input for the fundamental local signal (f_{LO}), RF signal (f_{RF}) and a drain terminal output for the harmonic frequency ($3f_{LO}$-f_{RF}) respectively. The Ka-band harmonic mixer is designed and fabricated using a commercial GaAs MESFET device with a plastic package. The proposed mixer will provide a solution for the problems found in the high cost, complex circuitry in a conventional Ka-band mixer. The 33.5 GHz harmonic mixer has a -10 dB conversion gain by pumping 11.5 GHz LO with a +5 dBm level.

Keywords

Harmonic, High Order, Mixer, Plastic Package.

I. Introduction

Over the last ten years, there has been an unprecedented growth in the number of systems that use the microwave and millimeter wave bands. The design parameters, such as low cost, high performance and reproducibility, are important considerations to design in microwave and millimeter wave systems[1]. The SHP(Sub-Harmonically Pumped) mixer, using an anti-parallel diode, has been used in the microwave and millimeter bands because of the advantage of low LO frequency, low spurious response, and noise suppression. But many sub-harmonic mixers, with an anti-parallel diode, were used and bonded to the circuit using silver epoxy[2][3] or were fabricated using a MMIC realization[4] resulting in higher cost and less reproducibility. Compared with conventional mixers, with an anti-parallel diode, SHP mixers using a active device which have similar SHP mixer properties as their diode counterparts have been developed, where two active devices are pumped in anti-phase at half of the LO frequency. The active SHP mixers, with anti-phase LO input[5], have a disadvantage of larger size, higher cost, and less reproducibility in their MMIC and Hybrid realization.

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In this paper, a Ka-band harmonic mixer, with a plastic packaged active device, is proposed to overcome these disadvantages of previous reported harmonic mixers. This harmonic mixer designis based on the multiplier theory that

there is a bias point to maximize a specific harmonic order with respect to a fundamental LO frequency. This can get the high-order mixing element ($f_{RF}\pm3f_{LO}$) to be greater than other mixing elements, pumping a RF frequency (f_{RF}) and LO frequency (f_{LO}), because of the bias voltage for the maximum third-order harmonic element ($3f_{LO}$).

The proposed harmonic mixer described in this paper offers several advantages over that of conventional SHP(Sub-Harmonically Pumped) mixers or high-order harmonic mixers. Similar to using a commercialGaAs MESFET, it gives economical cost and good efficiency of production. In addition, the proposed mixer has an additional advantage of small size because it does not use an additional phase shift circuit. The paper is organized as follows. SectionⅡ covers the design procedure of the harmonic mixer. The fabrication and performance of the proposed mixer and conclusion are discussed in section Ⅲ and Ⅳ.

Ⅱ. Harmonic mixer design

1. Bias selection based on multiplier operation

The major nonlinearities inthe FET causing harmonic generation are : 1) the gate-source and gate-drain nonlinear capacitors, C_{gs} and C_{gd}, which represent the gate-junction depletion layer capacitance; 2) the drain current I_{ds}' nonlinearity, which arises when the current is clipped when Vgs swings below pinch-off and/or swing positive to cause the gate diode, represented by R_{gs}, to conduct; 3) the nonlinearity of the V_{gs}-I_{ds}'transfer characteristics, which in the present instance is assumed to be quadric, but in practice is more complex ; and 4) the output conductance nonlinearity. But the drain clipping is the most impressive effect on the harmonic generation as compared with to others' nonlinear elements[6][7].

An even harmonic occurs when the output current or output voltage's waveform is distorted asymmetrically. On the other hand, an odd harmonic occurs when the output waveform is distortedsymmetrically to positive peak. Those effects are controlled by bias or drain termination.

The gate bias and gate input signal are selected to maximize the output level of the desired harmonic element by an approximation relating the harmonic drain current to the FET conduction angle. The harmonic drain current can be represented as a Fourier series expansion as a function of conduction angle and can be written as Equation (1) [8].

$$I_{dc} \approx I_{\max} \frac{2\theta}{\pi^2} \quad (1)$$

Where $I_N$is the drain current for the n^{th}harmonic, I_{dc} is the average of the drain current, $I_{max}$is the maximum drain current, and 2Θ is the conduction angle. From Equation (1), Fig. 1 shows harmonic output current as a function of conduction angle.

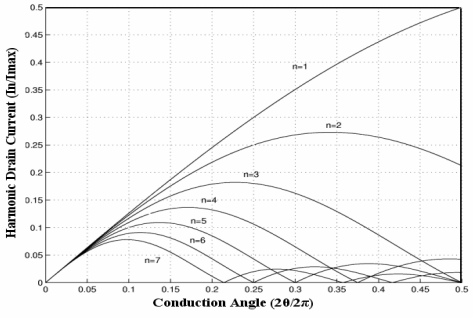


Fig. 1 Normalized harmonic current as a function of the conduction angle.

Conduction angle should be chosen to give high I_n

in order to maximize the desired harmonic output power. The optimum conduction angle is approximately $2\Theta = 0.23$ for the maximum third-order harmonic form Fig.1. However, This conduction angle equal to C class-bias conduction is not proper because the input matching is difficult and diode avalanche in the drain-gate is occurred when the gate has high minus voltage. Thus, to generate at the output a signal waveform rich with the desired third harmonic, biasing the device in a A-class and overdriving it until there is a clipping due to pinch-off on the negative swing and due to gate conduction on the positive swing [9].

Fig. 2 shows the output power level of a fundamental (f_{LO}), second harmonic ($2f_{LO}$) and third harmonic ($3f_{LO}$) element of a local signal by adjusting gate bias voltage for the applied LO signal. From Fig. 2, there is a specific gate bias voltage where the third harmonic is the maximum.

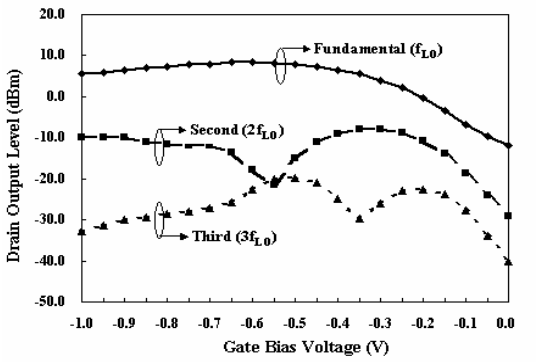
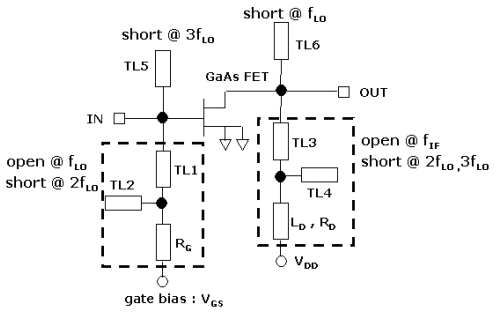


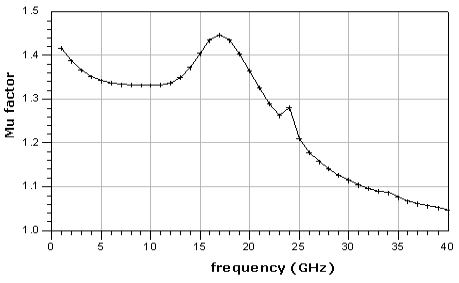
Fig. 2 Output harmonic generation as function of gate bias voltage.

2. The stability design of the circuit

The feedback of a fundamental element and harmonics at the drain can result in an unstable circuit. The sufficient elimination of unwanted harmonics and the proper stabilization of the circuit, even if some of the conversion gain must be sacrified, can be adjusted to ensure stability. Fig. 3(a) showsthe circuit for stable operation with the gate bias in maximizing the third harmonic frequency as in the previous step. The input bias network typically includes a high impedance quarter wavelength line at the fundamental frequency (f_{LO}). This is so that no fundamental power leaks into the DC bias and acts as a short-circuit at the second harmonic frequency ($2f_{LO}$) as it becomes half wavelength at the second harmonic ($2f_{LO}$). The open stub at the gate acts as a short-circuit at the third harmonic frequency ($3f_{LO}$) fed from the drain port. The output circuit also provides sufficiedt rejection of harmonics, and provides short-circuit terminations to harmonics at the drain to ensure stability. The open stub at the drain acts as a short-circuit at the fundamental harmonic frequency (f_{LO}). Fig. 3(b) shows the stability factor of the circuit be greater than one over the full frequency band.



(a)



(b)

Fig. 3 (a) Circuit (b) Stability factor with respect to frequency.

3. The port selection for signal injection to realize a mixer circuit.

Single active mixers are generally categorized into one of three topologies; (1) gate, (2) drain, and (3) source mixers. In the case of the gate mixer, both LO and RF signals are applied to the gate while the IF is extracted from the drain terminal. The FET is biased near pinch-off so that the applied LO signal can modulate the transconductance of the FET over a highly nonlinear operating regime. For the drain mixer, the LO and RF signals are applied to the drain and gate, respectively, while the IF signal is extracted from the drain. This mixer operates with the FET drain-source voltage near the knee region. In a source FET mixer, the LO and RF signals are fed into source and gate respectively while the IF signal is extracted from the drain. This topology allows a modest degree of LO-to-RF isolation. Since the source FET mixer does not require a coupler or combiner, it is a simple structure compared with other mixer topologies. However, this configuration requires careful bypassing technique in the source for the IF frequency in order to suppress instability.

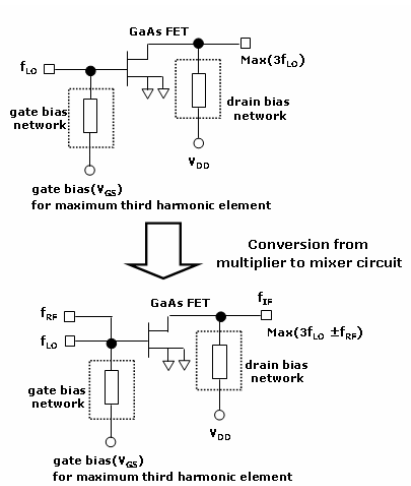


Fig. 4 The concept of converting from multiplier to mixer circuit.

Fig. 4(a) shows the conversion from the designed circuit based on multiplier theory to mixer circuit. The gate bias voltage is selected to maximize the third harmonic signal ($3f_{LO}$) by the previous section. The local frequency (f_{LO}) and the radio frequency (f_{RF}) are inputted to the gate and the intermediate frequency (f_{IF}) is outputted to the drain as a gate mixer structure, which has higher conversion gain then other mixer topologies such as drain mixer and source mixer[10].

Fig. 5 shows the structure of the proposed harmonic mixer, The local frequency (f_{LO}) and radio frequency (f_{RF}) to input gate after each matching, and IF signal (f_{IF}) is to the drain after the low pass filter. The gate bias voltage of the proposed mixer is selected on multiplier theory to maximize the third harmonic signal ($3f_{LO}$). The LO matching circuit is designed by a large signal scattering parameter as a large signal LO is applied. The matching circuit of the RF and IF ports is designed as quasi-linear because the RF and IF ports of impedance are affected by LO signal level[11].

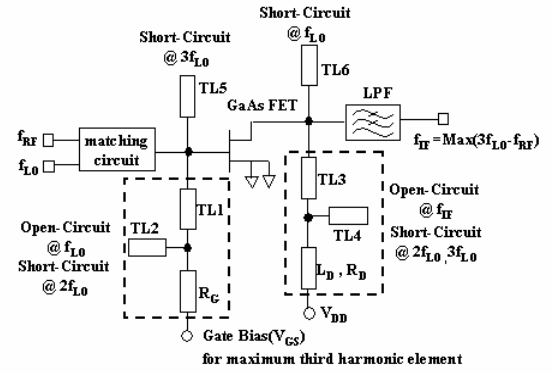


Fig. 5 The proposed harmonic mixer configuration.

The gate bias voltage of the proposed harmonic mixer is selected to make the mixing component between the applied RF signal (f_{RF}=33.5 GHz) and third harmonic signal ($3f_{LO}$=34.5 GHz) of the pumped fundamental LO signal (f_{LO}=11.5 GHz) to be maxi-

mum, which let the conversion loss be minimum at the immediate frequency ($f_{IF}=3f_{LO}-f_{RF}=1.0$ GHz).

Fig. 6 shows the conversion loss characteristic of the harmonic mixer as a function of gate bias voltage. Fig. 6 delineates the frequency conversion characteristic ($3f_{LO}-f_{RF}$) generated by the third-order harmonic component ($3f_{LO}$). As seen from Fig. 6, the conversion loss is -10dB when the gate bias voltage (V_{gs}) is -0.5V for maximum third harmonic generation and also shows conversion loss characteristics for both the harmonic mixing component ($f_{LO}-f_{RF}$) by the fundamental LO signal and the harmonic mixing component ($2f_{LO}-f_{RF}$) by the second LO signal.

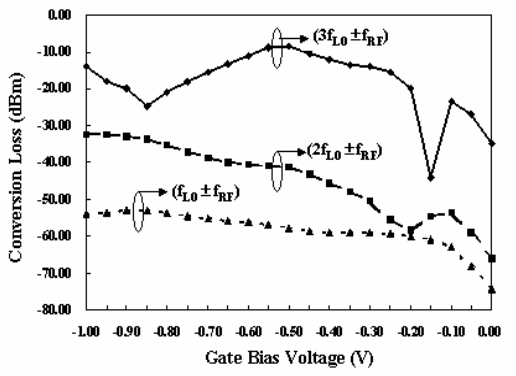


Fig. 6 The conversion loss of the third-order harmonic mixing and fundamental , second harmonic mixing.

III. Measurement Result

The proposed mixer fabrication is fabricated on a Teflon substrate, which has dielectric constant 2.17, 0.5mm substrate height and 18um conductor thickness.

Fig. 7 shows the measurement results of conversion loss performance at the immediate frequency ($3f_{LO}$-fRF) as a function of gate bias voltage when the fundamental LO signal is +5 dBm. Conversion loss is approximately -10dB when the gate voltage is -0.5V. As seen from the result, the conversion loss is rapidly decreased at other bias points except the gate bias voltage, which makes the third harmonic component ($3f_{LO}$) a maximum.

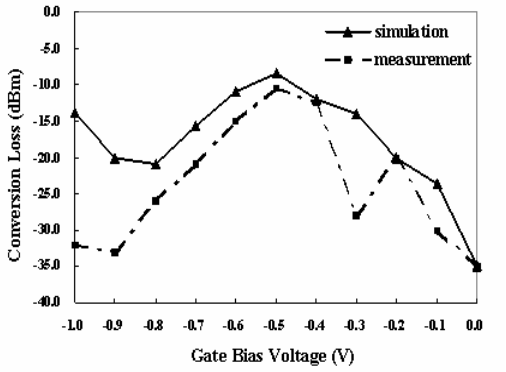


Fig. 7 The variation of the conversion loss with respect to gate bias voltage.

Fig. 8 shows the conversion loss as a function of the LO level when the gate bias voltage is -0.5V. The conversion loss is about -10dB when LO level is from +5 dBm to +10 dBm.

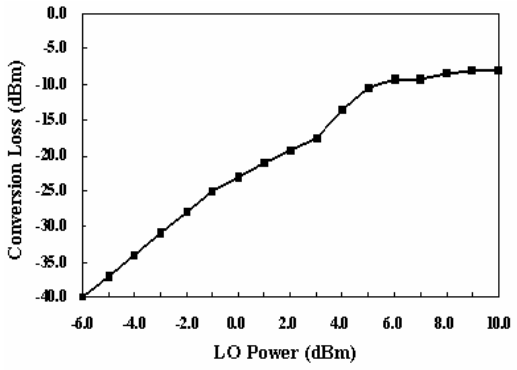


Fig. 8 The conversion loss performance with respect to LO power.

The output spectrum is approximately -52.5 dBm when the gate bias voltage is -0.5V with the fundamental LO level +5 dBm and RF level -40 dBm, as seen in the Fig. 9.

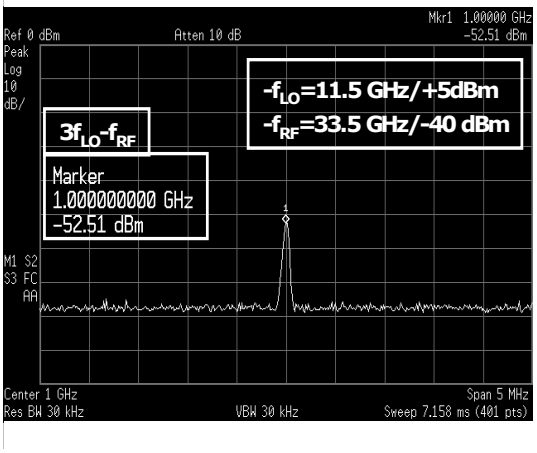


Fig. 9 IF output spectrum of the harmonic mixer.

Fig. 10 shows conversion loss performance as a function of RF frequency. The conversion loss is -8 ~ -10 dB when operating from 33.0 GHz to 36.0 GHz, which is lower than other published harmonic mixers at the Ka-band.

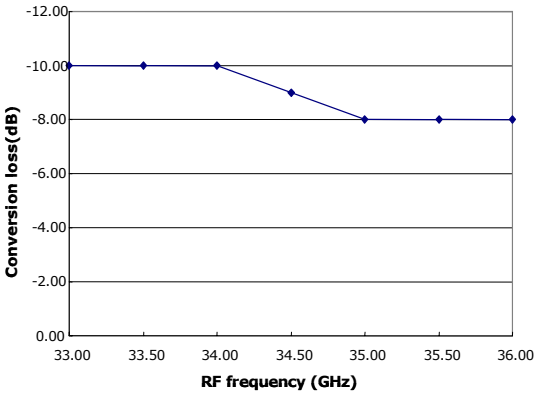


Fig. 10 The conversion loss with respect to RF frequency.

Fig. 11 shows the linearity performance of the proposed harmonic mixer when changing the RF signal level (33.5 GHz). As seen from Fig. 12, the 1-dB gain compression point is approximately 0 dBm.

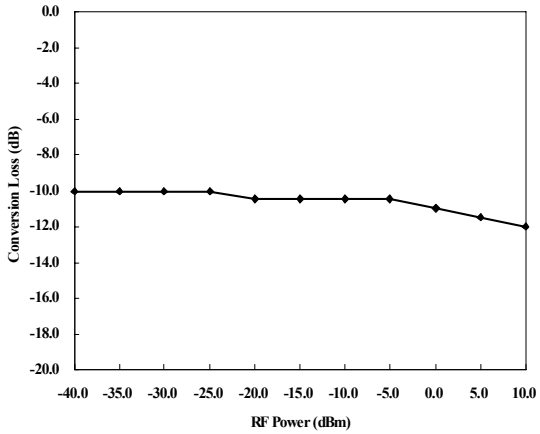


Fig. 11 Linearity performance.

Fig. 12 shows the isolation performance at the each port with the same environment for measuring the output spectrum. It is shown that the LO-RF isolation performance, worse than the RF-IF isolation, and the LO-IF isolation performance as known a single gate mixer' disadvantage. Table.1 summarizes the performance of the proposed third harmonic mixer.

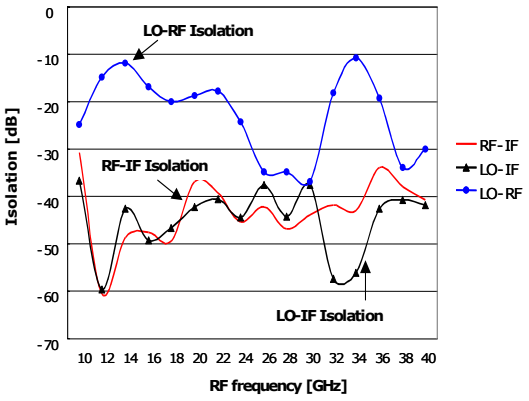


Fig. 12 Isolation performance.

Table 1. Summary of the proposed harmonic mixer.

Items		Design	Measurement
Frequency	RF	33.5 GHz	
	LO	11.5 GHz	
	IF	1.0 GHz	
Lo Power		0 dBm	5 dBm
Conversion loss @ 33.5 GHz		-10 dB	-10 dB
1-dB gain compression point(P1dB)		5 dBm	0 dBm
Isolation	LO-RF	-	-10 dBm
	LO-IF	-	-58 dBm
	RF-IF	-	-43 dBm

Ⅳ. Conclusion

In this paper, a new design method based on a frequencymultiplier is applied for a harmonic mixer. The proposed harmonic mixer that has -10dB conversion loss at the immediate frequency ($f_{IF}=3f_{LO}-f_{RF}$) by selecting the gate bias voltage which let the third harmonic component ($3f_{LO}$) of the fundamental LO signal (f_{LO}) to be maximum is designed and fabricated.

Table 2. Performance comparisons with the other papers.

Ref.	RF (GHz)	Device	Order	Loss (dB)	Tech.	LO level (dBm)
[5]	34~40	PHEMT	2	-9.5	MMIC	4
[12]	36.5 ~40	APT	8	-22 ~ -24.5	Hybrid	-
[13]	38~38.16	PHEMT	2	-15	MMIC	4
[14]	20~40	Diode	>10	-35 ~ -45	Hybrid	20
[15]	38	Diode	8	-23	MMIC	20
[16]	41.5	APD	3	-16	Hybrid	6
[17]	36~40	APD	2	-9.5	MMIC	6

Table.2 presents performance comparisons with other referenced papers. As compared with the other papers, the proposed harmonic mixer has many advantages, not only in electrical performance such as low conversion loss, but also in cost and circuit complexity by using a commercial GaAs MESFET with a plastic package.

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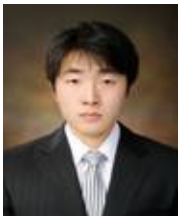

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