A Cyclic CMOS Time-to-Digital Converter

Jin Ho Choi and Ji Hong Kim , *Member, KIMICS*

Abstract—A CMOS TDC(time-to-digital converter) is proposed which has a simple cyclic structure. The proposed TDC consists of pulse-shrinking elements, D latches and D flip-flops. The operation is based on pulse-shrinking of the input pulse. The resolution of digital output can be easily improved by increasing the number of the pulse-shrinking elements, D latches and D flip flops. The TDC performance is improved in viewpoints of power consumption and chip area. Simulation results are shown to illustrate the performance of the proposed TDC circuit.

Index Terms—time-to-digital converter, cyclic structure, delay element, pulse shrinking element,

I. INTRODUCTION

TDC(Time-to-Digital Converter) is an important element for many instrumentation circuits such as range finders, frequency synthesis, and phase-meter[1-3]. In general, TDC contains analog and digital circuit blocks and the architecture is built on the capacitor charge redistribution principle. The digital value is obtained by analog-to-digital conversion of the capacitor charge voltage. Conventional TDC cannot easily be realized in portable systems due to large power consumption.

In this paper, the new TDC is proposed, allowing for a simplified *cyclic* structure and enhanced electrical performance such as power consumption and chip area.

This paper is organized as follows. Section II describes the schematic of proposed TDC circuit and CMOS TDC circuit. Section III presents simulation results for the designed TDC. Finally, section IV concludes this paper.

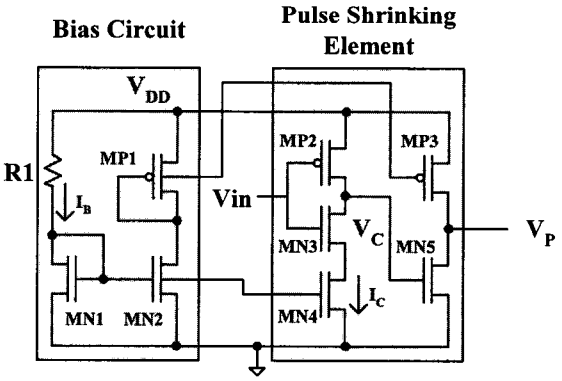
II. TDC Circuit implementation

Fig. 1 shows the pulse shrinking element. In Fig. 1(a) MN1 and MN2 are the constant current source. The drain currents of MN1 and MN2 are identical because the gate-to-source voltages of MN1 and MN2 are the same and MN1 and Mn2 have equivalent channel width and length. I_C flows through MN4 is given by

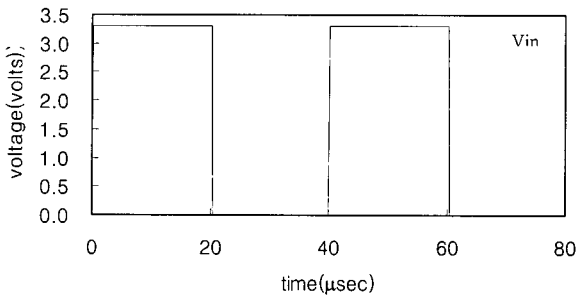
$$I_{RATIO} = \frac{I_C}{I_B} = \frac{(W/L)_{MN4}}{(W/L)_{MN1}} \quad (1)$$

where W is the channel width and L is the channel length. Fig. 1(b) and Fig. 1(c) show Vin, V_C and V_P waveforms. When the input pulse, Vin, is low MP2 is on and MN3 is off. V_C is high and the output, V_P, is low. When Vin is high MN3 is on and V_C decrease linearly because MN4 is a constant current source. When V_C voltage drops below the critical voltage, the output signal, V_P, is switched to a high state as shown in Fig. 1(b) and (c). The critical voltage is about 0.4 volts, which is obtained from SPICE simulation.

The width of Vin shrinks by the pulse shrinking element and the degree of pulse shrinking is controlled by the constant current source I_C which can be controlled by the change of R1 and the current, I_{RATIO}.



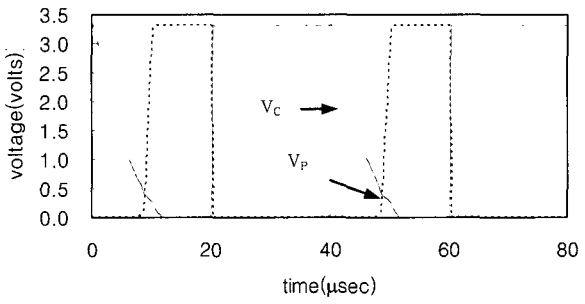
(a)



(b)

Manuscript received May 3, 2007.

Jin Ho Choi is with the Dept. of Computer Engineering, Pusan University of Foreign Studies, Busan, 55-1, Korea (Tel: +82-51-640-3194, Email: jhchoi@pufs.ac.kr) Ji Hong Kim is with the Dept. of Visual Information Engineering, Dongeui University, Busan, 995, Korea (Tel: +82-51-890-2267, Email: arim@deu.ac.kr)



(c)

Fig. 1 Pulse shrinking circuit and waveforms
(a)bias and pulse shrinking element circuits
(b)input waveform
(c)V_C and V_P waveforms

The pulse shrinking element reduces input pulse width by 10μsec as shown in Fig. 1(c).

Fig. 2 and Fig. 3 show D latch circuit and negative edge triggered D flip-flop circuit[4].

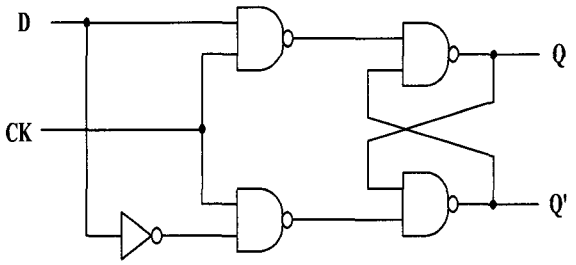


Fig. 2 D latch

The negative edge triggered D flip-flop ignores the pulse while it is at a constant level and triggers only on the negative edge of the clock signal. Fig. 4 shows the schematic of TDC circuit for input time digitization which consists of pulse-shrinking elements and D latches and D flip flops.

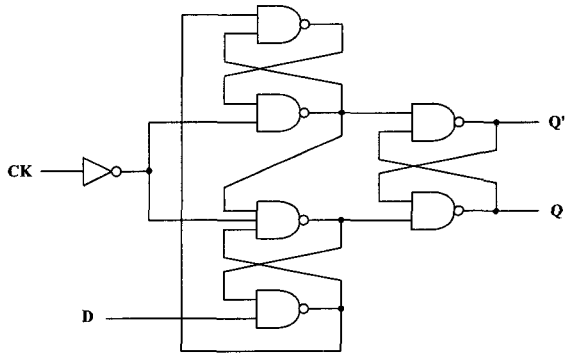


Fig. 3 Negative-edge triggered D Flip Flop

When the input, Vin, is high the outputs of pulse shrinking elements, V_{PX}, are stored in D latches. And then the outputs of D latches, V_{LX}, are transferred to the D flip-flops on the negative edge of input pulse, Vin.

Table 1 shows the digital output with input time interval. In table 1 t_R is the input time interval and V_{DX} are the outputs of D flip flops. And the information of input time interval is included in the outputs of D flip flops, V_{DX}.

Form table 1 the digital outputs, 2^2, 2^1 and 2^0 are expressed by

$$\begin{aligned} 2^2 &= V_{D3} \\ 2^1 &= V_{D5} + \overline{V_{D3}} V_{D1} \\ 2_0 &= V_{D6} + \overline{V_{D5}} V_{D4} + \overline{V_{D3}} V_{D2} + \overline{V_{D1}} V_{D0} \end{aligned} \quad (2).$$

where V_{D0}, V_{D1}, V_{D2}, V_{D3}, V_{D4}, V_{D5} and V_{D6} are the outputs of D flip flops. In Fig. 4 the logic circuit is implemented by using eq. (2).

The proposed TDC circuit is implemented only CMOS transistors without capacitor which has a simple cyclic structure. Thereby the chip area will be reduced compared to conventional TDC circuit.

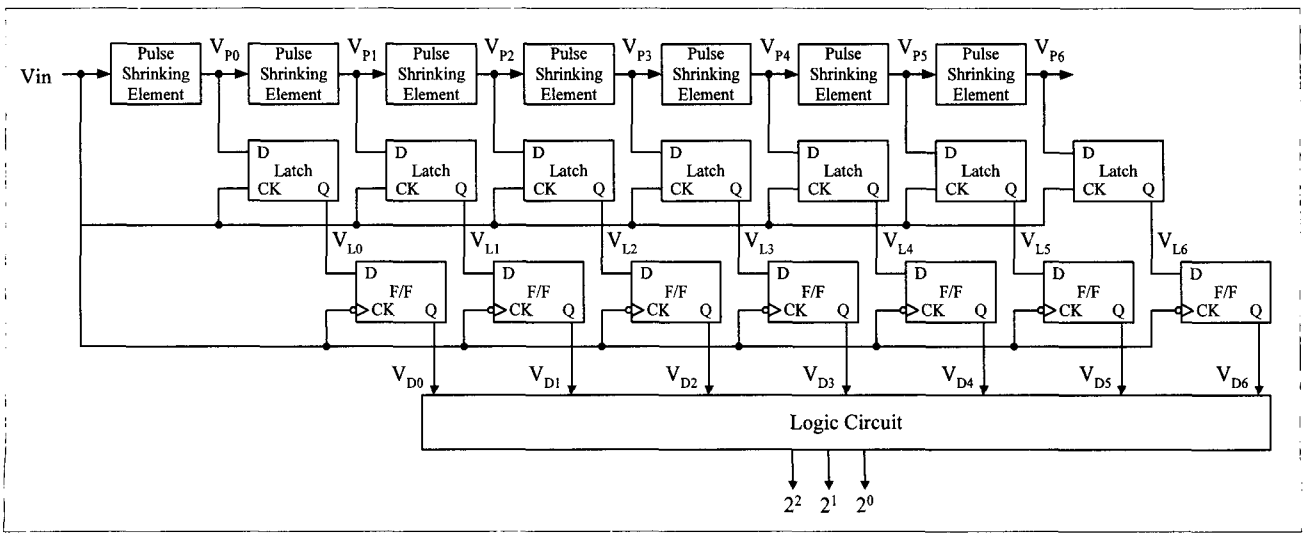


Fig. 4 The TDC(Time-to-Digital Converter) Circuit

Table 1 The digital outputs with input time intervals

time t(sec)	V_{D6} V_{D5} V_{D4} V_{D3} V_{D2} V_{D1} V_{D0}							Digital output		
								2^2	2^1	2^0
$0 \le t < t_R/8$	0	0	0	0	0	0	0	0	0	0
$t_R/8 \le t < 2t_R/8$	0	0	0	0	0	0	1	0	0	1
$2t_R/8 \le t < 3t_R/8$	0	0	0	0	0	1	1	0	1	0
$3t_R/8 \le t < 4t_R/8$	0	0	0	0	1	1	1	0	1	1
$4t_R/8 \le t < 5t_R/8$	0	0	0	1	1	1	1	1	0	0
$5t_R/8 \le t < 6t_R/8$	0	0	1	1	1	1	1	1	0	1
$6t_R/8 \le t < 7t_R/8$	0	1	1	1	1	1	1	1	1	0
$7t_R/8 \le t < t_R$	1	1	1	1	1	1	1	1	1	1

III. SIMULATION RESULTS

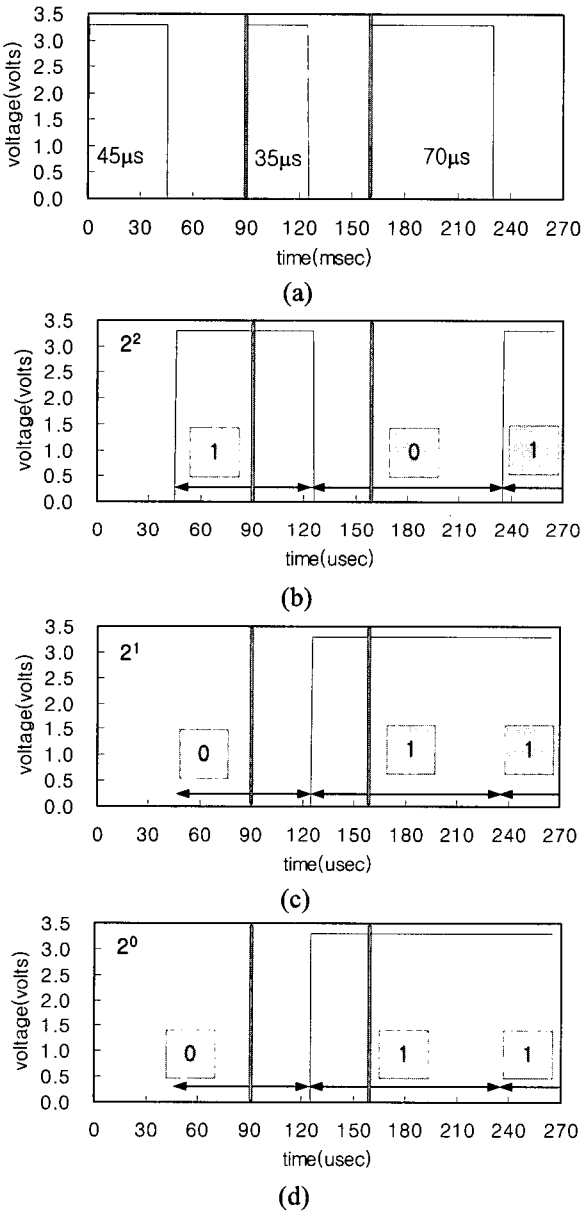


Fig. 5 output signals in designed TDC circuit
(a) input pulse (b) output signal, 2^2
(c) output signal, 2^1 (d) output signal, 2^0

The performance of the designed TDC is shown in Fig. 5 and table 2 when the input time interval, t_R, is 80μsec. Fig. 5(a) is the input signal and Fig. 5(b), (c) and (d) are the digital outputs. The digital outputs are obtained in the negative edge of input pulse, Vin. The digital outputs are sustained until next negative edge of input pulse. When input time interval is 45μsec the voltage of V_{D3}, V_{D2}, V_{D1} and V_{D0} are high because the degree of pulse shrinking is 10μsec. Thereby the digital output is (100). When the input time intervals are 35μsec and 70μsec, the digital outputs are (011) and (111), respectively.

The maximum power consumption is only 2.37mW in the proposed TDC circuit which decreases dramatically compared to conventional TDC converter.

Table 2 V_{DX} and digital outputs with input time intervals

Time t(sec)	V_{D6} V_{D5} V_{D4} V_{D3} V_{D2} V_{D1} V_{D0}							Digital output		
								2^2	2^1	2^0
t=45μsec 40μs≤t<50μs	0	0	0	1	1	1	1	1	0	0
t=35μsec 30μs≤t< 40μs	0	0	0	0	1	1	1	0	1	1
t=70μsec 70μs≤t< 80μs	1	1	1	1	1	1	1	1	1	1

IV. CONCLUSIONS

The time-to-digital converter is designed. The designed TDC is implemented only CMOS transistors without capacitors and the performance of TDC is improved in the viewpoint of chip area and power consumption. As well, the resolution of the digital output can be improved by increasing the number of pulse-shrinking elements, D latches and D flip flops. The designed TDC circuit shows enough output characteristics to use in time-to-digital signal processing.

REFERENCES

[1] Abdelouahab Djemouai, Mohamad A. Sawan and Mustapha Slamani, "New Frequency-Locked Based on CMOS Frequency-to-Voltage Converter: Design and Implementation," *IEEE Trans. On Circuits and System-II; Analog and Digital Signal Processing*, vol. 48, no. 5, pp. 441-449, May 2001.

[2] Norman M. Filiol, Tomas A. D. Riley, Miles A. Copeland and Calvin Plett, "A Receive Path Σ Δfrequency to Digital Converter," *IEEE International Symposium on Circuits and Systems*, Geneva, Switzerland, pp. 331-334, May 2000.

[3] Rahkonen. T. E, "The Use of Stabilized CMOS Delay Lines for The digitization of Short Time," *IEEE J. Solid State Circuits*, vol. 28, no. 8, pp. 887, *1993.*

[4] M. Morris Mano and Charles R. Kime, *Logic and Computer Design Fundamentals,* Prentice Hall, 1997, pp. 173–193.

Jin Ho Choi
received the B.S. degree in electronics from Busan University in 1985, and the M.S. degree in electronics from KAIST in 1987. He received the Ph. D. degree in electronics from KAIST in 1992. From 1992 to 1996, he was a researcher at Hynix Semiconductor Inc.. Since 1996, he has been a professor in Dept. of Computer Engineering, Pusan University of Foreign Studies. His research interest includes VLSI design.

Ji Hong Kim
received the B.S. and M.S. degree in electronics engineering from Kyungpook National University, Korea, in 1986 and 1988, respecttively, and the Ph. D. degree in electronic and electrical engineering from POSTECH, Korea, in 1996. He worked at ETRI from 1988-1997 and at Pusan University of Foreign Studies from 1997-2002. In 2002, he joined the Dongeui University, where he is an associate professor. His current research interests are in the area of digital image processing, computer graphics, and computer vision.