Characterization of Ultrathin Gate Dielectrics for Nanoscale CMOS Applications

Giwan Yoon, Linh Mai and Jae-young Lee, *Members, KIMICS*

Abstract**—**In this paper, MOS devices with ultrathin gate dielectrics (5.5 nm) are characterized and compared with those with conventional oxides particularly for nanoscale CMOS applications. Nitrogen concentrations and profiles in the nitride gate dielectrics were obtained that will play an important role in improving both hot-carrier lifetime and resistance to boron penetration. This approach seems very useful for future nanoscale CMOS device applications.

Index Terms—MOS devices, Ultrathin nitrided gate dielectrics, Hot carrier effects, Boron penetration

I. INTRODUCTION

Recently, nanoscale CMOS devices have been a great concern as the device sizes are increasingly scaled down dramatically beyond conventional regimes. Majority of the researches have been focusing on the nanoscaling issues, related to the device and process technologies [1]. On the other hand, an aggressive MOS device scaling has greatly demanded ultrathin gate dielectrics [2-5]. However, the ultrathin gate dielectrics have been a major concern in fabricating very reliable deep-submicron devices mainly due to hot carrier effects [2, 3] and boron penetration [4, 5]. Nitrided gate dielectrics have been proposed to be a promising alternative choice to the conventional SiO_2. In general, these dielectrics have been prepared in atmospheric pressure (~760 torr) using NH_3 or N_2O and are still looking for better process and optimization that can further improve the device characteristics. In this paper, a new technique, namely NH_3-nitrided N_2O-annealed oxides (NNO) is proposed and demonstrated to obtain the desired nitrogen concentration and profiles that may improve hot-carrier lifetime and resistance to boron penetration. The NNO gate dielectrics fabricated in reduced pressure (< 550 torr) have resulted in excellent hot-carrier lifetimes and barrier property to boron penetration without any other adverse effects on electrical properties and reliability.

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II. DEVICE FABRICATIONS

N-MOSFETs (NMOS) and p-MOSFETs (PMOS) with various nitrided gate dielectrics (Table 1) were fabricated on 200 mm epitaxial wafers. LOCOS isolation and threshold voltage (V_{th}) adjustment implants were performed. After removal of thin sacrificial oxides, various gate dielectrics were fabricated at different process conditions. The NNO dielectrics were fabricated by annealing thin SiO_2 in reduced pressure using NH_3 and/or N_2O. Then, reoxidation treatments in the NNO samples were performed in N_2O, followed by a post oxidation annealing in N_2. Wafers with different gate dielectrics were combined and processed together through poly-Si deposition. After patterning and reoxidation of poly-Si gates, the shallow S/D extensions called MDD [2] were made with BF_2 and As. After sidewall spacer patterning, the poly-Si gates and S/D regions were heavily doped with BF_2 for PMOS and with As for NMOS. These implants were activated by rapid thermal annealing (RTA). The $CoSi_2$ self-aligned silicide process was performed for the reduction of gate electrode and S/D resistance.

Table 1 Oxide charge (Qox), interface state density (Dit), oxide thickness (Tox), peak nitrogen concentration ([N]), interface roughness (Ra) for dielectrics.

Sample Name	**Q_{ox} (q/cm^2)**	**D_{it} ($cm^{-2}.eV^{-1}$)**	**T_{ox} (Å)**	**[N] Atomic (%)**	**Ra (nm)**
Conventional Oxide	9.6E10	6.7E10	56	~0	0.135
N_2O-Oxide	2.0E11	1.1E11	55	1.1	-
NNO-1	2.8E11	9.3E10	57	2.6	-
NNO-2	3.1E11	1.0E11	56	3.2	0.144

III. RESULTS AND DISCUSSION

Nitrogen distributions by SIMS depth profiling were investigated for N_2O-oxide and NNO samples where the samples with a cap of amorphous silicon on dielectric film were prepared to enhance the resolution by eliminating any possible surface artifacts during analysis.

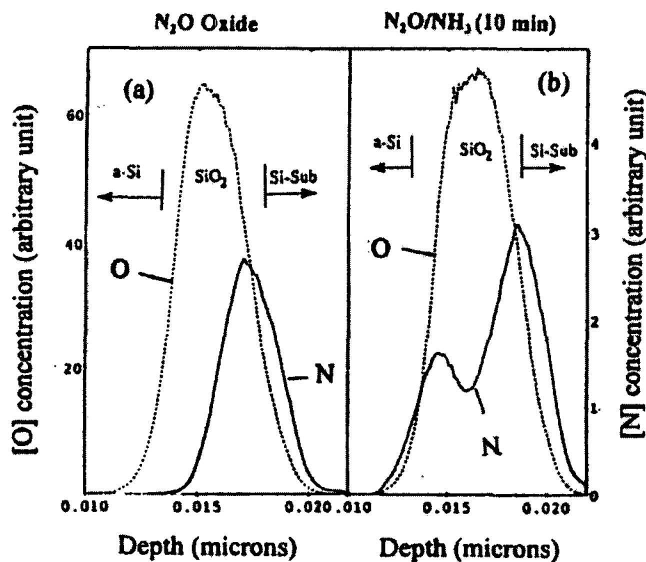

Fig. 1 SIMS depth profiles for 85Å nitrided gate dielectrics: (a) N2O-oxide and (b) NNO samples.

N_2O-oxide samples always showed nitrogen peak at bottom interface, whereas NNO samples interestingly exhibited two nitrogen peaks at both, top and bottom interfaces (Fig. 1). It is believed that most of nitrogen atoms near top interface are incorporated during NH_3-nitridation following the first N_2O annealing. Nitrogen peak at bottom interface is known to play a critical role in preventing boron penetration. For even thinner oxides, however, peak nitrogen alone at bottom interface may not be sufficient enough to completely prevent boron penetration. In Fig. 2, drain current (I_{DS}) and transconductance (G_m) were plotted as a function of gate voltage (V_{GS}) for NMOS and for PMOS. While NNO and N_2O-oxides devices show slightly lower peak G_m at low-field than that of the conventional oxide, they begin to have higher G_m at high field. Higher nitrogen concentration at bottom interface resulted in higher degradation in peak G_m mainly due to increase of interface charges. Hot carrier lifetimes of NMOS devices were extracted for 55Å gate dielectrics. Lifetimes of NNO gate dielectrics were ~7 times longer than those of conventional gate oxides (Fig. 3). The NNO samples exhibited no significant shift in threshold voltage (V_{th}) compared with conventional oxides (Fig. 4), implying high resistance to boron penetration. Time zero dielectric breakdown (TZDB) characteristics were measured where the NNO dielectrics showed almost comparable distribution to both conventional oxides and N_2O-oxides, indicating no significant NH_3-nitridation induced micro-defects.

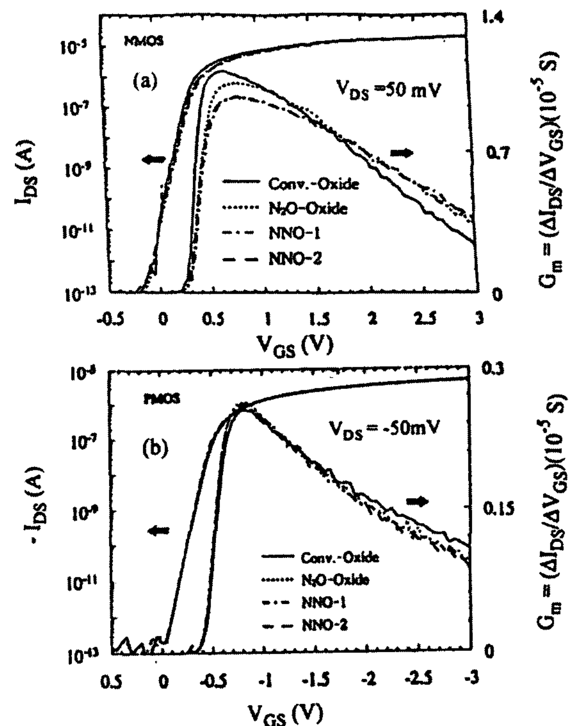

Fig. 2 Drain current and transconductance characteristics for 55Å gate dielectrics: (a) NMOS and (b) PMOS devices. (W/L = 40μm/40μm).

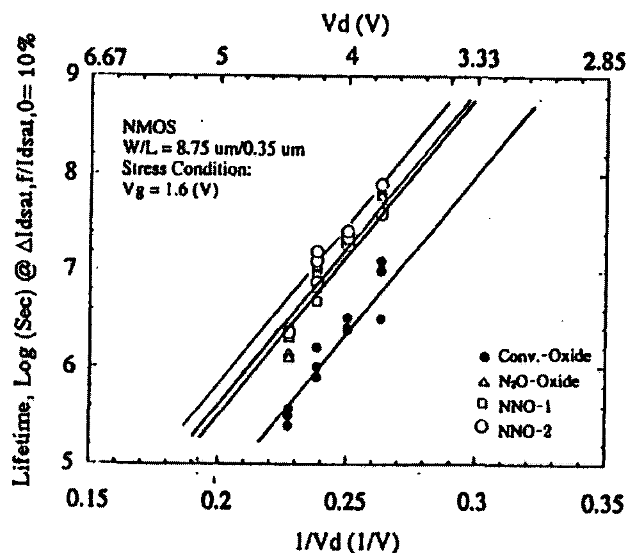

Fig. 3 Extracted lifetimes of NMOS devices with 55Å different gate dielectrics.

IV. CONCLUSIONS

NH_3-nitrided N_2O-annealed oxide (NNO) has been proposed and demonstrated to obtain the desired nitrogen concentration and profile that could improve hot-carrier lifetime and resistance to boron penetration. Thus, this approach may be useful for future nanoscale CMOS applications.

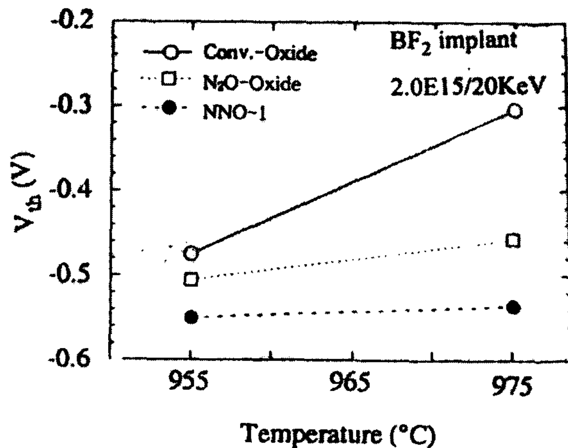

Fig. 4 Variation in threshold voltage of PMOS devices with ~ 45Å gate dielectrics.

ACKNOWLEDGMENT

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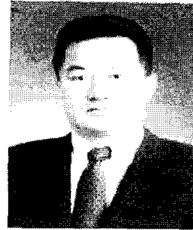

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