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A Five Mask CMOS LTPS Process With LDD and Only One Ion Implantation Step

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Abstract

We have developed a CMOS LTPS process which requires only five photolithographic masks and only one ion doping step. Drain/Source areas of NMOS TFTs were formed by PECVD deposition of a highly doped precursor layer while PMOS contact areas were defined by ion implantation. Single TFTs, inverters, ring oscillators and shift registers were fabricated. N- and p-channel devices reached field effect mobilities of 173cm²/Vs and 47cm²/Vs, respectively.

Keywords : poly-silicon, CMOS, ion implantation

1. Objectives and Background

Low temperature polysilicon (LTPS) thin film transistors are extremely promising devices for AMOLEDs as well as for high resolution AMLCDs. As LTPSs have high charge carrier mobility compared to a-Si:H TFTs, LTPS TFTs are also suitable for the integration of row and column driver electronics on the panel [1]. However, while only one type of TFTs (n-channel or p-channel) is required for an active matrix, CMOS is best suited for high performance driving circuits because of its high switching speed and low static power dissipation. Also, there are some proposed OLED-pixel circuits which require both NMOS and PMOS TFTs. Usually seven or more photolithographic steps are required for the production of CMOS circuitry with lightly doped drain (LDD) structures [2]. One mask step can be saved if no LDD is implemented, but leakage current of n-channel TFTs is then increased [3].

2. Experimental Procedures

Based on our ion-doping free process for NMOS LTPS TFTs, we have developed an LTPS (450 °C maximum process temperature) CMOS process that requires only five photolithographic steps [4]. The entire process flow is shown in Fig. 1. On a 360 nm thick silicon oxide buffer layer on Corning 1737 glass, 40 nm of highly phosphorus doped microcrystalline silicon is deposited by PECVD at 13.56 MHz and 280 °C, followed by photolithographic definition of source/drain areas for the n-channel TFTs. Then a 50 nm layer of intrinsic amorphous silicon is deposited at 280 °C and crystallized by single area excimer laser crystallization (SAELC) after dehydrogenation at 450 °C in either high vacuum or in an N_2 atmosphere [5]. The process temperature of the dehydrogenation step was higher than that of any other process step. The temperature that is necessary for dehydrogenation could be further reduced by laser treatment at low energies. Crystallisation was performed with a Sopra VEL15 XeCl excimer laser at energy densities of 540 mJ/cm² and 560 mJ/cm² in ambient air. This guarantees simple processing without having to maintain an inert atmosphere during crystallisation. A long pulse duration of approximately 200 ns allows the formation of highly doped contact areas and LDD regions by diffusion of phosphorus into the intrinsic silicon [6]. Measurements indicate that diffusion length was only several hundred nanometers which allows utilisation of this technique even for TFTs with short channels of only a few μm. NMOS TFTs with channel lengths of 5 μm have already been processed in our laboratory and showed the same on/off ratio as that for a 10 μm channel length. After the active islands were patterned for n- and p-channel TFTs, 100 nm of silane based PECVD gate oxide was deposited at 300 °C.

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A molybdenum-tantalum (MoTa) alloy was sputtered as gate metallisation and was defined by wet etching overlapping the earlier defined n-type doped areas (see Fig. 1). Drain/source regions of the p-channel TFTs were created by self aligned implantation of BF_2 without any protection of the n-doped regions. After laser activation of boron at 330 mJ/cm², silicon nitride was deposited by PECVD as an intermetallic dielectric layer and contact holes were opened through nitride and gate oxide in a two step plasma etching process. Contact metallization was sputtered, and was wet chemically structured. Finally, the devices were annealed at 350 °C under N_2 atmosphere for contact improvement.

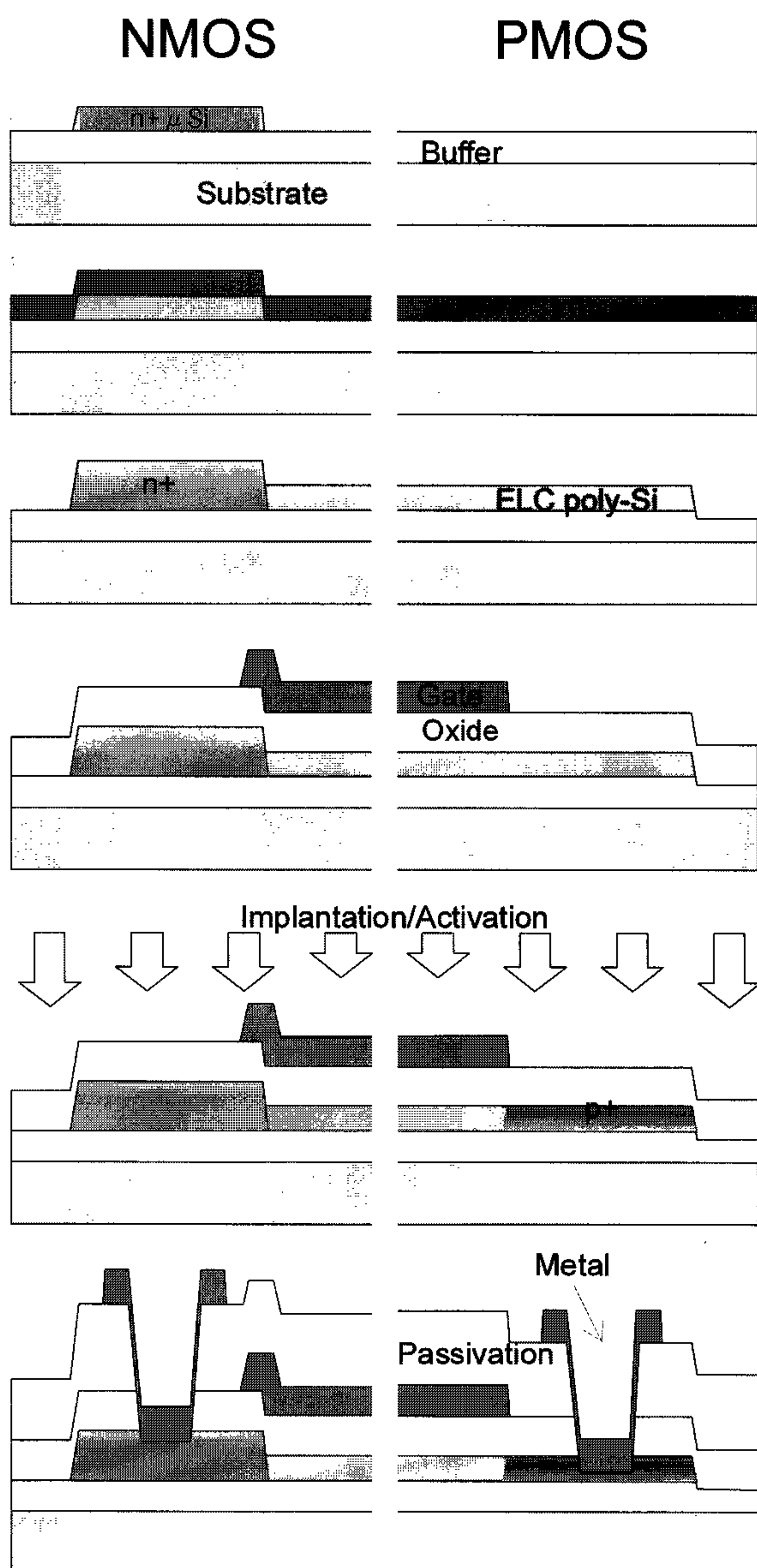

Fig. 1. Process flow of five mask CMOS-process

3. Results

It is evident that the implantation parameters are crucial for this process because there is no masking layer protecting the n-doped regions. The implantation dose must be sufficient to achieve a good ohmic contact between the semiconductor and the source/drain metallization without counter-doping the unprotected n-doped regions. Also the implantation depth has to be carefully adjusted. As phosphorous diffuses into the intrinsic silicon from below there is a gradient in its concentration resulting. If the maximum of the boron is implanted right at the interface between gate oxide and silicon, - as it would be ideal for PMOS TFTs - counter doping occurs, resulting in stacked layers of p-type and n-type material. Since both types of charge carriers (electrons and holes) are then present in the contact areas the result is an unipolar TFT with very high off currents. The input characteristic curve of such a TFT is shown in Fig. 2.

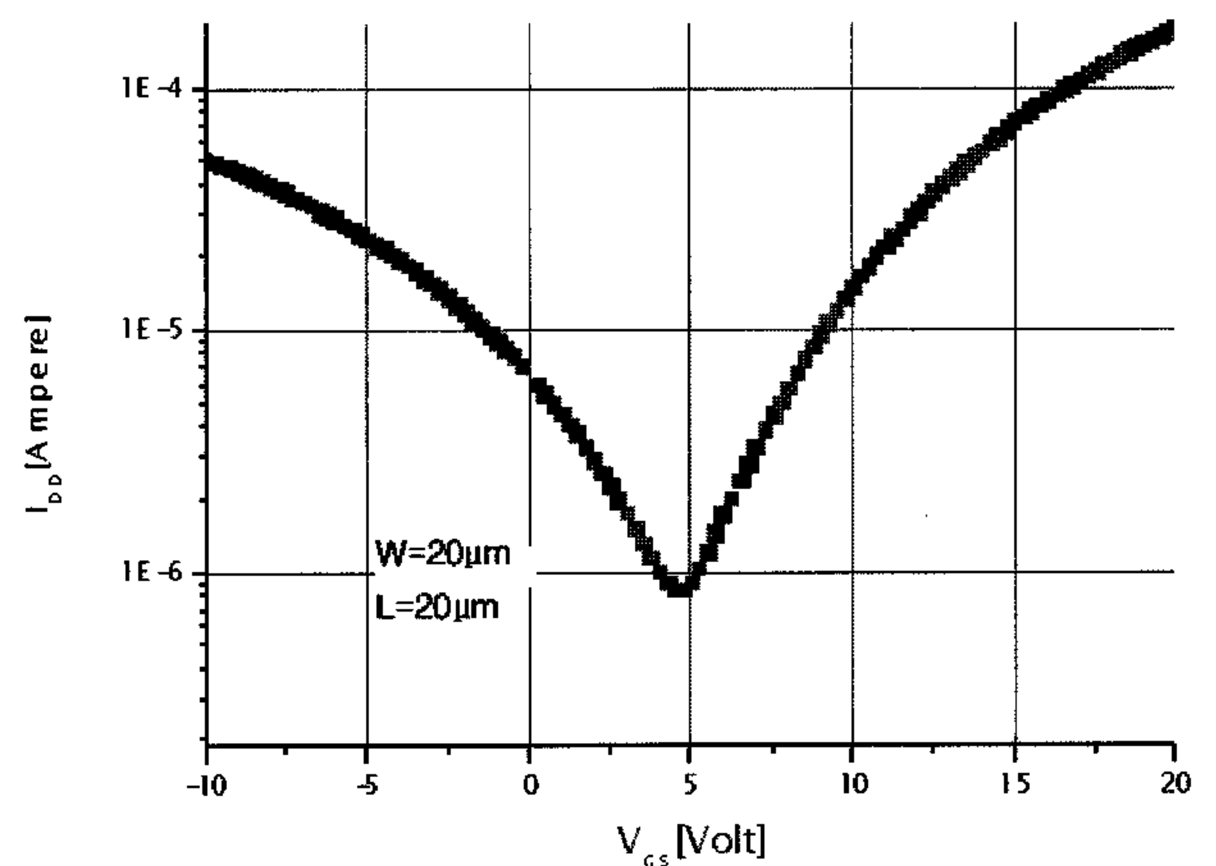

Fig. 2. Input characteristic of TFT with insufficient acceleration energy during implantation of boron

With higher ion acceleration voltages, the boron maximum was shifted below the silicon surface into a region with higher phosphorous concentration and no more counter doping occurs. We found acceleration voltages above 150keV suitable. So far, the devices that were produced with implantation doses between $0.5 \cdot 10^{15}$/cm² and $6 \cdot 10^{15}$/cm² were fully functional. Even at the lowest implantation dose, ohmic contacts were produced as indicated by the linear U-I behavior of the p-type silicon resistor shown in Fig. 3. Optimization of the implantation parameters will be a key issue in further improvement of process.

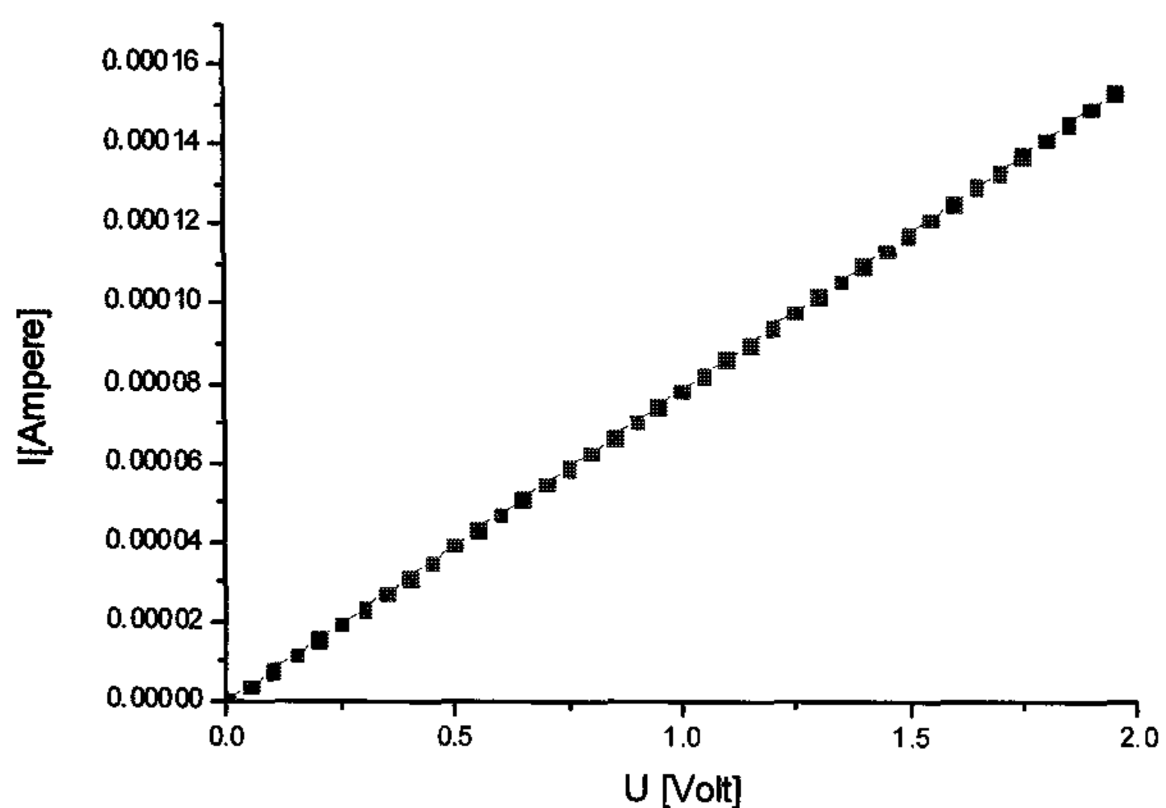

Fig. 3. I-U characteristics of a p-type silicon resistor

Single TFTs as well as inverters, ring oscillators and shift registers have been implemented on the same substrates.

Single TFTs showed similar results compared to those of standard NMOS- and PMOS processes that use excimer laser crystallization(ELC). Fig. 4 shows input characteristics for n- and p-channel TFTs. The n-channel TFT has a mobility of 173 cm^2/Vs, threshold voltage of 6.5 V and subthreshold slope of 0.86 V/dec. The p-channel TFT has a mobility of 47 cm^2/Vs, threshold voltage of 4.8 V and subthreshold slope of 0.74 V/dec.

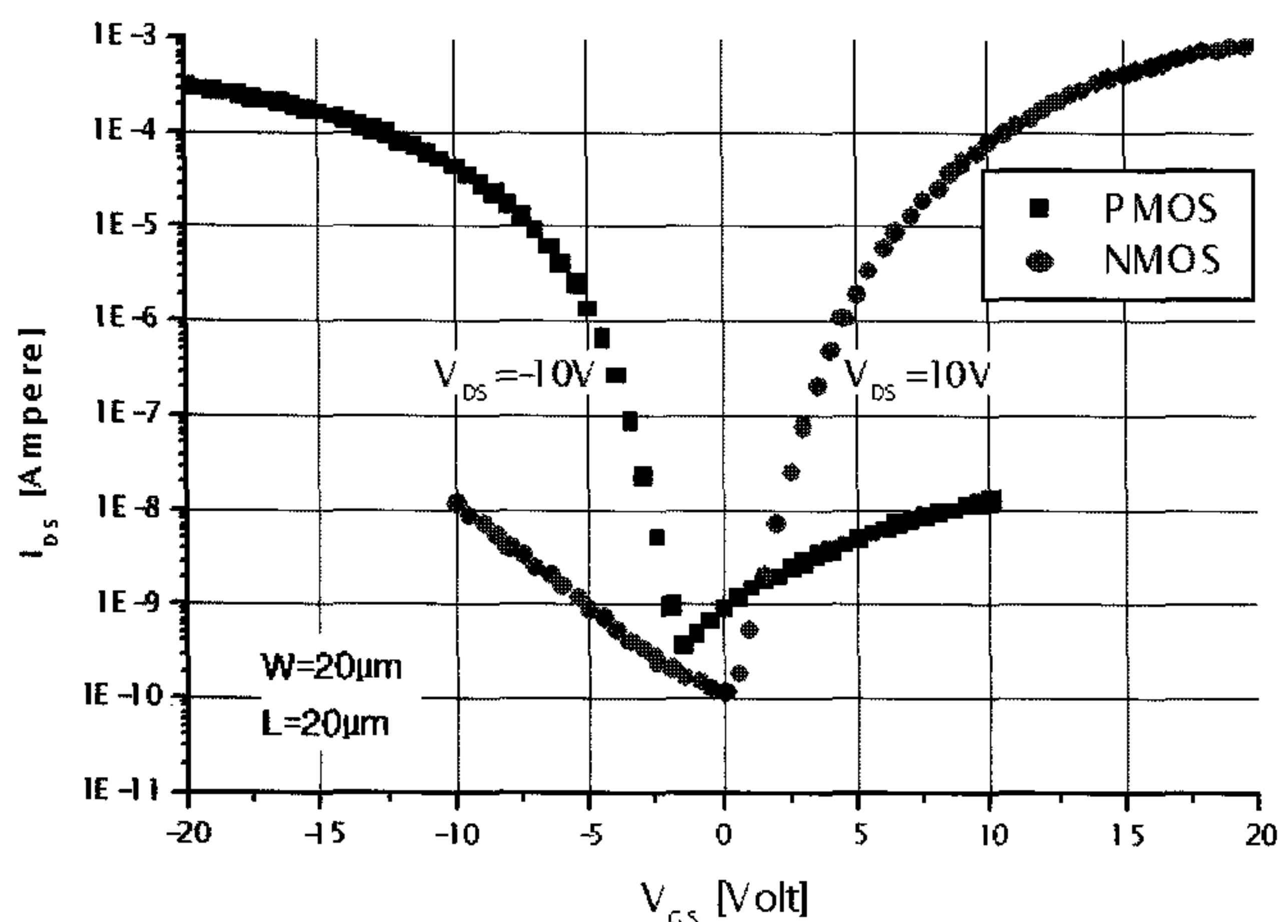

Fig. 4. Input characteristics of n- and p-channel TFTs

The inverters showed a behavior that was typical for CMOS devices with full voltage swing and very steep transfer characteristics. Fig. 6 shows the transfer characteristic of a CMOS inverter that shares the same substrate with the single TFTs. The structure of an individual inverter is depicted in Fig. 5. The overlap between the gate electrode and the n-doped regions creates an additional capacitance, and the overall parasitic capacitance increases, compared to fully self aligned CMOS processes. However, since the electron mobility is higher than the hole mobility by a factor 2-3, the NMOS TFT usually has a narrow channel and its overlap capacitance plays a minor role. For the inverter shown in Fig. 3, the channel length is 10 μm and overlap is 5 μm. The p-channel TFT is twice as wide as the n-channel TFT, so the overlap capacitance is only approximately 25% of the total inverter's input capacitance. The overlap can be decreased significantly but a high precision control during alignment of the gate mask would be required.

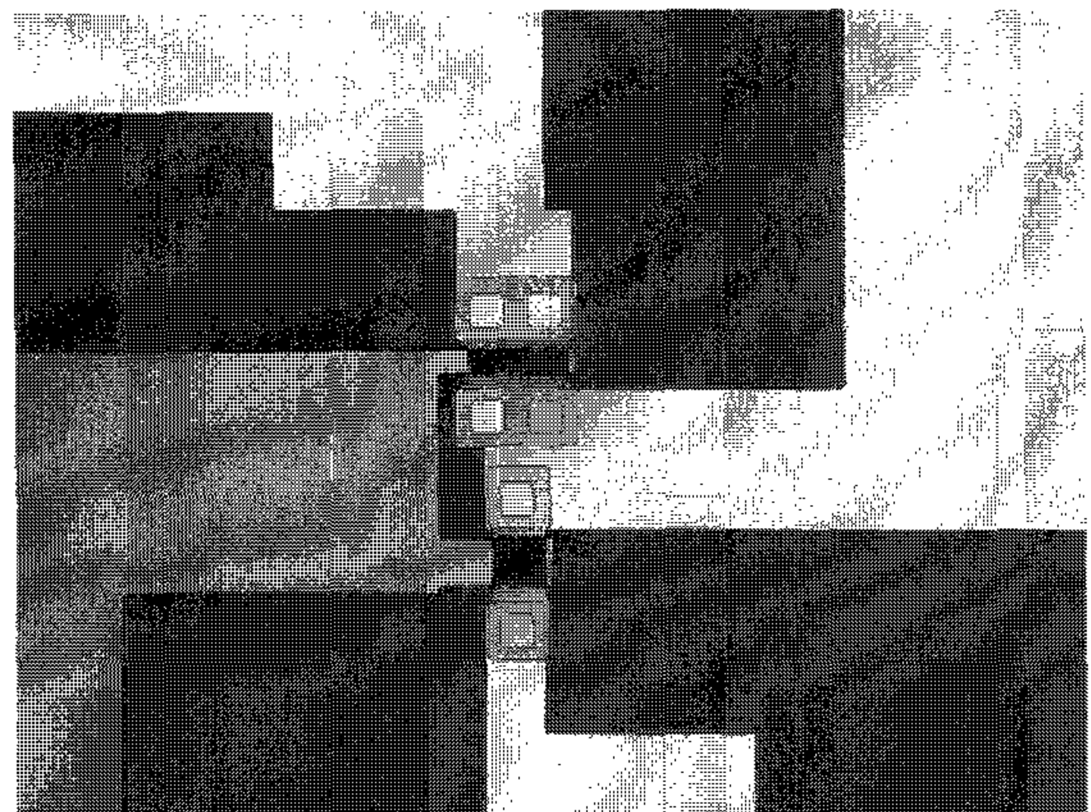

Fig. 5. Optical micrograph of CMOS inverter

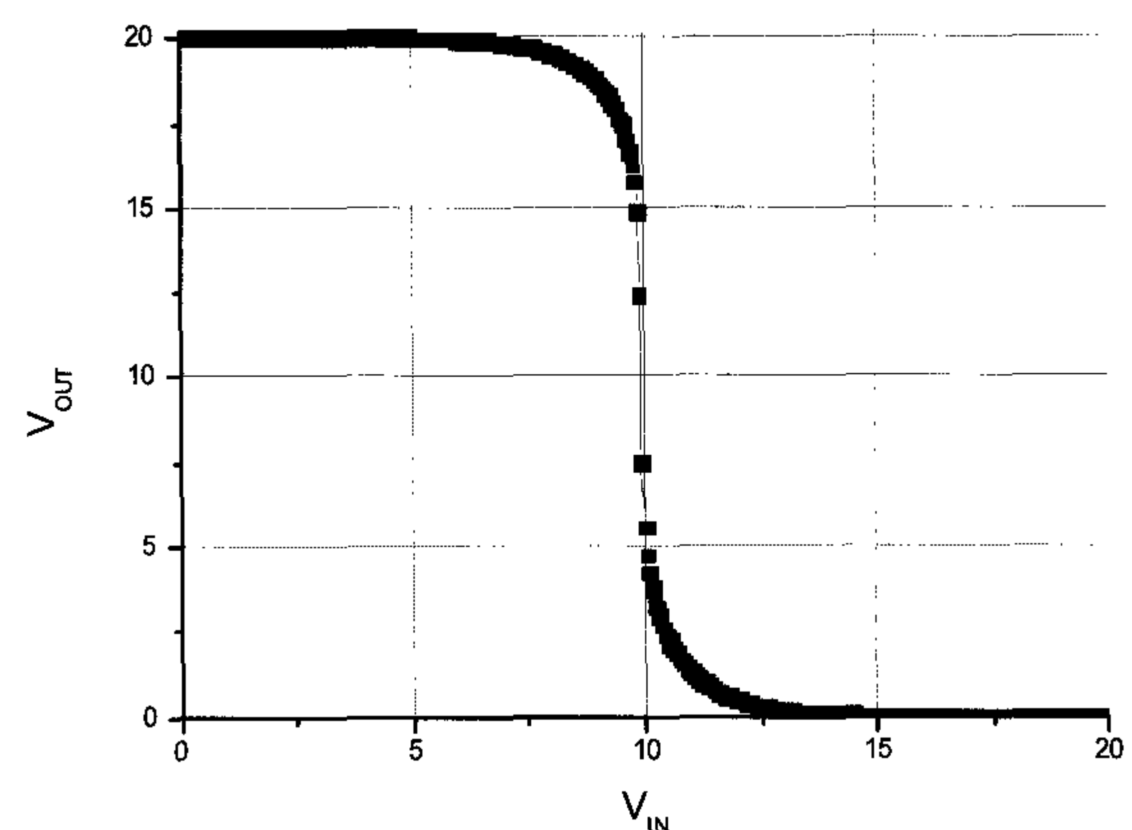

Fig. 6. Transfer characteristics of CMOS inverter

We implemented ring oscillators in order to determine the maximum switching speed of our circuits. Depending on their crystallisation conditions, the oscillator made of eleven inverters with a channel length of 10 μm showed an oscillation frequency of high as 3 MHz at V_{dd}=20 V. This

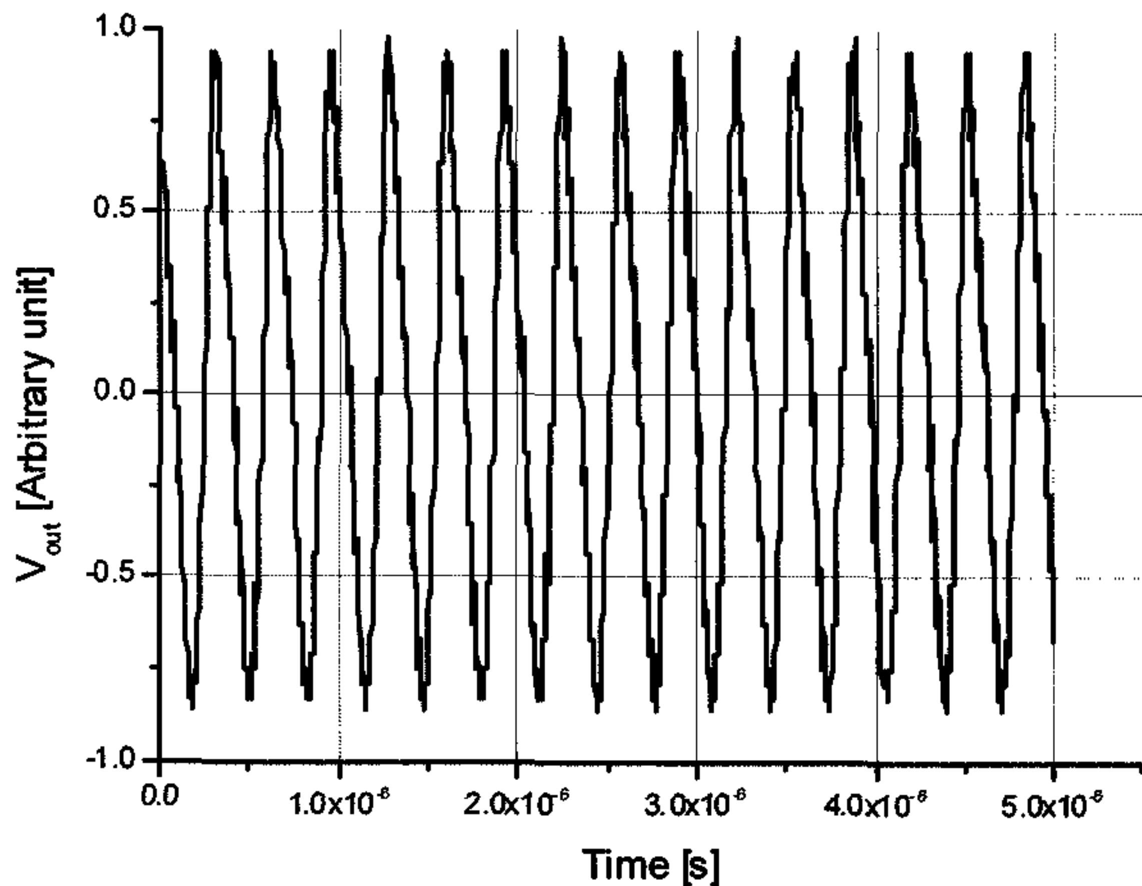

Fig. 7. Ring oscillator output

value can be interpreted as an operating frequency of over 30 MHz or a delay time t_d of about 30 ns for the single inverter. Fig. 7 shows the output signal of one ring oscillator measured directly by an oscilloscope that was connected with a coaxial cable. We expect the inverters to work at frequencies around 120 MHz after scaling the process to 5 μm channel length.

Simple two phase dynamic shift registers with five TFTs and one capacitor per stage were implemented as well. Every stage consists of two CMOS inverters and one NMOS switching TFT (Fig. 8). This design requires only four external lines (CLK1, CLK2, GND and synchronisation). The two clock signals were interchanged at every other stage. V_{OUT} of every stage was connected to V_{IN} of the following stage. All devices had a channel length of 10 μm. NMOS and PMOS TFTs have a width of 20 μm and 40 μm, respectively. C_l had a capacitance of approximately 1pF. The implemented registers have successfully been measured and all requirements of a gate driver were fulfilled. Fig. 9 shows the clock signals, input signal and the output signals of six consecutive stages at an operating speed of 20 kHz. A capacitive load of 100 pF could be driven without any additional output stages. Depending on the geometries of switching TFTs, this performance is sufficient for the gate driver of a full color qVGA display.

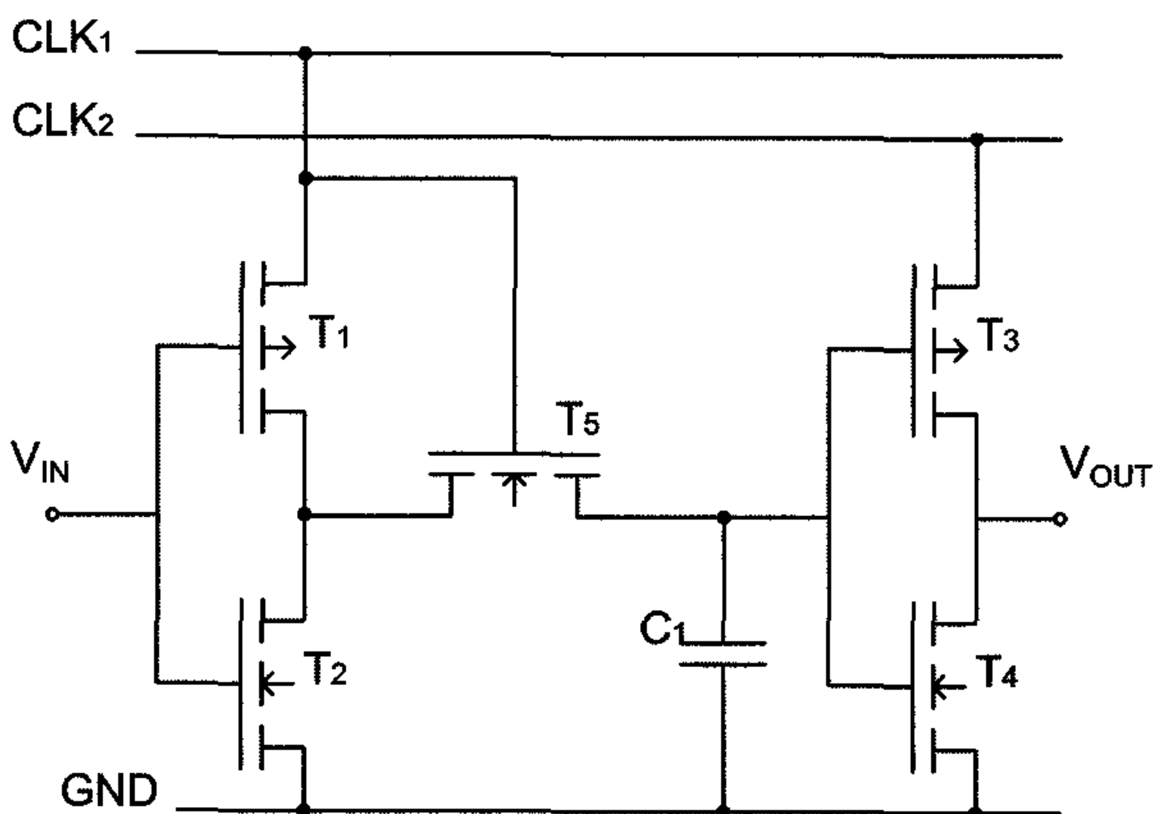

Fig. 8. One stage of the implemented CMOS shift register

4. Impact

We were able to produce CMOS circuits with a very simple and cost effective process. The TFTs showed the

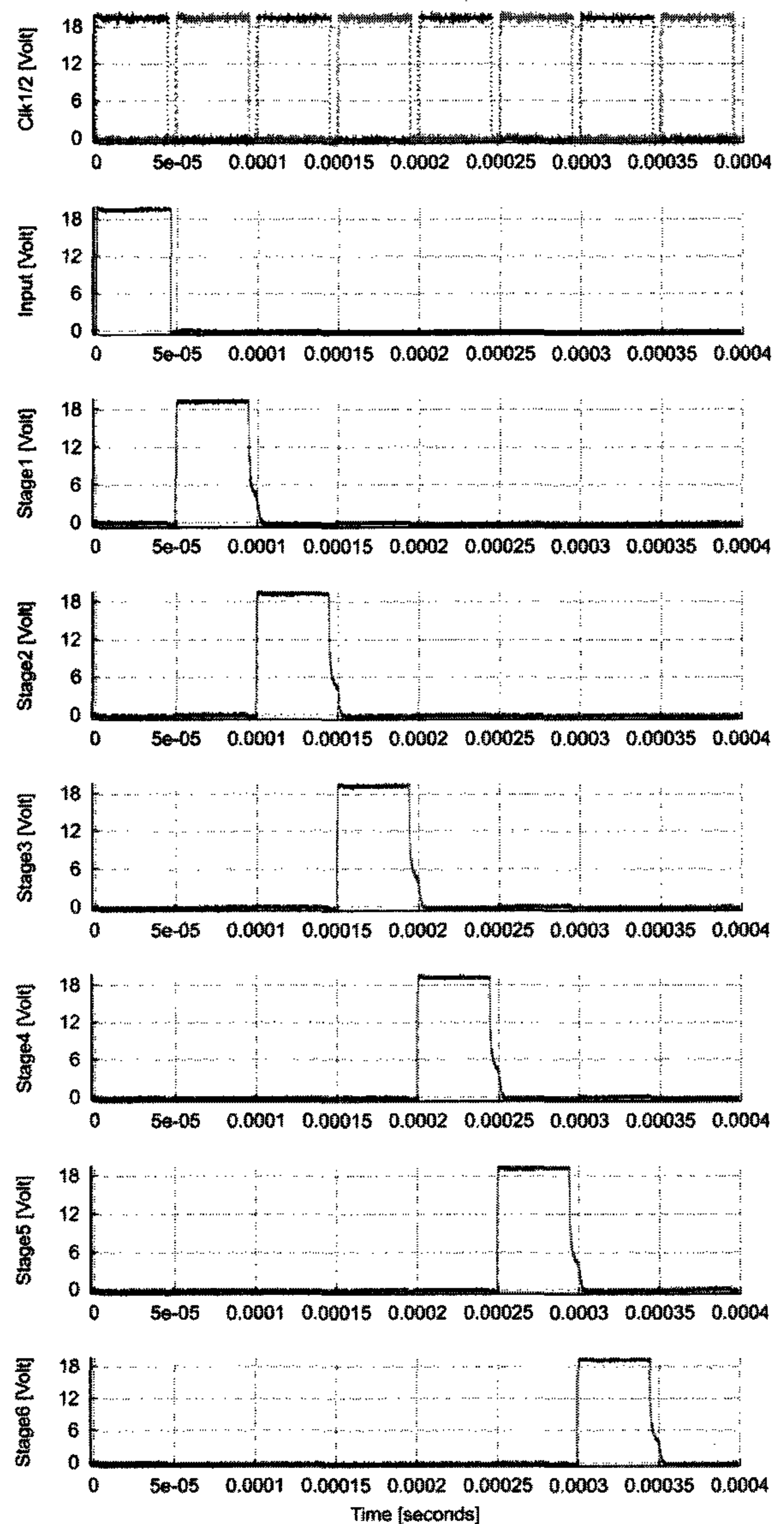

Fig. 9. Signal of six shift register stages

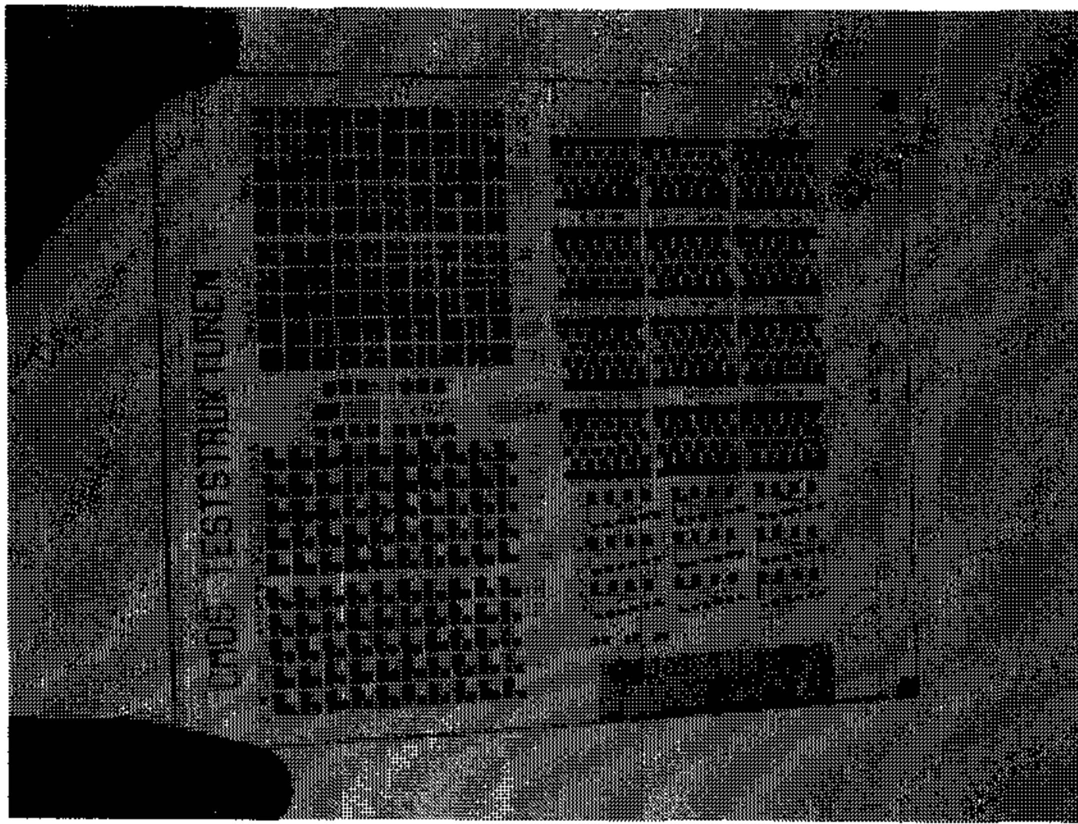

Fig. 10. A substrate with single TFTs, inverters, ring oscillators and shift registers

same performance as TFTs produced on SAELC-material with more complicated processes. The availability of ion doping free NMOS TFTs allows the implementation of large area active matrices, while an ion doping step is necessary only for the high performance driver electronics at the borders of the panel[4]. The throughput can be enhanced by reducing the time spent in the ion doping equipment. Additionally, it is possible to use CMOS pixel circuitry for advanced OLED panels. No additional mask step is necessary before the ion doping.

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