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Improvement of Carrier Mobility on Silicon-Germanium on Insulator MOSFET Devices with a Strained-Si Layer

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Abstract

The effects of heat treatment on the electrical properties of strained-Si/SiGe-on-insulator (SGOI) devices were examined. We proposed the optimized heat treatment processes for improving the back interfacial electrical properties in SGOI-MOSFET. By applying the additional pre-RTA (rapid thermal annealing) before gate oxidation step and the post-RTA after source/drain dopant activation step, the electrical properties of strained-Si channel on $Si_{1-x}Ge_x$ layer were greatly improved, which resulting the improvement of the driving current, transconductance, and leakage current of SGOI-MOSFET.

Key Words : SGOI-MOSFET, Strained-Si channel, RTA, Interface states, Mobility enhancement

1. INTRODUCTION

As the gate lengths of silicon metal-oxide-semiconductor (MOSFET) device scaled down to sub-100 nm regime, the operation of transistors is mainly limited by the short-channel effects (SCE). Silicon-on-insulator (SOI) MOSFET devices can relax the SCE compared to the conventional MOSFET fabricated on the bulk-silicon[1,2]. Especially, the strained-Si/SiGe-on-insulator (SGOI) MOSFET have attracted much higher attention than the SOI MOSFET because of its superior transport performance[2]. It has been reported that the electron and the hole mobility enhancement of carriers in the strained-Si inversion layer increases with Ge content in the $Si_{1-x}Ge_x$ layer, that is higher Ge mole fraction leads to higher electron mobility[3-5]. However, a limiting factor of nano-scale strained-Si SGOI wafers in mass production of MOS transistor is relying on reducing a high density of defects, resulting in poor channel properties as Ge content increases[6]. There are several interfaces at the gate oxide/strained-Si channel/$Si_{1-x}Ge_x$ layer/buried oxide in the SGOI MOS devices. These interfacial properties that depend on the thermal process will significantly influence on the device performance of SGOI MOSFET.

Therefore, we evaluated the electrical properties of strained-Si channel on the $Si_{1-x}Ge_x$ layer in SGOI substrate in this work. Since the rapid thermal annealing (RTA) is inevitable process for the ultra-shallow junction formation and became one of key technologies for suppressing the SCE in nano-scale CMOS (complementary metal-oxide-semiconductor) device, the effects of RTA and furnace annealing after RTA on the device performance of SGOI MOSFET as a function of Ge content was also investigated.

2. EXPERIMENTAL

Nano-scaled strained-Si channel SGOI wafers were fabricated by an optimized process of low-temperature epitaxial graded growth and buffered $Si_{1-x}Ge_x$ growth. To obtain strained-Si on a relaxed $Si_{1-x}Ge_x$ layer, a graded $Si_{1-x}Ge_x$

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layer was grown on a p-type Si substrate at 550 °C by varying the Ge concentration from 0 to 10, 15, and 20 at%. The chemical-mechanical polishing (CMP), hydrogen implantation, bonding of donor wafer with oxidized wafer, cleavage at hydrogen implanted plane, and surface treatment processes were then applied to fabricate nano-sclae SGOI substrate with a strained-Si channel. The strained-Si layer with a 10-nm-thick was formed on the relaxed $Si_{1-x}Ge_x$ layer of 50-nm-thick. The thickness of buried oxide (BOX) was 200 nm. Also, the conventional SOI wafer without $Si_{1-x}Ge_x$ layer with a 10-nm-thick Si layer was prepared as a control group. N-channel MOSFET devices were fabricated on SGOI or SOI substrates in order to characterize the current transport characteristics depending on the Ge contents in $Si_{1-x}Ge_x$ layer. Thermal oxidation in a dry O_2 ambient was employed to grow the 4-nm-thin gate oxides. For the gate electrode, 100-nm-thick in-situ phosphorus-doped poly-Si films were deposited by low pressure chemical vapor deposition (LPCVD). And then, the plasma immersion doping with phosphorous was followed for shallow source/drain formation at 450 °C temperature[7]. In order to evaluate the device performance of SGOI MOSFET, the pre-RTA at 900 °C for 30 sec in N_2 ambient was implemented before gate oxidation step, the conventional RTA process for dopant activation annealing was done at 850 °C for 10 sec, and the post-RTA treatment was applied at 500 °C for 30 min in a N_2 ambient.

3. RESULTS AND DISCUSSION

Figure 1 shows the SEM (scanning electron microscopy) image of SGOI n-MOSFET devices to characterize the current characteristic as a function of the Ge concentration in the SiGe layer. The gate length and the channel width of strained-Si SGOI n-MOSFET was in the range of 2-20 μm, and the mesa isolation technology was used for Si active region definition.

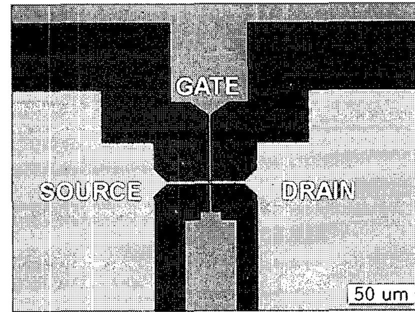
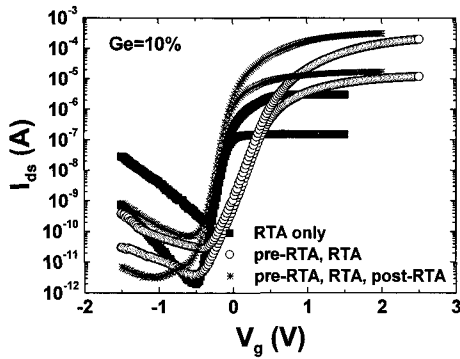
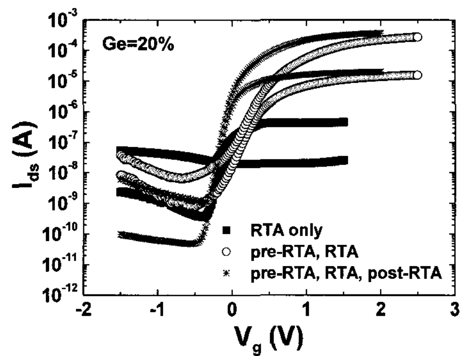


Fig. 1. Optical microscope images of strained-Si SGOI n-MOSFET device.

Figure 2 shows the I_{ds}-V_g characteristics of strained-Si SGOI n-MOSFET with 10 and 20 % Ge content, where V_d was 0.1 or 1 V. The results show the effects of applying RTA only, the pre-RTA process, and both the pre-RTA and post-RTA processes. The pre-RTA process significantly enhanced the drain current as compared to that with RTA only, as shown by the open squares. This could probably be attributed to the pre-RTA process accelerating the dopant activation annealing. Degradation of the subthreshold swing was observed, however, because of the generation of a large mechanical stress at the interface between the gate oxide and the strained-Si channel. On the other hand, the combination of the pre-RTA, RTA, and post-RTA processes after source/drain activation annealing significantly enhanced the drain current by two orders of magnitude as compared to that with RTA process only. Applying all three annealing steps also improved the subthreshold slope of the strained-Si SGOI n-MOSFET from 156 mV/dec to 75 mV/dec. This improvement is associated with the reduction of interfacial trap density (D_{it}) at gate oxide/strained-Si channel. Because the post-RTA process is effective for relaxation of stress at interface at the gate oxide/ strained-Si channel, the conduction characteristics at subthreshold region were improved. Also, it is found that the leakage current of MOSFET considerably decreased by applying both the pre-RTA and post-RTA processes, especially in 20 % Ge content.



(a) 10 % Ge content



(b) 20 % Ge content

Fig. 2. I_{ds}-V_g characteristics obtained from the SGOI n-MOSFET devices. Closed squares correspond to without the pre-RTA treatment before gate oxidation, and open circles correspond to the pre-RTA treatment. Closed triangles correspond to the combination of pre-RTA before gate oxidation and post-RTA furnace annealing after source/drain activation.

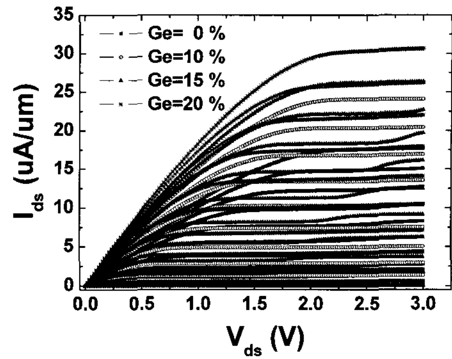


Fig. 3. I_{ds}-V_{ds} characteristics obtained from the SGOI n-MOSFET devices for 0 %, 10 %, 15 %, and 20 % Ge content in relaxed $Si_{1-x}Ge_x$ layer.

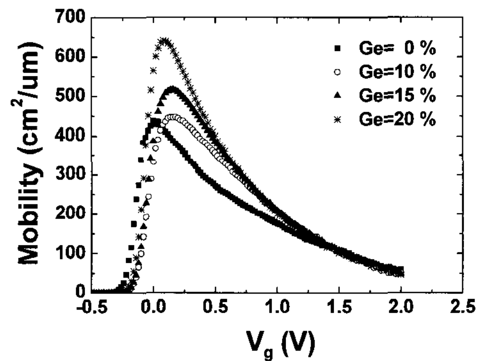


Fig. 4. Enhancement of electron mobility in strained-Si MOSFET as a function of Ge content of relaxed SiGe layer in SGOI substrates.

Figure 3 shows the I_{ds}-V_{ds} characteristics of SGOI n-MOSFET devices with 0, 10, 15 and 20 % Ge content. These results were obtained from the optimized heat treatment process. It is found that the drain current increased with the Ge content in SiGe layer. This is attributed to the fact that a mobility enhancement of electrons in the strained-Si inversion layer increases with Ge content in the SiGe layer, because the amount of strain in the strained-Si layer is proportion to the Ge content of SiGe layer[8,9].

Figure 4 shows the field effect mobility of strained-Si SGOI n-MOSFET devices as a parameter of Ge content. By applying both pre-RTA before gate oxidation and post-RTA after gate oxidation process, the significant enhancement of electron mobility in strained-Si layer SGOI MOSFET was achieved. Optimal process conditions of the pre-RTA were 900 ℃ for 30s and the post-RTA was 500 ℃ for 30 m in N_2 ambient.

The enhancement of mobility were 2.8, 18.9 and 47.4 % for 10, 15 and 20 % Ge contents,

Table 1. Enhancement of field effect mobility of strained-Si SGOI n-MOSFET as a function of Ge contents after optimized heat treatment processes.

Ge contents (%)	Mobility (cm^2/Vs)	Enhancement (%)
0	435	-
10	447	2.8
15	515	18.9
20	641	47.4

respectively, as shown in Table 1. Therefore, we can conclude that the addition of pre-RTA and post-RTA process is very effective for improving the electrical characteristics of nano-scale strained-Si channel SGOI n-MOSFETs.

4. CONCLUSION

In summary, the electric characteristics of strained-Si channel SGOI n-MOSFETs were degraded as the Ge concentration in $Si_{1-x}Ge_x$ layer increased. By applying the additional pre- and post-RTA process, the driving current, transconductance, and leakage current were significantly improved. Therefore, the addition of pre- and post-RTA process, consisting of 30 sec at 900 °C and 30 min at 500 °C in a N_2 ambient, was very effective in improving the electrical characteristics of nano-scale strained-Si channel SGOI n-MOSFETs.

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