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Fabrication of SOI FinFET Devices using Arsenic Solid-phase-diffusion

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Abstract

A simple doping method to fabricate a very thin channel body of the nano-scaled n-type fin field-effect-transistor (FinFET) by arsenic solid-phase-diffusion (SPD) process is presented. Using the As-doped spin-on-glass films and the rapid thermal annealing for shallow junction, the n-type source-drain extensions with a three-dimensional structure of the FinFET devices were doped. The junction properties of arsenic doped regions were investigated by using the n^+-p junction diodes which showed excellent electrical characteristics. The n-type FinFET devices with a gate length of 20-100 nm were fabricated by As-SPD and revealed superior device scalability.

Key Words : Solid phase diffusion, Ultra-shallow junction, Nano-scale, FinFET, As-doped spin-on-glass

1. INTRODUCTION

The metal-oxide-semiconductor field-effect-transistor (MOSFET) is the most dominant electronic device in integrated circuit manufacturing. As the dimension of silicon MOSFETs shrinks to sub-100 nm regime, reducing the short channel effects becomes major efforts for the further scaling down of nano-scaled complementary metal-oxide-semiconductor (CMOS) device applications. To overcome the short channel effects, some modified MOSFET device structures have been proposed to improve the short channel effects immunities[1-3]. Multiple-gate MOSFET (MUG FET) is considered as the promising devices for CMOS scaling into deep sub-100 nm gate lengths due to the more effective energy barrier controllability between the source and drain by the gate bias[4-6]. The FinFET has vertical silicon channels of fin-shape and self-aligned double-gate structure and reported as a promising device technology for the post-CMOS device applications[7]. However, three-dimensional device architecture of FinFET leads to more complicate processing especially the doping of source/drain extension regions in comparison with the conventional planar CMOS transistors[8]. The solid phase diffusion (SPD) process is an alternative doping method for three-dimensional device architecture. Since the SPD process uses the thermal diffusion of impurity from the dopant source to the substrate instead of implanting accelerated atoms, it is known as a defect-free process[9].

Therefore, we investigated the fabrication of n-type FinFET devices by arsenic SPD using the As-doped spin-on-glass films as n-type impurity diffusion source. The n^+-p junction diodes with an ultra shallow junction depth were fabricated by arsenic SPD and the electrical properties of diodes were characterized. In addition, the n-type FinFET devices with a gate length of 20-100 nm was fabricated by arsenic SPD and the electrical characteristics were evaluated.

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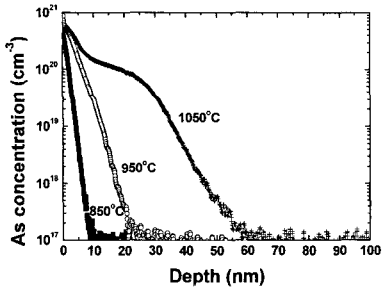


Fig. 1. SIMS profiles of arsenic for various RTA process temperatures.

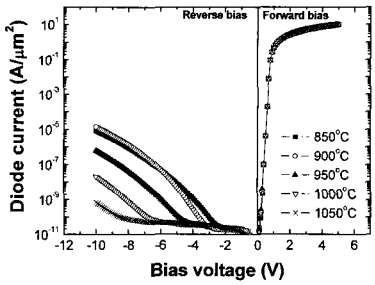


Fig. 2. I-V characteristics of n^+-p diode fabricated by arsenic SPD methods with a parameter of RTA temperature.

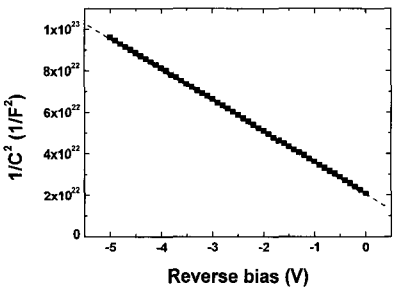


Fig. 3. $1/C^2$-V curves of n^+-p ultra shallow junction doped by As at temperature of 900 °C.

2. EXPERIMENTAL

The p-type silicon-on-insulator (SOI) wafers with 200 nm buried oxide layer and 100 nm top silicon layer were used for n-type FinFET's fabrication. Silicon fin channels with a width of 20 nm were obtained by EBL and Cl_2-based inductively coupled plasma reactive ion etch (ICP RIE) process. A gate oxide with a thickness of 4 nm was grown by dry oxidation and an in-situ phosphorus-doped poly-Si film with a 100 nm thickness was deposited as a gate electrode using the low-pressure chemical-vapor deposition (LPCVD). Poly-Si gate electrodes were formed by patterning of electron-beam lithography (EBL) and etching of ICP RIE process. The silicon nitride film with 20 nm thickness was deposited by LPCVD and was etched back to form the sidewall spacer. A liquid-state dopant source containing arsenic was used as a SPD source. A liquid-type dopant source was changed to a solid-state As_2O_5 layer by baking processes in N_2 ambient. A rapid thermal annealing (RTA) with high ramp-up rate (+50 °C/s) and ramp-down rate (-50 °C/s) was carried out in N_2 ambient at 950 °C for diffusing the arsenic to the source-drain extensions of n-type FinFET devices.

3. RESULTS AND DISCUSSION

Figure 1 shows the SIMS profiles of arsenic for various temperatures of RTA process. The arsenic atoms were gradually diffused from the doping source layer to the silicon substrate by thermal energy and the diffusion length of arsenic was increased with increasing RTA temperature. In order to suppress the short-channel effect in nano-scaled CMOS technologies, a shallow junction is required. As shown in Fig. 1, an ultra-shallow junction depth less than 20 nm can be successfully obtained at 950 °C.

Figure 2 shows the current-voltage (I-V) characteristics of n^+-p diodes fabricated on the silicon substrate by SPD as a parameter of RTA temperature. The reverse bias current decreased with increasing temperature, because the junction depth increased with diffusion temperature. On the other hand, the forward bias current increased with RTA temperature, which is attributed to the reduction of resistance at arsenic doped region.

Figure 3 shows a plot of $1/C^2$ versus reverse bias for diodes fabricated by SPD from the As containing spin-on-glass films at RTA temperature of 900 °C. For the ultra shallow and abrupt junction, i.e., one-sided step junction, a square of reciprocal of capacitance induced by space charge in depletion region is proportional

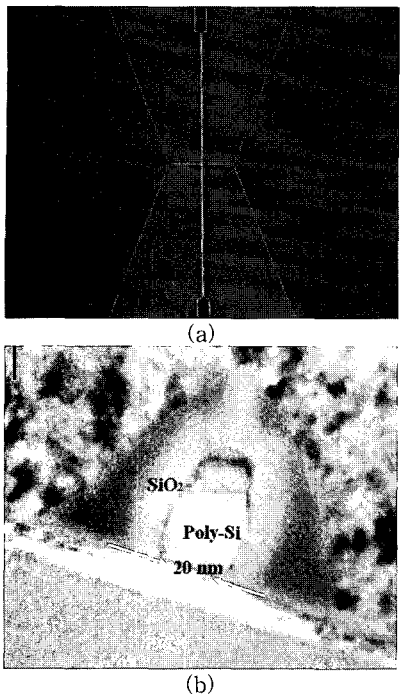
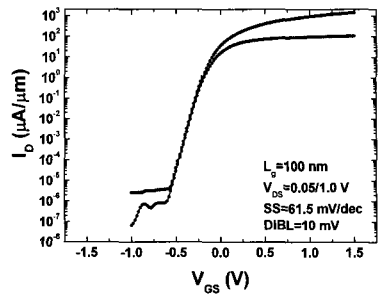
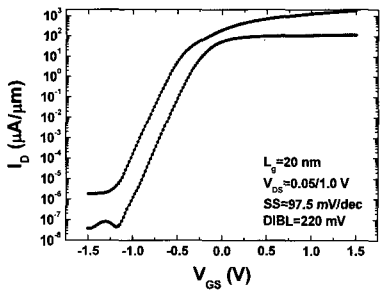


Fig. 4. Plane-view SEM image (a) of fabricated FinFET with a 20 nm gate length and cross-sectional TEM image of gate line (b).



(a) 100 nm gate length



(b) 20 nm gate length

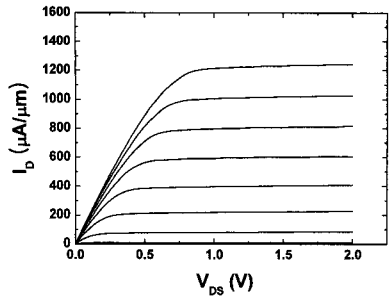
Fig. 5. I_d-V_g characteristics of n-type FinFETs.

to reverse bias voltage. As depicted in Fig. 3, $1/C^2$-V curves are linear, which demonstrate that junctions fabricated by SPD have a feature of one-sided step junction.

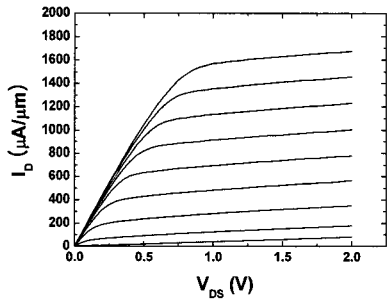
Figure 4 shows the plane - view scanning electron microscope (SEM) image of FinFET device and the cross-sectional transmission electron microscopy (TEM) image of poly-Si gate electrode with a 20 nm length. The nitride sidewall spacer of poly-Si gate electrode with a 20 nm thickness was also observed. In order to pattern the fin channels, the electron-beam lithography was used. The hydrogen silsesquioxane (HSQ, Fox-12, Dow Corning) film with 100 nm thickness was used to generate the ultra-fine fin-type channel and gate electrode patterns. This HSQ layer played an important role as hard mask of dry etching process. After formation of Si_3N_4 sidewall spacer, a liquid-type dopant sources were spin coated and a RTA was carried out for doping of the source-drain extension regions.

Figure 5 shows the subthreshold current characteristics (I_d-V_g) .for the n-type FinFET devices with the gate length of 100 nm and 20 nm. It is found that excellent subthreshold characteristics were obtained by the As-SPD process. The subthreshold swing and DIBL (drain induced barrier lowering) for 100 nm gate length were 61.5 mV/dec and 10 mV, respectively. This subthreshold swing is almost equivalent to the ideal value of silicon MOSFET device (60 mV/dec at room temperature). On the other hand, the subthreshold swing of 97.5 mV/dec and DIBL of 220 mV were obtained from the 20 nm gate length FinFET.

Figure 6 shows the drain voltage-drain current (I_d-V_{ds}) characteristics of n-type FinFETs with the gate length of 100 nm and 20 nm. The short channel effect was not observed in arsenic SPD FinFET even in 20 nm gate length. From these results, we can conclude that the arsenic SPD process is a promising doping technology for the further device scaling of nano-scale n-type FinFET devices.



(a) 100 nm gate length



(b) 20 nm gate length

Fig. 6. I_d-V_{ds} characteristics of n-type FinFETs.

4. CONCLUSION

A shallow-junction formation technique for the fabrication of n-type FinFET device with sub-100 nm gate length was reported. Using the arsenic SPD process with As-doped spin-on-glass diffusion source, the n-type FinFETs with gate length of 20-100 nm and the n^+-p junction diodes with extremely shallow junction depth were fabricated. Arsenic SPD was proved to be very effective process for sub-100 nm CMOS technology, because the n^+-p junction diodes with shallow junction depth and the n-type FinFET devices with a 20 nm gate length showed good electrical characteristics. Therefore, we concluded that the arsenic SPD process using the As-doped spin-on-glass films was a promising doping technique for the further device scaling of nano-scale n-type FinFET devices.

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