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갈로이스 부분장 변환을 이용한 새로운 고속의 경제적 치엔탐색기의 설계법에 대하여

(New Fast and Cost effective Chien Search Machine Design Using
Galois Subfield Transformation)

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요 약

리드솔로몬 복호기에서 4중 오류 이상의 오류치와 위치를 발견해 정정하는 보통 치엔탐색기를 사용한다. 이때 기존의 방법은 회로량이 많고 지연시간이 길어 비효율적이었다. 본 논문에서는 갈로이스 부분장을 이용 이 탐색기를 속도도 빠르고 회로량도 대폭 줄인 새로운 효율적 탐색기회로 설계법을 제시한다. 본 논문에서는 4중 오류위치를 정확히 추출함을 보였으나, 이새 설계된 탐색기회로는 5중이상의 오류위치도 정확히 찾을 수 있는 설계이다. 새로운 회로는 정확히 오류위치를 발견할 수 있음이 예를 통해 검증되었다.

Abstract

In Reed Solomon decoder, when there are more than 4 error symbols, we usually use Chien search machine to find those error positions. In this case, classical method requires complex and relatively slow digital circuitry to implement it. In this paper we propose New fast and cost effective Chien search machine design method using Galois Subfield transformation. Example is given to show the method is working well. This new design can be applied to the case where there are more than 5 symbol errors in the Reed-Solomon code word.

Keywords: RS(Reed Solomon), Decoder, Error Locator polynomial, Galois Field(GF), Chien search machine, Newtonian Identities, Subfield Transformation, Number of Errors

I. Introduction

Reed Solomon coding theory is very famous well known nonbinary error correction method for Digital

Electronic Devices (Consumer and Communication products.)^[3].

In this paper, new RS(Reed Solomon) Decoder, which is correcting more than 4 symbol 1 errors, design method is proposed using Galois Subfield Transformation^[5]. This method can be used when there are less than 4 error symbols, but in this case there are more efficient method which is described author's another paper^[1,7].

In chapter 1 Introduction is written to introduce the whole paper. In chapter II, we briefly described how the Newtonian identities are used to determine the number of error symbols in the codeword. In

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chapter III we describe two types of classical Chien Search Machine design methods are described and two methods are compared from each other^[9]. In Chapter IV we describes new efficient (fast and economical) chien search machine design method. The new design uses Galois subfield transformation from $GF(2^4)$ to $GF(2^8)$ field to simplify the Galois elements arithmetic operation^[2].

Here we design various subcircuits, for example, $**2$ (Square), and $**3$ (exponent power of 3) calculator circuits. The total number of gates and propagation delay is greatly reduced compared with those of classical chien searchmachine described in chapter 3. In this chapter we proves that the new circuit is working well by finding 4 error locations of arbitralily given error locator polynomials which has 4 solutions corresponding to 4 error locations, using the new machine.

In chapter V future works that will be taken by us, and Comparisons between Old design and New design are described.

II. Error Locator polynomial and determination of number of error symbols in the RS codeword

The RS(Reed Solomon) codes are based on finite fields, often called Galois fields.

In CDP, RSC(32,28), on $GF(2^8)$ field, code is used and up to 2 symbol errors can be corrected^[1].

An RS code with 8bit symbols will use a Galois field $GF(2^8)$, consisting of 256 symbols. In decoding Reed-Solomon code, we should calculate the Syndromes as in equation 1.

Let

$$C(X) = \sum_{j=0}^{n-1} C_j X^j$$

Be the Transmitted polynomial, and let

$$r(X) = \sum_{j=0}^{n-1} r_j X^j$$

Be the received polynomial. Then error pattern of the channel is

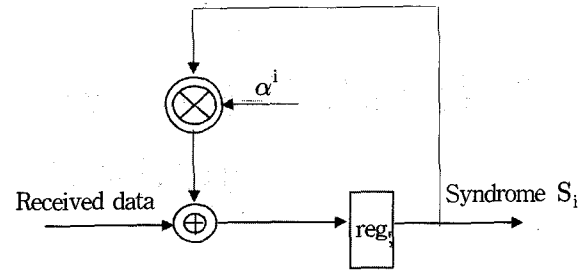


그림 1. RS 복부호기의 신드롬 계산기

Fig. 1. Syndrome calculator of RS codec.

$$E(X) = \sum_{j=0}^{n-1} E_j X^j$$

Where E_j ($j = 0$ to $n-1$) are error values. Here Syndromes are defined as

$$S_i = E(\alpha^i) (i = 0, 1, \dots, 2t-1) \quad (1)$$

For t error correction coding.

In this paper, for finding Error values and positions, syndrome calculator shown in Fig.1 is used^[6].

Now if there are t errors, error values are E_n ($n=0, 2\cdots, t-1$) and their positions are α^{j^n} ($n=0, 1, \dots, t-1$).

Then Let

$$\beta_j (j = 0, 1, \dots, t-1) = \alpha^{j^n} (n = 0, 1, \dots, t-1)$$

and Error Locator polynomial is defined as

$$\begin{aligned} \delta(X) &= (X - \beta_0)(X - \beta_1) \cdots (X - \beta_{t-1}) \\ &= \sum_{k=0}^t X^k \delta_{t-k} \end{aligned} \quad (2)$$

Now Newton's identities are following set of equations.

$$\sum_{j=1}^t S_{t-j+v} \delta_j = S_{v+t} (v = 0, 1, 2, \dots, t-1) \quad (3)$$

These equations are for t error correcting Reed-Solomon codec^[9]. Now let's define

$$A_i = [S_{v-1} S_{v+1-1} S_{v+2-1}]^T, \text{ for } i = 0, 1, 2, \dots, v-1 \quad (4)$$

Here If

$$F(v-1) = \det[A_0 A_1 A_2 \cdots A_{v-1}] \quad (5)$$

Then if $F(v-1) \neq 00$ and $F(v) \equiv 0$, there are

v errors in the One Reed Solomon codeword^[4].

In these days, Equation (3) are solved using only 1 Multiplier and embedded Software coding to control the Main CPU core(Noramlly Arm core) of the system(Digital A/V system, for example, CDP, DAT, HDTV, etc.). So we get the coefficients δ_j 's of error locator polynomial (2).

III. Classical Chien Search Machine

In this section, we describe 2 types of currently used Chien search machine^[4,9]. The machine here and New design described in next section can be applied to finding any number of Errors in the code word.

1) First type

For less than 3 symbol errors in the RS ECC decoder, please see the Author's another paper^[1,3]. For more than 4 symbol errors in the RS codeword, we usually use Chien search machine shown in Fig. 2^[9]. If Chien search machine is used for less than 3 symbol error case for RS decoder, it is very inefficient in speed and costwise. Chien search machine finds out all the solutions(i.e., error locations) of error locator polynomials, Equation (2) (in this case order of the equation is 4, so there are 4 solutions for the equation (6))^[4]. Synchronized to the clock pulses, The Multipliers are connected to the D type F/Fs and They output α^{4i} , α^{3i} , α^{2i} , α^i ^[5]. So The machine's out Z becomes 0 when α^i is the solution (i.e., error location). In this way, the Machine finds out all 4 error locations sequentially (increasing order). Definitely for more than 5 error case, in same way the machine works.

Following Fig. 2. is a typical Chien Search Machine finding 4 symbol errors. But as you see, the circuitry is relatively complex and the speed is slow since everytime it iterates it requires accumulated multiplication, so becomes slow. The number of multiplier in GF(2⁸) field is 7, and there are 4 8-bit Filpflops(Registers).

The output $Z = \delta_4 + \alpha^i \delta_3 + \alpha^{2i} \delta_2 + \alpha^{3i} \delta_1 + \alpha^{4i} = 0$,

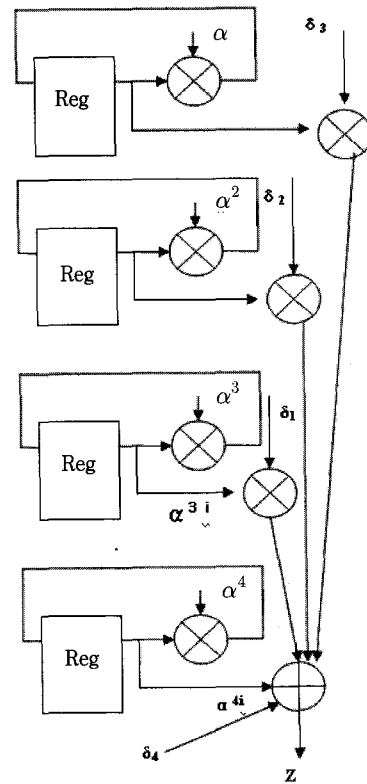


그림 2. 첫 번째 유형의 치엔 탐색기 구조圖 (4중 오류의 경우)

Fig. 2. Type 1 Classical Chien Search machine. (4 Error case)

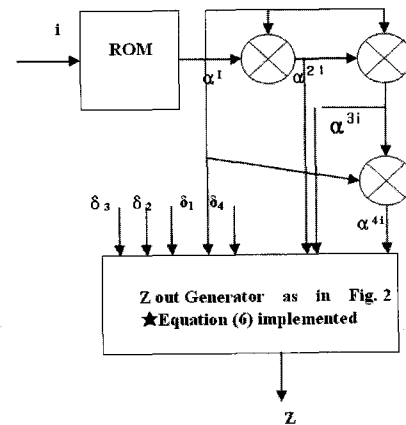


그림 3. 두 번째 유형의 치엔 탐색기 구조圖

Fig. 3. Type 2 Classical Chien Search machine.

when α^i is correct error position.

The Gate Count for Z out Generator(Equation (6)) is same as in Fig. 2. But I to α^i Transform ROM is anyway needed for other part of ECC block also, then Type 2 is definitely simpler than Type case (Type 2 needs only 3 Multipliers comparing 4 Multipliers of Type 1 case (excluding Zout cct) and

no needs of Flip Flops. Also clock cycle period of type 1 is longer than 3 series propagation delays of type 2 case, so Type 2 Processing speed is faster than that of type 1.

$$Z = \delta_4 + \alpha^1 \delta_3 + \alpha^{21} \delta_2 + \alpha^{31} \delta_1 + \alpha^{41} \quad (6)$$

IV. New Chien Search Machine Design for Reed-Solomon Decoder in GF(28)

In this chapter we describe new chien search machine structure using GF(2⁸) to GF(2⁴) Transformation^[5]. Let's see Fig. 4 for the whole structure of the machine. The structure is composed of 3 parts (Transform part, HW of each exponent implementation, Z out generation part in GF(2⁴)). Here we don't need Inverse transformation from GF(2⁴) to GF(2⁸), so resulting in additional saving the hw circuitry of the machine. The main idea of saving the HW circuit amount is the big simplification of

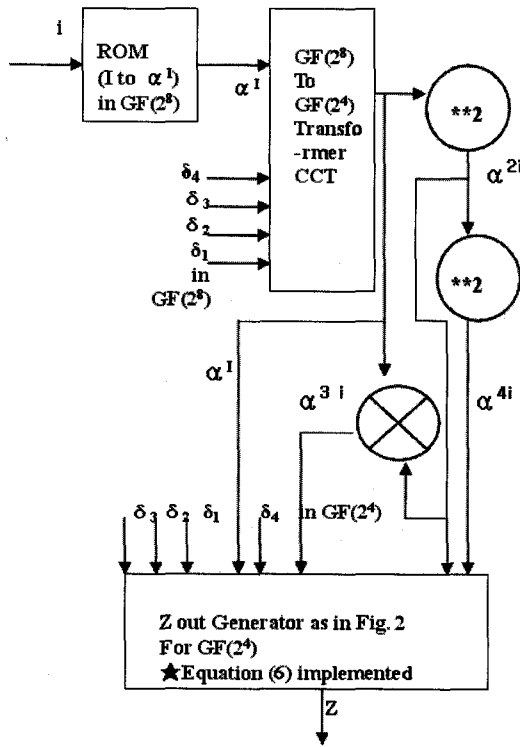


그림 4. 새로운 유형의 치엔 탐색기 구조圖
(4중 오류의 경우)

Fig. 4. New Chien Search machine Block Diagram.
(4 symbol Error case)

HW circuit in GF(2⁴) field and **2 circuit is much simpler than the multiplier circuit in GF(2⁴) field^[5].

Let's analyse the Circuit in Fig.4. There are 3 Kind of subcircuits in the machine. 1st Sub block is GF(2⁸) to GF(2⁴) Transfer circuit. The logic equation is as follows^[5].

$$\text{IF } A = A_0 + \beta A_1, \text{ where } A, \beta \in \text{GF}(2^8)$$

$$\text{And } A_0, A_1 \in \text{GF}(2^4) \quad (7)$$

$$\text{Also } A = (b_0, b_1, b_2, b_3, b_4, b_5, b_6, b_7) \text{ and}$$

$$A_0 = (Z_0, Z_1, Z_2, Z_3), A_1 = (Z_4, Z_5, Z_6, Z_7)$$

$$\begin{aligned} Z_0 &= b_0 + b_1 + b_5 \\ Z_1 &= b_1 + b_3 + b_5 \\ Z_2 &= b_2 + b_3 + b_6 \\ Z_3 &= b_1 + b_3 + b_4 + b_6 \\ Z_4 &= b_1 + b_2 + b_3 + b_5 + b_6 + b_7 \\ Z_5 &= b_2 + b_5 + b_6 \\ Z_6 &= b_1 + b_2 + b_3 + b_4 + b_5 + b_6 \\ Z_7 &= b_1 + b_3 + b_4 + b_5 \end{aligned} \quad (8)$$

Now Multiplier in GF(2⁴) is IF

$$\begin{aligned} C &= AB \\ &= (A_0 + \beta A_1)(B_0 + \beta B_1) \\ &= (C_0 + \beta C_1) \end{aligned}$$

where $A_0, A_1, B_0, B_1, C_0, C_1 \in \text{GF}(2^4)$.

Then

$$\begin{aligned} C_0 &= A_0 B_0 + A_1 B_1 \lambda, \lambda \in \text{GF}(2^8) \\ C_1 &= A_0 B_1 + A_1 B_0 + A_1 B_1 \end{aligned} \quad (9)$$

So the Multiplier in GF(2⁴) requires 4 multipliers over GF(2⁴), 3 adders over GF(2⁴) and a λ multiplier over GF(2⁴). Now IF $A=B$, then equation (9) becomes **2 (Square) circuit in Fig. 4^[5]. In this case(9) becomes equation (10) as follows.

$$\begin{aligned} C_0 &= A_0^2 + A_1^2 \lambda \\ C_1 &= A_1^2 \end{aligned} \quad (10)$$

This circuit of equation (9) is really simple as if $A_0 = (x_0, x_1, x_2, x_3)$, $A_0^2 = (x_0 + x_2 + x_3, x_3, x_1 + x_3, x_2 + x_3)$ and λA_0 is $(x_3, x_0, x_1, x_2 + x_3)$, because λA_0 is, when $A_0 = x_0 + x_1 \lambda + x_2 \lambda^2 + x_3 \lambda^3$, $x_0 \lambda + x_1 \lambda^2 + x_2 \lambda^3 + x_3 \lambda^4 = (x_0 + x_2 + x_3, x_3, x_1 + x_3, x_2 + x_3)$ and A_0^2 is $x_0 + x_1 \lambda^2 + x_2 \lambda^4 + x_3 \lambda^6 = (x_0 + x_2 + x_3, x_3, x_1 + x_3, x_2 + x_3)$ using $\lambda^4 = \lambda^3 + 1$ (the primitive polynomial of GF(2⁴)). So $A_0^2 \lambda = (x_2 + x_3, x_0 + x_2 + x_3, x_3, x_1 + x_2)$ ^[5].

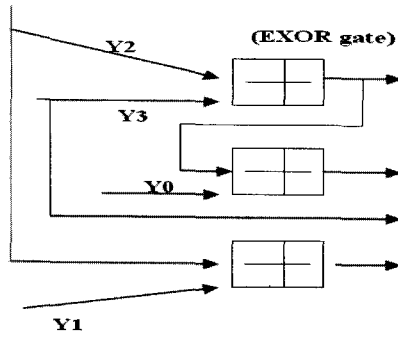


그림 5. A12 λ 형성회로

Fig. 5. A12 $\lambda = (Y2+Y3, Y0+Y2+Y3, Y3, Y1+Y2)$ Circuit.
 $**A1 = (Y0, Y1, Y2, Y3)$.

So the equation (9) requires 9 EXOR gates totally and $A1^2 \lambda$ circuit is drawn in Fig.5.

<Example1>

If the Error locator polynomial over $GF(2^8)$ is

$$(x + \alpha)(X + \alpha^2)(X + \alpha^3)(X + \alpha^4) \\ = X^4 + X^3\delta_1 + X^2\delta_2 + X\delta_3 + \delta_4$$

$$\text{So } \delta_1 = \alpha^{76}, \delta_2 = \alpha^{76}, \delta_3 = \alpha^{81}, \delta_4 = \alpha^{10}.$$

These Values are normally calculated from Newtonian identity equations (3) using known Syndromes^[8]. Now Find 4 correct error locations $\alpha, \alpha^2, \alpha^3, \alpha^4$ using New Chien Search Machine.

<Solution>

All $\delta_i (i = 1 \text{ to } 4)$ and $\alpha^i (i = 1)$ are transformed to $GF(2^4)$ elements using equation (8) as follows^[5].

$$\begin{aligned} \delta_1 &= \alpha^{76} = \alpha^4 + \beta\alpha^5 \\ \delta_2 &= \alpha^{251} = \alpha^{10} + \beta\alpha^7 \\ \delta_3 &= \alpha^{81} = 1 + \beta\alpha^{12} \\ \delta_4 &= \alpha^{10} = \alpha^{12} + \beta\alpha^{12} \quad \text{Also} \\ \alpha^i &= \alpha = \alpha^5 + \beta\alpha^{11} \end{aligned}$$

Now using Square circuit (**2) and Multiplier circuit for Equations (9) and (10) in Fig.4, we find in $GF(2^4)$ field

$$\alpha^{2i} = \alpha^2 = \alpha^2 + \beta\alpha^7 \text{ and}$$

$$\alpha^{3i} = \alpha^3 = \alpha^8 + \beta\alpha^{11},$$

$$\alpha^{4i} = \alpha^4 = \alpha^3 + \beta\alpha^{14}$$

Finally Zout Generator detects whether out is zero

or not as follows.

LSB Part in $GF(2^4)$, $\alpha^{12} + \alpha^8 + \alpha + \alpha^7 + \alpha^3 = 0$ and MSB Part in $GF(2^4)$, $\alpha^{12} + \alpha^7 + \alpha^{11} + \alpha^9 + \alpha^{14} = 0$. So $\in GF(2^8)$ is really correct Error position. For $\alpha^i (i=2,3,4)$, we find They are also correct error positions.

★★ See EX2 for $i=2$ case !!

<Example 2>

For $i=2$ case : Now let's verify that α^2 is another Error location.

<Solution>

$\alpha^i = \alpha^2 = \alpha^2 + \beta\alpha^7$ using Transform circuit, In Fig. 4 (Equation 8) and similarly,

$$\begin{aligned} \alpha^{2i} &= \alpha^4 = \alpha^3 + \beta\alpha^{14} \\ \alpha^{3i} &= \alpha^6 = \alpha^{14} + \beta\alpha^7 \\ \alpha^{4i} &= \alpha^8 = \alpha^{12} + \beta\alpha^{13} \end{aligned}$$

using Square circuit and Multiplier of Fig. 4 in $GF(2^4)$. Now Finally we find Z out is also Zero and catch that α^2 is also Correct Error position.

V. Conclusion and Discussion

Classical Type 1 Chien machine is better for System synchronization control than Type 2 machine so more widely used than type 2 machine .

So here we compare type 1 and New Chien machine for gate counts and speed. Anyway Type2 is smaller than Type 1 machine, and has about 80% gate Counts. Type 1 machine and New machine has same Z generator equation. But gate countes are different from each other. If we assume F/Fs of Type 1 machine and ROM of new design have almost same size, so we 'd better compare the circuit section just after F/F and ROM(i to α^i) of two Chien machines. Table 1 shows the summary of 2 machine comparison.

Here We see our New Design is really Cost efficient (Gate Count of New design is about 57% gate count of the old design). Also, The speed of

표 1. 고전적 치엔 머신과 새로운 치엔 머신의 회로소자(앤드와 엑스오아 게이트) 갯수 비교표

Table 1. Gate count Comparison between New design and Classical Chien machine.

	#of EXOR gates	# of AND gates	Remark
Classical Type 1 machine	7X73 = 511	7X64=448	7 Multipliers in $GF(2^8)$
New Chien Machien	5X13+4X75+2X9=383	4X48=192	4 Multipliers and 2 Squaring circuits ($**2$) in $GF(2^4)$. Also $GF(2^8)$ to $GF(2^4)$ Transfer Circuit for δ_i s and α^i

New design is faster than that of Type 1 machine since propagation delay path is much shorter for New design than for Type 1.

Future Work is for Economic design of Reed Solomon Encoder^[3]. Here we want to design very fast and low cost GF field Arithmetic operator circuit^[2].

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