JOURNAL OF KOREA MULTIMEDIA SOCIETY, VOL. 10, NO. 12, DECEMBER 2007(pp. 1585-1590)

5-Tap Adaptive PRML Architecture for High-Density Optical Disc Channel

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ABSTRACT

This paper introduces adaptive PRML (Partial Response Maximum Likelihood) architecture with PR (a,b,c,d,e) channel type for the improved readability of high-density optical discs with capacity greater than 30GB. The proposed PRML architecture consists of an adaptive equalizer, a Viterbi detector and a channel identifier. Detailed description for each component is included. The architecture is implemented in chip and also confirmed its performance on the test board mounting the chip. Test results show that the proposed 5-tap PRML architecture is well operated, and less than 2×10^{-4} of BER (Bit Error Rate) is achieved with radial and tangential tilt margin of $\pm 0.6°$ on self-made 30GB BD at 1x speed.

Keywords: PRML, Adaptive Equalizer, Viterbi Detector

1. INTRODUCTION

The advent of IT era brings on enormous demand for storage and transmission for high capacity digital data. Of all storage elements, an optical disc is more convenient and cheaper than any other storage elements, and can be a primary storage element used AV and PC applications. After introducing CD (Compact Disc) in 1982, the optical disc has been an important role as a media in storing the digital data. In the mid-1990s, the DVD emerged for movies in SD (Standard Definition) quality. Since its introduction, the market for DVD players has grown rapidly, making them a very successful consumer product. The DVD has the capacity to store SDTV broadcasts of more than two hours at 4-8Mb/s. However, after beginning of HDTV broadcasts, the need of high-density disc arises. To store HDTV broadcasts in 23-25Mb/s for more than two hours, more than the capacity of 23 GB (Giga Byte) is needed. Therefore, BD-RE format was announced in 2002[1]. All formats of BD including BD-ROM, BD-RE and BD - R are almost fixed in the end of 2005. In case of using the high-density optical disc such as BD, the disc noise increases and the signal-to-noise ratio (SNR) declines. Many different types of research have been carried out up to now to facilitate optical disc data detection in the presence of these problems [2-5]. In [3], the limit equalizer improves SNR without increasing inter-symbol-interference (ISI) and improves jitter and error rates during operation. In [5] and [6], the architecture of PR (a,b,a) PRML for 23GB BD-RE was presented. But its architecture is inadequate in application of high-density optical discs such as over 30GB optical disc.

In this paper, the 5-tap adaptive PRML architecture that can be applied to optical discs with capacity greater than 30GB is introduced. First, we briefly introduce the general optical disc system and the algorithm and architecture of 5-tap PRML having the improved readability. Then, the system including the proposed PRML architecture is implemented and tested. Finally, the conclusions are described.

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Receipt date : Mar 6. 2007, Approval date : Jul, 11. 2007
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2. GENERAL FRONT-END SYSTEM OF AN OPTICAL DISC SYSTEM

General optical system is electrically divided into 3 parts including RF, front-end and back-end block. Fig. 1 shows a simplified bock diagram of an optical disc system. The RF block interfaces with the pick-up and includes the functions of AGC (Automatic Gain Control), DC removal, balance adjustment, and offset adjustment to process the differential RF, tracking error, and focus error signals. It detects the envelope of a signal for adjustment of focus bias and performs the function of AGC to sustain the constant amplitude of a signal. It has also the function of the equalization, which compensates the high frequency components of a RF signal, following after the AGC. After the analog equalization, the differential equalizes RF outputs direct to the front-end block. The front-end block receives the RF signal and outputs the user data to the back-end block. In playback mode, the analog RF signal is entered into the front-end block, digitized with ADC (Analog to Digital Converter) and utilized in PLL (Phase-Locked Loop) to recover the channel clock. The PLL block extracts a synchronized clock with the input RF signal. It can be implemented in digital or mixed type. The recovered data from the PRML block are sent to the data processor including functions of demodulation, buffer management, error correction and so on. The front-end block also includes the servo block, which control the spindle and step motors for focus and track servo. The back-end block is involved in the source coding such as MPEG2 (Moving Picture Experts Group2) and H.264 and encryption such as CSS (Content Scrambling System), CPRM (Content Protection for Recording Media) and AACS (Advanced Access Content System).

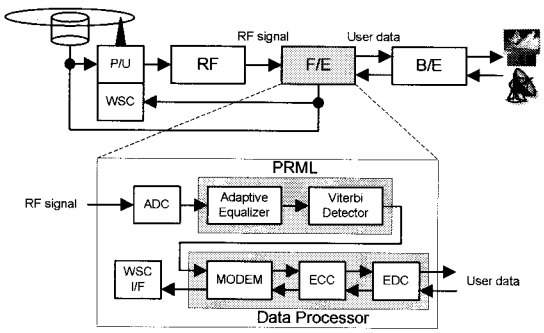


Fig. 1. A simplified block diagram of an optical disc system.

Hereafter, it will be focused on the PRML, which consists of an adaptive equalizer and a Viterbi detector, in the front-end block. The optical channel can be characterized by data density, track density, optical pick-up property, and so on. Generally, an adaptive equalizer adopts different PR type channel according to the disc characteristics. The adaptive equalizer in the previous BD system of [6] adopts PR (a, b, a) type channel. Generally, the adaptive equalization is processed by an adaptive digital FIR (Finite Impulse Response) filter together with a LED, and a LMS (Least Mean Square) calculator [2]. The Viterbi detector receives the output data of the adaptive equalizer and outputs a serial bit stream data to the data processor. After the receiving the serial data, the data processor demodulated the serial data, corrected the demodulated data with RS (Reed Solomon) decoder and transferred the corrected data to the back-end block through ATA (Advanced Technology Attachment) interface.

Because the system has PR (a, b, a) type channel and the 17PP modulation has the minimum run length of 2T, the values after the equalization will split into just four values [6]. T is the clock period of 1 channel bit. Fig. 2 shows conventional adaptive equalizer used in [6]. It consists of an 11-tap adaptive digital FIR filter, a LED and a LMS calculator. To optimize the tap coefficients of the FIR filter together, the level error detector stores 11-tap FIR filter outputs, and compare them in order to find the detected level of the outputs which is matched to the expected level of a target response within a given time interval. The LED subtracts the de

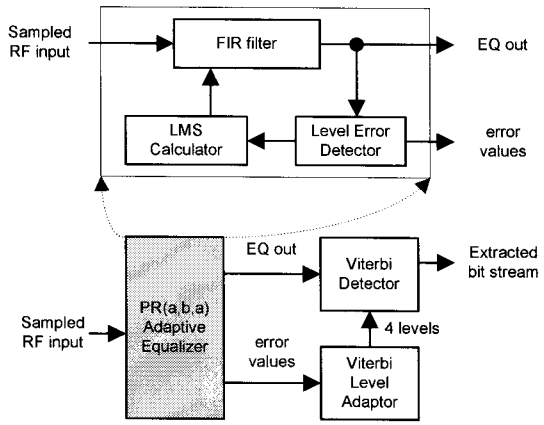


Fig. 2. Conventional Adaptive Equalizer.

tected level from the predetermined expected level of a partial response, and then the output error value for LMS calculation is determined.

Fig. 3 shows conventional Viterbi detector. The equalized output data of an adaptive equalizer are entered into the BMC (Branch Metric Calculator) to calculate BM. The calculated BM is selectively added through the ACS (Add Compare Select) according to the predefined trellis diagram. Then the bit serial data are extracted from the path memory block through the trace-back method and transferred to the demodulation block of the data processor.

3. PROPOSED ADAPTIVE PRML WITH PR (a,b,c,d,e) CHANNEL TYPE

Fig. 4 shows the block diagram of the proposed 5-tap PRML architecture. It consists of an adaptive equalizer, a Viterbi detector and a channel identifier. It also adopts PR(a,b,c,d,e) as the optical channel for high density optical discs such as BD. In the modulation of BD has minimum run length of 2T, the values after PR (a,b,c,d,e) equalization will split into just 16 reference values. For the minimum run length is 2T and the target channel is PR(a,b,c,d,e), the trellis diagram is shown in Fig. 5. The predetermined 16 levels are displayed in the right of Fig. 5.

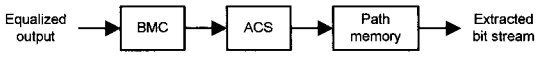


Fig. 3. Viterbi detector.

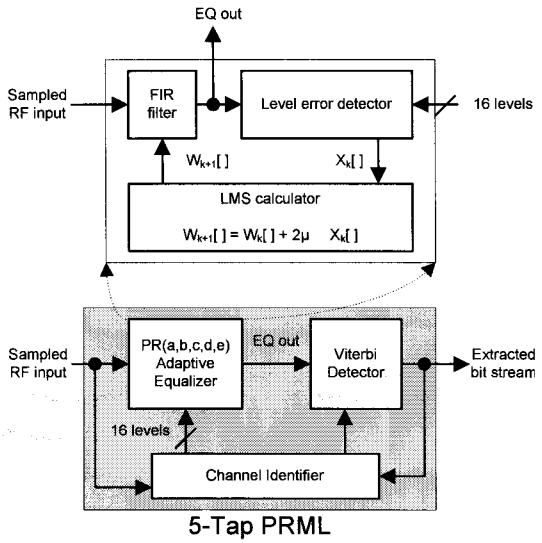


Fig. 4. Block diagram of the proposed PRML architecture.

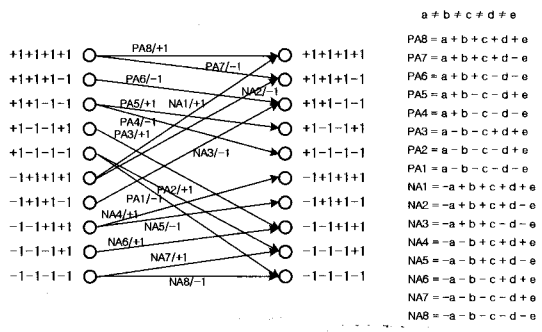


Fig. 5. Trellis diagram and 16 levels.

The adaptive equalizer is equivalent to the 11-tap FIR filter and its output to the output of the filter. After all the adaptation process is equivalent to the updating of the tap coefficients of the filter. The adaptive method is processed by LMS algorithm as follows:

$$W_{k+1} = W_k + 2 \cdot \mu \cdot \varepsilon \cdot X_k \qquad (1)$$

In here, W_{k+1}, W_k, X_k, ε, μ are new filter coefficients for (k+1)'th sample time, current filter coefficients at (k)'th sample time, input data placed

on all filter taps at (k)'th sample time, adaptation error, and adaptation gain. In equation (1), the adaptation gain, μ, is an invariable controlled by the system, but the adaptation error, ε, is a variable calculated. To update the tap coefficients of the filter, W_{k+1}, the adaptation errors, ε, is calculated in the LED. The architecture of the LED is shown in Fig. 6. The adaptation level errors are obtained from the predefined reference levels subtracted the output data of the filter. The processing delays between the filter outputs and the extracted bit stream, which selects the reference level among 16 reference levels, should be adjusted. The LMS calculator performs the function of equation (1). As you know, the 16 reference levels are not fixed. They should be changed according to the channel characteristics. The function of a channel identifier finds out suitable 16 levels that represent the channel characteristics with the 5-tap Viterbi structure and the adaptive equalizer. It selectively updates one level among 16 Viterbi levels at each sample time as follows:

$$L_{k+1} = L_k + d / c \qquad (2)$$

In here, L_{k+1}, L_k, d, c are the selected new level for (k+1)'th sample time, the selected current level at (k)'th sample time, the level error corresponding to the subtracted value the selected level from input data at (k)'th sample time, and the channel identification gain.

The presented Viterbi detector is similar to conventional Viterbi detector except for the number of reference levels. Fig. 7 shows one of the 16 BMCs. BM call "PA8 error," the absolute value of the difference between the FIR filter output signal and the predefined reference level, "PA8" which is generated from the channel identifier, is calculated. A total of 16 BM from "PA8 error" to "NA8 error" are calculated. According to the predefined trellis diagram, total 16 BMCs are necessary to feed forward to ACSs. The 16 reference levels calculated in the channel identifier are varied. ACS determines as the new state metric the smaller value

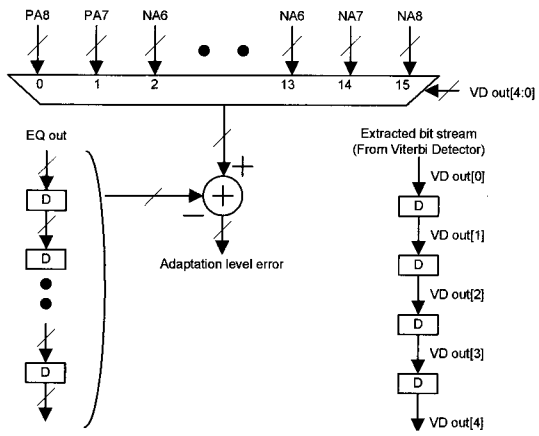


Fig. 6. Level error detector.

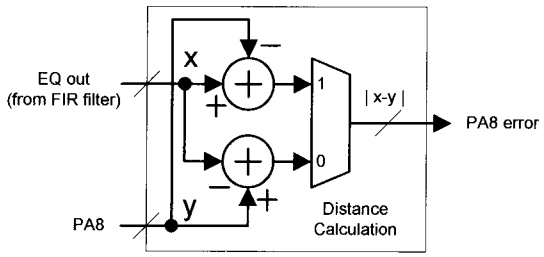


Fig. 7. Branch Metric Calculator.

obtained by adding two BM that are input to each state to the current state metric, as shown in Fig. 2. Fig. 8 shows the ACS that determines the state of "SM_1111" among the 10 states. In here, the signal of "sel_1111" is a control signal to be used in the path metric selector. Total 10 ACSs are existed to calculate the maximum likelihood. In this architecture, when overflow occurs, the normalized overflow values are replaced with the calculated metrics. Fig. 9 shows the architecture of the path memory select. The n-bit path memory data are

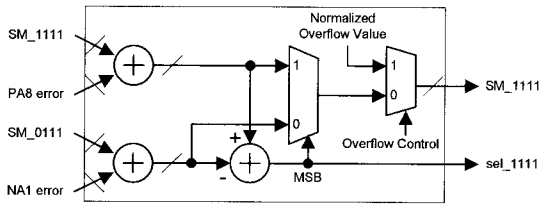


Fig. 8. Add-Compare-Select.

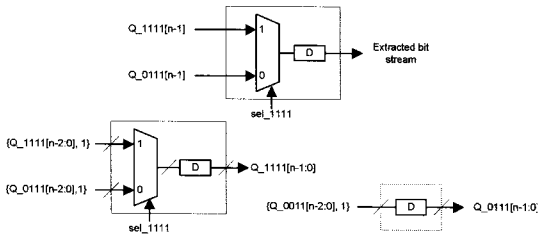


Fig. 9. Path memory selector.

selected with the control signals such as sel_1111 and sel_0111. In this scheme, the length of n is variable according to the system configuration.

4. IMPLEMENTATION AND TEST RESULTS

The front-end processor including the proposed PRML architecture is fabricated in 0.18-μm CMOS technology. Then, the test board mounting the fabricated chip is implemented as shown in fig. 10. To confirm the performance of the proposed 5-tap PRML architecture, the BER measurements are accomplished on self-made 30GB BD at 1x speed. Systems that use 3-tap adaptive PRML in which the conventional PR(a,b,a) was adopted and systems that include the limit equalizer showed a BER in the order level of 10^{-1} to 10^{-2} for a 30GB BD at 1x speed. Therefore, BER measurements were accomplished for just the system that contains the 5-tap adaptive PRML. Test results are shown in fig. 11. Fig. 11(a) shows BER according to the radial tilt. If the reference BER permitted by the system is assumed to be $2\times10-4$, the proposed 5-tap PRML architecture has a good performance of radial tilt margin of more than ±0.6°. Fig. 11(b) shows BER depending in tangential tilt. It shows similar results to those in radial tilt.

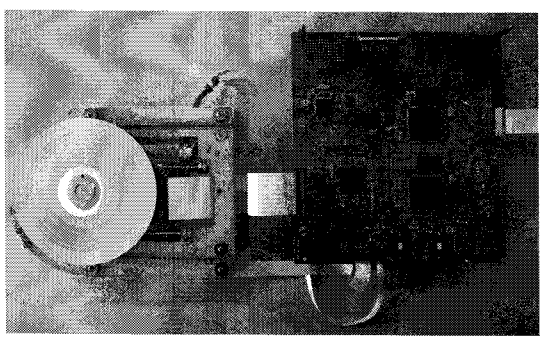
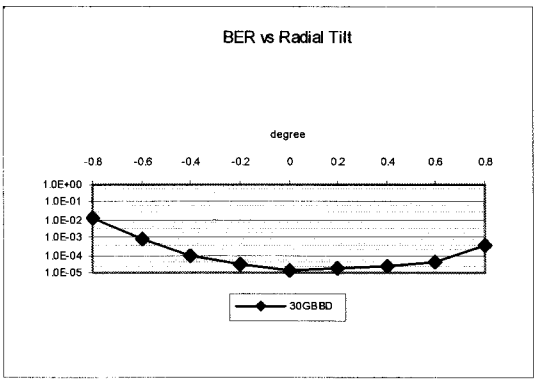
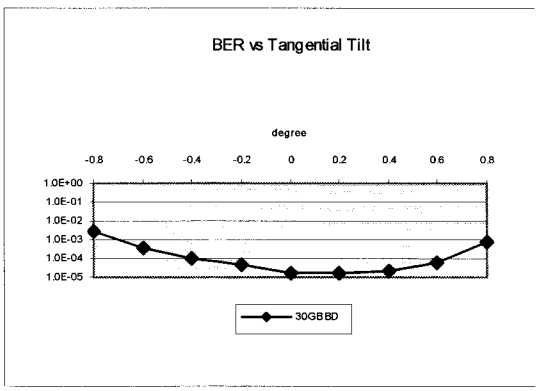


Fig. 10. Test board.



(a)



(b)

Fig. 11. BER vs. (a) radial tilt, and (b) tangential tilt on 30GB BD.

5. CONCLUSIONS

The architecture of 5-tap adaptive PRML for high-density optical disc is described. The components of the proposed PRML are presented and fully explained. The chip is fabricated in 0.18μm CMOS technology and mounted on the test board. The BER measurements are done with self-made 30GB BD at 1x speed. Test results show that the

proposed architecture has good performance on high-density optical disc.

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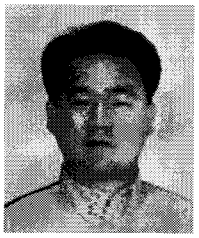

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