Effect of Channel Length in LDMOSFET on the Switching Characteristic of CMOS Inverter

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(Received November 8 2006, Accepted February 5 2007)

A two-dimensional TCAD MEDICI simulator was used to examine the voltage transfer characteristics, on-off switching properties and latch-up of a CMOS inverter as a function of the n-channel length and doping levels. The channel in a LDMOSFET encloses a junction-type source and is believed to be an important parameter for determining the circuit operation of a CMOS inverter. The digital logic levels of the output and input voltages were analyzed from the transfer curves and circuit operation. The high and low logic levels of the input voltage showed a strong dependency on the channel length, while the lateral substrate resistance from a latch-up path in the CMOS inverter was comparable to that of a typical CMOS inverter with a guard ring.

Keywords : LDMOSFET, CMOS inverter, Transfer characteristic, Latch-up

1. INTRODUCTION

The basic operation of a LDMOSFET(lateral double-diffused MOSFET) is similar to that of any MOSFET. However, the drain-source blocking voltage may be in the range of 100 volts, and the current driving capability of this device is usually high. The advantages of LDMOSFET are that it requires only a small input current[1,2]. Moreover, the high switching speed can be controlled with a very small gate current. Hence, LDMOSFET has found increasing applications in gate driver IC and high frequency converters.

The conventional CMOS inverter is the most popular digital logic circuit because of low power dissipation and high speed[3,4]. Currently, a typical CMOS inverter does not meet the needs for diverse power applications in a digital circuit. A new type of CMOS inverter for a wide power supply range and a large output voltage swing in a digital driver IC was suggested.

A LDMOSFET pair in CMOS inverter was examined for a high power application and high speed. Compared with a typical CMOS inverter, a LDMOSFET complementary inverter is believed to have good latch-up immunity and high voltage allowance due to the p/n junction-type source. The junction-type source in LDMOSFET can control the channel parameters to provide a high voltage swing in digital logic, and eliminate the need for a guard ring for latch-up immunity in a CMOS inverter, which is the most effective way of preventing latch-up.

The electrical characteristics of a LDMOSFET CMOS inverter were examined in terms of the voltage transfer characteristics, on-off switching properties and latch-up with a variation in the n-channel length and impurity concentration. Figure 1 shows a cross section of the CMOS inverter, where LDMOSFET has the typical structure consisting of a drift region and a main channel enclosing the source region. With the output node constrained to swing from ground to V_{DD}, the drain-to-body junctions in the n-channel device are always reversed –biased. A simulation is carried out using a TCAD MEDICI simulator. Table 1 shows the geometrical structure and doping levels.

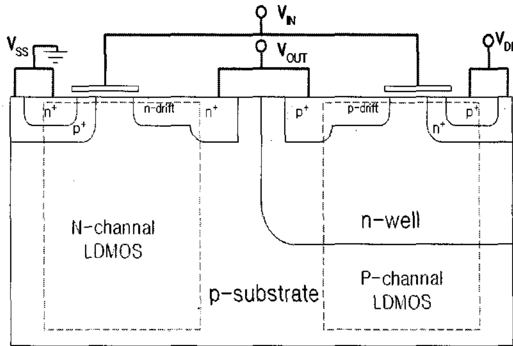

Fig. 1. Cross section of a CMOS inverter using LDMOSFET.

Table 1. Parameters of the geometric structure and doping levels.

Parameter name	value
n-channel length and doping level	0.5 μm, 5E17cm^{-3}
p-channel length and doping level	0.5 μm, 5E17cm^{-3}
n-drift length and doping level	5 μm, 2E16cm^{-3}
p-drift length and doping levels	5 μm, 6E16cm^{-3}
N and P LDMOS oxide thickness	150 Å

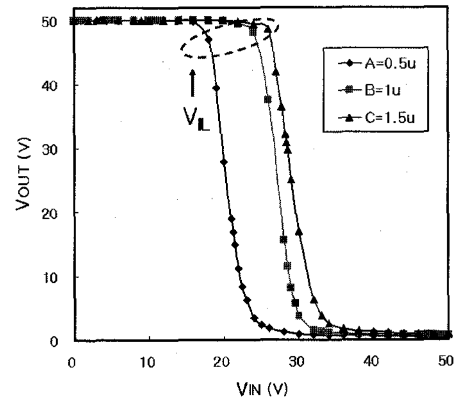

Fig. 2. Voltage transfer characteristic of a CMOS inverter as a function of the n-channel length.

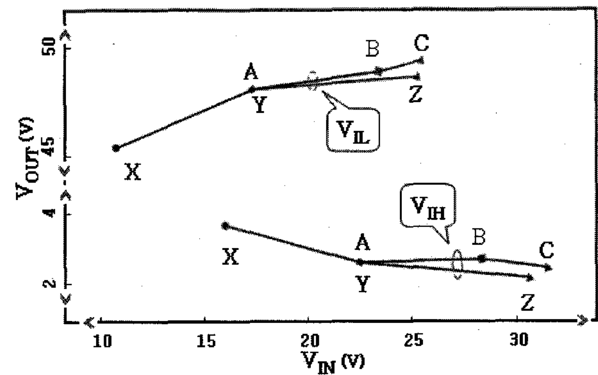

Fig. 3. High and low logic levels of the input voltage as a function of the n-channel length (A, B, C) and doping levels (X, Y, Z).

2. RESULT

Figure 2 shows the voltage transfer characteristic of a CMOS inverter, where A, B, and C correspond to the 3 different channel lengths of 0.5 μm, 1.0 μm, 1.5 μm, respectively.

The voltage transfer characteristics were obtained by varying the n-channel length at a doping level of 5E17 cm^{-3}. Each transfer characteristic has five distinct segments corresponding to the different modes of operation of the p and n-channel LDMOSFET. The first segment of the transfer characteristics was obtained when the p-LDMOSFET was in the triode region and the n-LDMOSFET was under saturation conditions, while the last segment is in an opposite operating region. The other segments were the interface regions and uncertainty region. The two cases of logic input voltages were considered: low input voltage V_{IL} when the input voltage, V_I, is at the logic-0 level; and the high input voltage, V_{IH}, when the input voltage, V_I, is at the logic-1 level. V_{IL} increased with increasing n-channel length. The result arises from the dependency of the threshold voltage and the conductance of the LDMOSFET on the channel length. The high and low digital output logic levels were almost in the output voltage where the input voltages V_{IL} and V_{IH} are located. The logic output voltages did not show as strong a dependency on the channel length as the input voltages of V_{IL} and V_{IH}.

Figure 3 shows the input logic levels, V_{IL} and V_{IH}, as a function of the channel length. Figure 3 also shows the effect of the n-channel doping levels, where X, Y and Z correspond to doping levels of 0.5E17 cm^{-3}, 1E17 cm^{-3} and 6E17 cm^{-3}, respectively at a channel length of 0.5 μm. The threshold voltage and channel conductance increased with increasing doping level. This alters the transfer characteristic resulting in an increase in V_{IL} and V_{IH}.

The effect of the n-channel length on the output logic levels can be observed in the equipotential lines at a gate

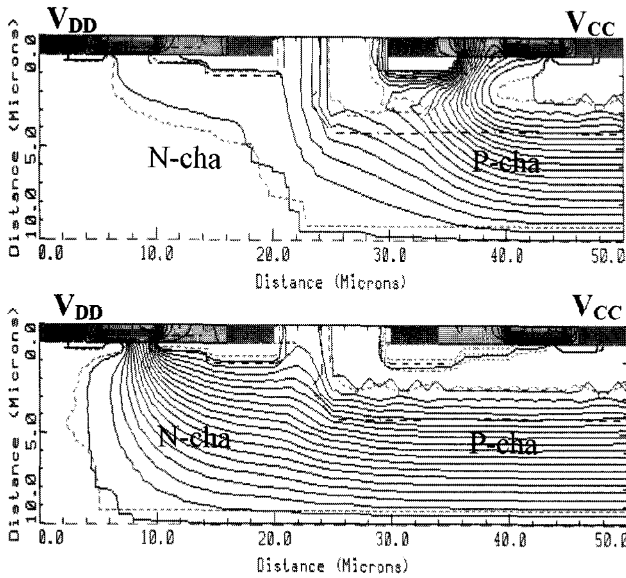

Fig. 4. (a) Cross-sectional view of the equipotential lines at a 0.5 ㎛ channel length with Vg=25 V.
(b) Cross-sectional view of the equipotential lines at a 1.5 ㎛ channel length with Vg=25 V.

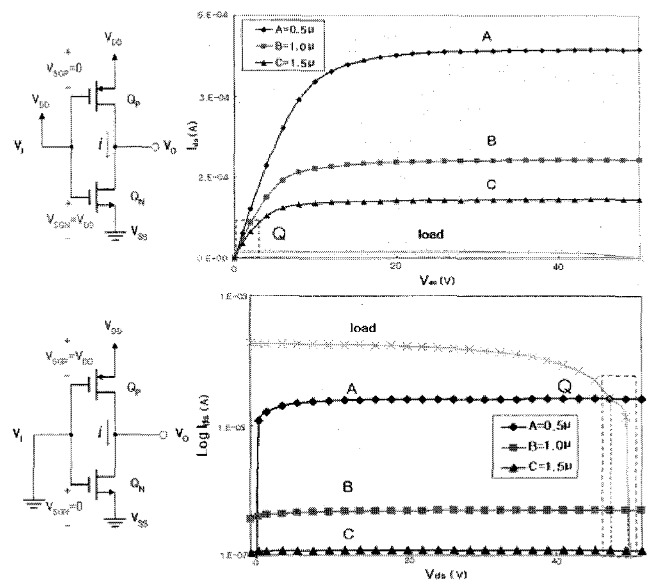

Fig. 5. (a) Operation of the CMOS inverter as a function of the channel length when the input voltage V_I is high.
(b) Operation of the CMOS inverter as a function of the channel length when the input voltage V_I is low.

voltage of approximately 25 V, as shown in Fig. 4. In Fig. 2, the low output voltage was obtained in the A channel length(0.5 μm) at an input voltage of 25 V, while, at the same input voltage, a high output voltage was observed in the B channel length(1.5 μm).

Figure 4(a), which has a 0.5 μm channel length, indicates that the p-channel LDMOSFET is in the higher potential compared with the n-channel one. The output current flows between the n-channel MOS and V_{SS}. Consequently, the output voltage is at the logic-0 level. On the other hand, the opposite case is shown in the second structure, which is in the B channel length and the output voltage is at the logic-1 level. In both cases, the edge of the drift region was in a high potential, and the junction type source was in a low potential region. This shows that even in the same voltage application, the channel length can alter the output logic level.

In Fig. 5, the n-channel LDMOSFET is considered to be the driving transistor, and the p-channel LDMOSFET is considered to be the load. Fig. 5(a) illustrates one case, when $V_I = V_{DD}$, showing the I_D-V_{DS} curve for the n-channel LDMOSFET Q_N.

When the input is high(V_{DD}), the n-channel device is turned on, the p-channel device is off. Hence, there is no dc path from V_{DD} to V_{SS}. The load curve is superimposed on the curves of the n-channel device. Since the p-channel device Q_P is turned off, the load curve will be at almost a zero current level. The current-voltage curves of the driver were obtained as a function of the n-channel length.

The operating point will be at the intersection of the two curves, where the output voltage is almost zero, and the output voltages are almost same regardless of the channel length. Fig. 5(b) shows the other extreme case, when $V_I = 0$ V. In this case, the n-channel LDMOSFET is in the off state. Therefore, its I_D-V_{DS} curve is almost a horizontal straight line at a zero current level. As shown, at the operating point where the driver curve meets load one, the output voltage is almost equal to V_{DD}. An analysis of Fig. 5 indicates that the n-channel length does not affect on the output logic levels of V_{OH} and V_{OL}.

The CMOS circuit is susceptible to latch-up due to of the presence of a pnpn structure. The four-layer structure of the n-well process arises from a p^+ source, n-well, a p substrate, and an n^+ drain. The layout technique and process change are effective ways of preventing latch-up. The CMOS inverter using LDMOSFET is considered to have a structure of latch-up immunity by reducing the substrate and well resistance.

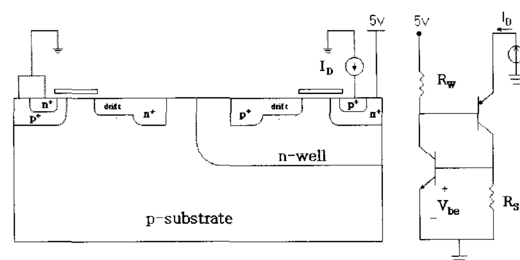

Fig. 6. Circuit of the latch-up path for the measurement of the substrate resistance, Rs.

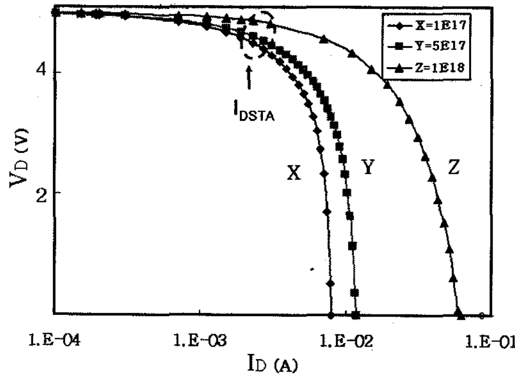

Fig. 7. I-V characteristics for the Rs measurement as a function of the n-channel doping levels.

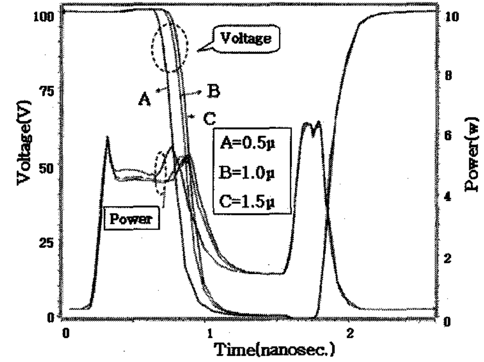

Fig. 9. Switching characteristics of the driver circuit as a function of the channel length.

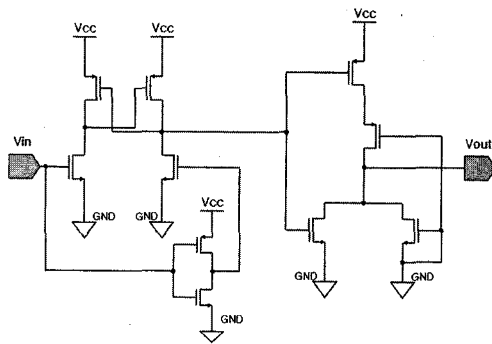

Fig. 8. LDMOSFET gate driver circuit for high power applications.

Figure 6 shows a cross-sectional view and circuit of the latch-up path for measuring the substrate resistance (Rs). The p/n junction-type source is considered to decrease the substrate resistance(Rs) and well resistance (Rw). With increasing current from the current source, which is connected to an emitter of a parasitic npn transistor, the emitter-base voltage(V_D) maintains a 5 V saturation state. At the moment of the turn-on state of the parasitic npn transistor, the voltage, V_D, decreases drastically. From this, the triggering current, Is, can be obtained. The substrate resistance, Rs, was measured from the triggering current, Is, and a saturation voltage of 0.6 V between the base and emitter in the pnp transistor. In Fig. 7, the substrate resistance(Rs), which was obtained when the voltage, V_D, decreases drastically, decreases with increasing channel doping. The measured substrate resistance(Rs) is in the 1 kΩ range, which is almost the same range in a typical CMOS inverter with a guard ring.

Figure 8 shows the output of the gate driver circuit, which consists of a level-shifter and CMOS inverters. The latch-up, output voltage swing, and device speed were tested in this circuit.

Figure 9 shows the output waveforms as a function of the channel length, whose frequency is 500 MHz. The figure shows a large voltage swing(100 V) with no latch-up and short delay times between the high and low logic outputs. It also shows that a faster output response is obtained with a shorter channel length, while the variation in the channel length has almost no affect on the high and low output voltages, power consumption, and delay times.

3. CONCLUSION

The electrical characteristics of a LDMOSFET CMOS inverter were investigated as a function of the n-channel length and impurity concentration. The transfer characteristics of the CMOS inverter and the on-off switching operation showed a strong dependency on the channel length. The digital logic levels of the input voltage increased with increasing n-channel length, while those of the output voltage showed no dependency. The junction-type source decreased the lateral substrate resistance resulting in good latch-up immunity.

ACKNOWLEDGEMENTS

This work was supported by the research grant of Chungbuk National University in 2006.

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