Alternative Optimization Techniques for Shallow Trench Isolation and Replacement Gate Technology Chemical Mechanical Planarization

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This paper discusses two approaches for pre-polishing optimization of oxide chemical mechanical planarization (CMP) that can be used as alternatives to the commonly applied dummy structure insertion in shallow trench isolation (STI) and replacement gate (RG) technologies: reverse nitride masking (RNM) and oxide etchback (OEB). Wafers have been produced using each optimization technique and CMP tests have been performed. Dishing, erosion and global planarity have been investigated with the help of conductive atomic force microscopy (C-AFM). The results demonstrate the effectiveness of both techniques which yield excellent planarity without dummy structure related performance degradation due to capacitive coupling.

Keywords : CMP, Etchback, Reverse masking, C-AFM

1. INTRODUCTION

Polish rates in chemical mechanical planarization (CMP) have inherent pattern density dependence. Regions on the surface where the ratio of high areas to low areas is bigger tend to be polished faster than regions with small ratios, resulting in non-planarity after the CMP step. The overpolishing in less dense regions results in dishing of low areas and stop-layer erosion of high areas[1] (Fig. 1). Dishing in turn leads to problems in consecutive process steps such as step coverage defects after reactive ion etching (RIE) or depth-of-focus related problems during lithography. Erosion causes performance degradation or even device failure.

In order to prevent the above mentioned problems, CMP optimization is required. Although different ways exist for improving the planarization step, such as optimization of the polish parameters or selecting better consumables (pad and slurry), the most efficient way is improving the design of the IC in order to provide more 'CMP-friendly' starting conditions.

The most common design optimization at present is the dummy insertion method[1] which, as the name implies, consists of introducing new, dummy structures in low areas. These dummies are not required for the IC functionality, but serve only as a means for equalizing pattern density across the surface. Many manufacturers choose this technique because it provides very good planarity results at no added cost, i.e. there is no additional increase in process complexity. However, dummy structures couple capacitively to the functional structures in the IC which has a negative effect on performance[2]. The magnitude of this effect is going to increase in the future as devices shrink in size and come closer to each other.

Therefore, considering ways towards attaining ultimate performance in microelectronic circuits, investigation of alternatives for CMP design optimization makes logical sense. In this work we analyze the advantages and disadvantages of two alternative optimization approaches, namely reverse nitride masking (RNM) and oxide etchback (OEB).

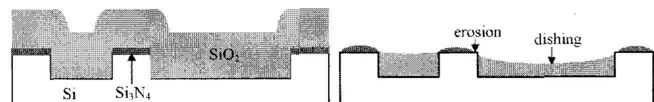

Fig. 1. Cross section of a wafer surface before (left) and after STI CMP (right).

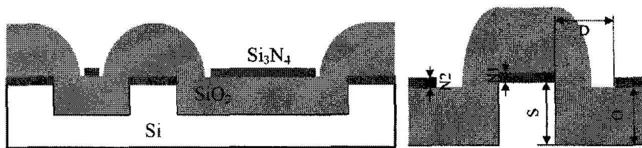

Fig. 2. Wafer surface with RNM optimization before CMP (left) and zoom-in (right) showing important process parameters: O – oxide thickness, D – spacing distance, S – trench depth in silicon, N1 – nitride stop-layer thickness and N2 – reverse nitride layer thickness.

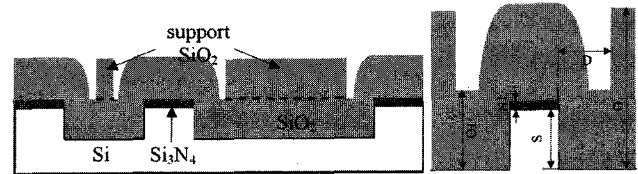

Fig. 3. Wafer surface with OEB optimization before CMP (left) and zoom-in (right) showing important process parameters: O – oxide thickness before etchback and after etchback in isolation areas, O1 – oxide thickness after etchback in exposed areas, D – spacing distance, S – trench depth in silicon and N1 – nitride stop-layer thickness.

2. OPTIMIZATION CONCEPT

Reverse nitride masking and oxide etchback are two optimization techniques in which, unlike dummy insertion, additional isolating material is structured in order to optimize polishing. In the case of RNM, this material is a second thin nitride layer and in the case of OEB, it is the deposited isolation oxide itself. Both techniques avoid performance degradation due to capacitive coupling at the expense of increased process complexity by introducing additional lithography and etching steps.

STI CMP is chosen as the planarization step where the optimization techniques are to be tested. However, as explained later, the results are fully applicable to replacement gate CMP. The optimization principles are also valid for back-end planarization.

2.1 Reverse nitride masking

The goal of RNM is to effectively control overpolishing in low pattern density regions by providing an additional stop-layer in low areas as illustrated in Fig. 2. The structuring of the nitride layer is performed using an additional mask. The mask is characterized by a specific spacing between the structures on it and on the original STI mask. This spacing determines how close to the active areas the surface is protected from overpolishing. Smaller spacing is expected to give better results but also requires more precise alignment.

2.2 Oxide etchback

Unlike RNM, the goal of oxide etchback is to equalize pattern density by preliminary oxide etching over high areas. In this case the result is maximizing pattern density throughout the wafer (Fig. 3). The same mask produced for RNM is also used for OEB. The different spacing in this case determines to what extend pattern density variations are minimized after etchback. Again, smaller spacing gives better results, but requires better alignment.

3. DEVICE FABRICATION

Initially, the new reverse masks needed for the second photolithography step are designed and produced. Masks with three different spacing distances are manufactured: 1, 2 and 3 μm.

Tests are performed on 4" pSi(100) wafers. A 100 nm silicon nitride layer is deposited on all wafers by atmospheric pressure chemical vapor deposition (APCVD). STI photolithography, CHF_3-O_2 RIE of the nitride and $SiCl_4$ RIE of the silicon bulk define trenches with a depth of approximately 300 nm below the silicon surface i.e. 400 nm below the top nitride surface. The batch is then split in two for testing the two optimization techniques.

The first sub-batch is optimized with RNM. A 300 nm thick plasma-enhanced chemical vapor deposition (PECVD) oxide is deposited (equal to the silicon trench depth), followed by a second APCVD nitride deposition (100 nm). A second photolithography is performed next using the reverse masks. Finally, the second nitride layer is structured by another RIE step.

The second sub-batch receives OEB optimization. A PECVD oxide of around 1 μm is deposited (in this case the oxide must be thicker than twice the total trench depth including the nitride thickness). Photolithography with the reverse masks follows and an oxide RIE of 400 nm (equal to the total trench depth) completes the process, ensuring equal height in isolation and active areas.

After manufacturing is complete, CMP is carried out. Planarization is performed on a Strasbough 6EC polish machine equipped with Universal Photonics ESM-U polish pads and using a high-selectivity STI slurry from H.C. Starck. CMP is carried out in several steps per wafer with atomic force microscopy (AFM) control in-between the steps in order to observe the progress of the planarization process. For both optimization techniques

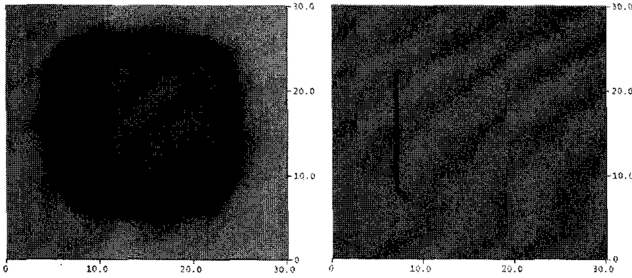

Fig. 4. Topographic (left) and corresponding electrical (right) C-AFM scan of an area on a wafer with RNM optimization after CMP, indicating nitride erosion at the left edge of the active area due to mask misalignment.

CMP continues until the first nitride stop-layer is reached everywhere on the wafers as shown by the AFM measurements.

Following CMP, wafers are cleaned in a Corwet P200 cleaner, using brush and megasonic cleaning with water, ammonium hydroxide (NH_4OH) and hydrochloric acid (HCl).

4. RESULTS AND DISCUSSION

To evaluate the planarization results conductive atomic force microscopy (C-AFM) is used. As previously demonstrated[3], C-AFM provides an accurate way of detecting nitride erosion with nanometer resolution, even in case of very smooth transitions between various materials where conventional topographic AFM fails to detect erosion. This is because of the additional electrical information which is supplied simultaneously and independently from the topographic information.

4.1 Reverse nitride masking

Global planarity measured after nitride removal is below 100 nm across the 4" wafers. Dishing is eliminated completely in large isolation areas because of the nitride layer protection and is only present within the spacing between the structures on the two masks. Concerning nitride erosion, it is absent for spacing of 1 μm. With 2 μm spacing, there is erosion in certain areas due to misalignment of the masks (Fig. 4). This is because misalignment causes different actual spacing in different positions on the wafer and within one structure itself. This misalignment is beneficial for the tests because it allows determining the precise critical distance at which erosion first appears. As shown in Fig. 5, for the parameters chosen in the test process, erosion occurs at spacing distances above 2.7 μm. It should be noted that erosion also depends on the vertical difference between the two nitride levels. The higher the second nitride level is, the smaller the erosion is (at the expense of some additional topography).

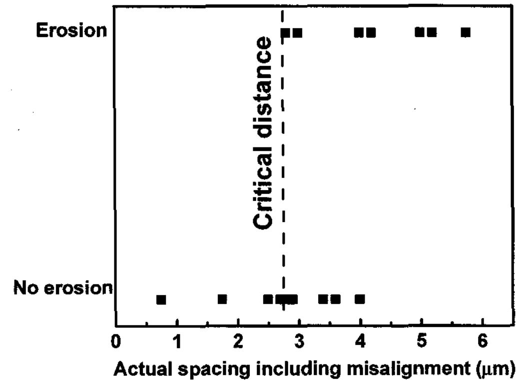

Fig. 5. Dependence of actual spacing distance between the masks (including misalignment) on erosion.

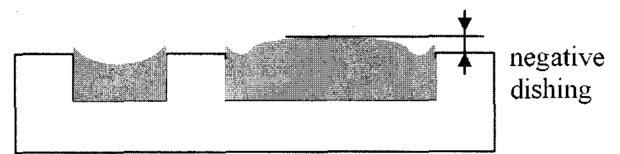

Fig. 6. Wafer surface with OEB optimization after CMP and nitride removal illustrating negative dishing in large isolation areas.

4.2 Oxide etchback

Planarity after nitride removal is below 100 nm across the wafers. Dishing is strongly reduced. Actually, for very large isolation areas where there is negative dishing, i.e. the area is slightly elevated above active area level (Fig. 6). As for erosion, OEB optimized wafers are found to be less sensitive to spacing. Erosion is fully eliminated for all tested spacing distances, even with the additional misalignment. This positive result can be explained with the fact that, as AFM measurements in-between polishing steps indicate, planarity is reached before reaching end-point of polishing. This leads to a much shorter overpolishing time needed and therefore there is no excessive thinning of the stop-layer.

An AFM scan over a transistor area on a wafer with OEB optimization after polishing is shown on Fig. 7.

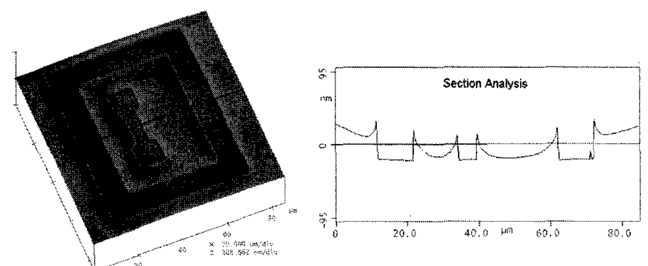

Fig. 7. Topographic AFM scan of a transistor area on a wafer with OEB optimization after CMP and nitride removal (left) and a cross section along the black line (right).

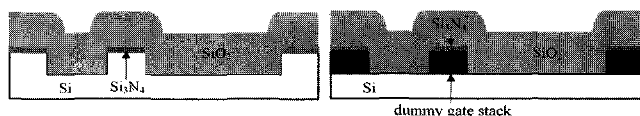

Fig. 8. Schematic showing analogy between wafer top structure for STI (left) and replacement gate technology (right) processing prior to CMP.

4.3 Discussion

Global planarity obtained with both optimization techniques is below or close to 100 nm. There is no doubt that by using more advanced equipment even better results can be obtained. The limiting factors for planarity in the case of RNM are stop layer thickness and spacing. Using spacing below 1 μm in combination with a thinner nitride layer will presumably bring planarity below 50 nm. In case of OEB, planarity can be improved further by reducing nitride thickness, lowering spacing and possibly using tiled support oxide structuring which will yield further reduction in pattern density distribution. For both optimization techniques, another useful addition would be the application of flexible spacing in order to change spacing within a wafer depending on pattern density. Using lower spacing in less dense regions can compensate for the higher polish rates there. Planarity in the presented tests is also limited due to non-uniformities in the deposited oxide and nitride layers, depth variations in the etched trenches and other technical difficulties coming from using university research level equipment.

Regarding possible applications of RNM and OEB, as described above, tests have been performed on the STI level. However, comparing the wafer surface before STI CMP and the oxide CMP in replacement gate technology (Fig. 8), it is straightforward to see that the two planarization processes are identical and RNM and OEB can be implemented for RG without major changes. Reverse masking or etchback techniques can also be used as optimization for the second CMP step in RG – the patterning of the real gate. In this case the metal itself can be etched back or oxide/nitride layers can be used as stop-layers depending on polish chemistry. The principle of pre-structuring of the to-be-polished material (OEB) or an additional layer (RNM) also holds true for all other planarization steps in IC manufacturing.

5. CONCLUSION

We have demonstrated the functionality of two techniques for CMP planarity optimization: oxide etchback and reverse nitride masking. These techniques are applicable in various CMP processes: STI, replacement gate technology, etc. Their major advantage to the commonly used dummy tile insertion is the absence of additional parasitic capacitances in the circuit and their major disadvantage is the increased process complexity. A planarity of around 100 nm is reached for both techniques using university level equipment and fixed geometries. It is clear that state of the art equipment and adaptive geometries can give significantly better results. We conclude that both optimization techniques are good candidates for replacing dummy tile insertion in applications where maximum performance is required.

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