Phase Locked Loop Sub-Circuits for 24 GHz Signal Generation in 0.5 μm SiGe HBT technology

Wooyeol Choi and Youngwoo Kwon

***Abstract*—In this paper, sub-circuits for 24 GHz phase locked loops(PLLs) using 0.5 μm SiGe HBT are presented. They are 24 Ghz voltage controlled oscillator(VCO), 24 GHz to 12 GHz regenerative frequency divider(RFD) and 12 GHz to 1.5 GHz static frequency divider. 0.5 μm SiGe HBT technology, which offers transistors with 90 GHz fMAX and 3 aluminum metal layers, is employed. The 24 GHz VCO employed series feedback topology for high frequency operation and showed -1.8 to -3.8 dBm output power within tuning range from 23.2 GHz to 26 GHz. The 24 GHz to 12 GHz RFD, based on Gilbert cell mixer, showed 1.2 GHz bandwidth around 24 GHz under 2 dBm input and consumes 44 mA from 3 V power supply including I/O buffers for measurement. ECL based static divider operated up to 12.5 GHz while generating divide by 8 output frequency. The static divider drains 22 mA from 3 V power supply.**

***Index Terms*—24 GHz, Frequency Divider, MMIC, PLL, SiGe HBT and VCO**

I. INTRODUCTION

As one of ISM bands, 24 GHz has versatile application including short range automotive radar. One of the most important building blocks of automotive radar systems is signal generator. Especially for frequency modulated continuous wave(FMCW) radar, performance of signal generator limits performance of overall system. Although voltage controlled oscillator(VCO) in conjunction with look-up table is classical method for FMCW signal generation, a phase locked loop(PLL) has some unique advantage over VCO method.[1] PLLs can generate more stable and linear chirp even in wide range of variation and have more controllability which enables programmable and multi-usable signal source. One major drawback of PLL is its complexity since it requires several analog and digital circuit blocks such as VCO, frequency dividers, phase detector, low pass filter and control circuits. However, recent advances in integrated circuit technology allow complex integration with a small size and low power consumption.

SiGe HBT shows higher speed in terms of cutoff frequency(f_T) and maximum oscillation frequency(f_{MAX}) compare to CMOS in same technology generation. Moreover, for some advantages such as higher current density and better low frequency noise, SiGe HBT is suitable for high frequency applications.[2-5] Furthermore, integration with CMOS as BiCMOS enables complicated analog digital mixed circuits. One can employ SiGe HBTs for high frequency block and CMOS for low frequency and control block. [4, 5]

Fig. 1 shows typical block diagram of 24 GHz PLL sub-system. 24 GHz VCO and following frequency dividers have operating frequency over 1.5 GHz. Typically, the frequency divider chain is composed of an analog frequency divider which handles the highest frequency and following series of static dividers which is implemented by using high speed logic circuit such as emitter coupled logic (ECL).

In this work, high frequency blocks of 24 GHz PLL

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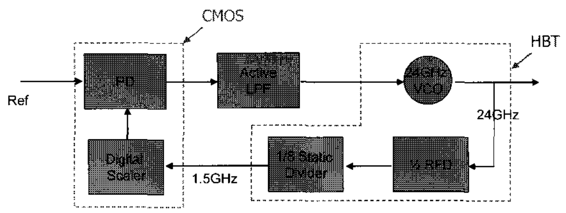


Fig. 1. Block diagram of typical 24 GHz PLL sub-system.

sub-system are developed in commercially available low cost 0.5μm SiGe HBT technology. Those circuits are 24 GHz VCO, 24 GHz to 12 GHz analog frequency divider and static frequency divider up to 12 GHz.

II. CIRCUIT DESIGN & MEASUREMENT

The 0.5 μm SiGe HBT technology used in this work has selectively implanted collector(SIC) and non-SIC version of HBT which has 50 GHz and 80 GHz cutoff frequency and 90 GHz maximum oscillation frequency. High quality passive devices such as poly resistors, inductors using thick aluminum and metal-insulator-metal capacitors are offered as well. Some technology parameters found in [6] are summarized in table I.

Table 1. Technology parameters of 0.5μm SiGe HBT process.

Devices	SiGe2-RF	
	Non-SIC	SIC
Minimum emitter width [μm]	0.5	
Base sheet resistance [Ohm]	2000	
Current gain	250	
VCB0 [V]	11.0	9.5
VCE0 [V]	4.3	2.4
FT [GHz]	50	80
Fmax [GHz]	90	90
Metal layers	3	

2.1 24 GHz Voltage Controlled Oscillator

The VCO employed series feedback topology. A variable capacitor formed by using varactor diode(D1) makes main transistor(Q1) unstable and steers the oscillation frequency. Base terminal of main transistor(Q1) is terminated by finite effective inductor to cancel out parasitic capacitance. The effective inductor is formed by using shorted transmission line. Series feedback topology has higher operating frequency compare to conventional cross coupled one common in low frequency VCO design and it does not requires high input impedance buffer amplifier which is not available at high frequencies. Therefore, common emitter buffer which has low input impedance can be used. The schematic of the VCO is shown in Fig. 2.

The fabricated VCO are shown in Fig. 3. Overall size of the chip is 900x450 μm^2 including probing pads. From the measurement, it is found that the output frequency can be tuned from 23.2 GHz to 26 GHz with output power from -3.8 dBm to -1.8 dBm. Phase noise of

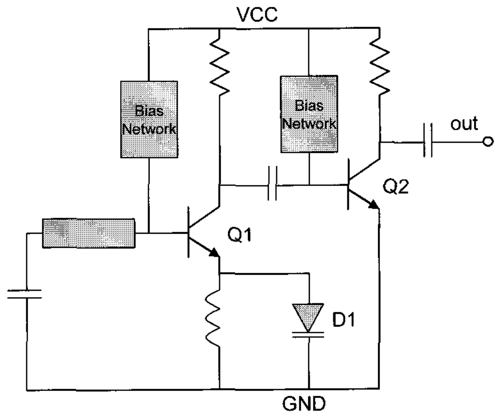


Fig. 2. Schematic of 24 GHz VCO.

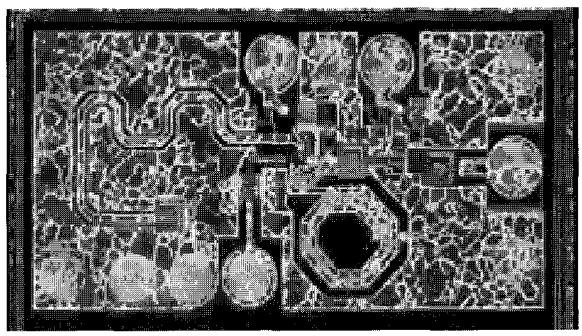


Fig. 3. Photograph of 24 GHz VCO.

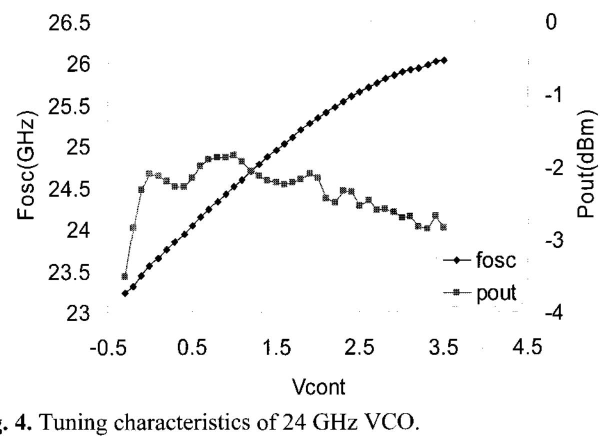


Fig. 4. Tuning characteristics of 24 GHz VCO.

The VCO is measured to be about 80 dBc/Hz at 1 MHz offset. Relatively poor phase noise is from base and collector bias network composed of resistors and diode connected transistors.

2.2 24 GHz to 12 GHz regenerative frequency divider

The frequency divider following VCO takes input of 24 GHz and generates 12 GHz output. Since the operating frequency is high for the given f_T of the HBT(80 GHz), the frequency divider employed regenerative topology introduced in [7]. A regenerative frequency divider(RFD) is based on a mixer having a self feedback from IF output to RF input. RFD has high operation frequency but suffer from small bandwidth compare to static frequency dividers which work from near DC to about a fifth of cutoff frequency. Therefore, RFD is preferable for the frequency divider after VCO. A Gilbert cell mixer with output buffer is designed and two IF outputs of the mixer are fed back to the RF inputs of the mixer itself. Typically one inverting amplifier is placed in the feedback path to satisfy the in-phase condition at RF input port. However, at high frequency,

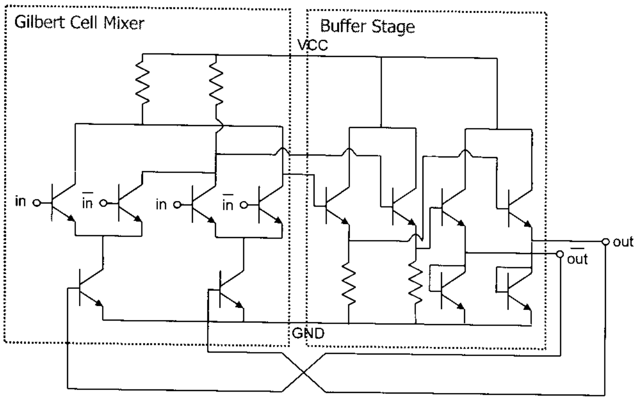


Fig. 5. Schematic of 24 GHz to 12 GHz RFD.

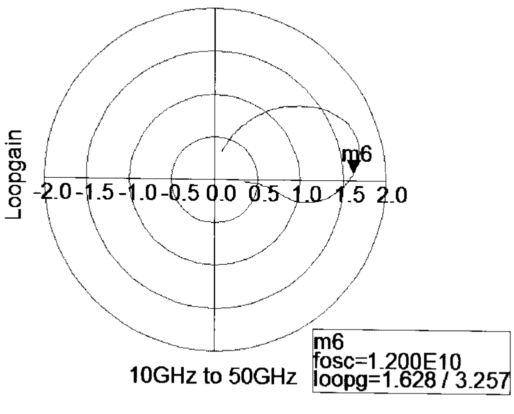


Fig. 6. Simulated loopgain of RFD.

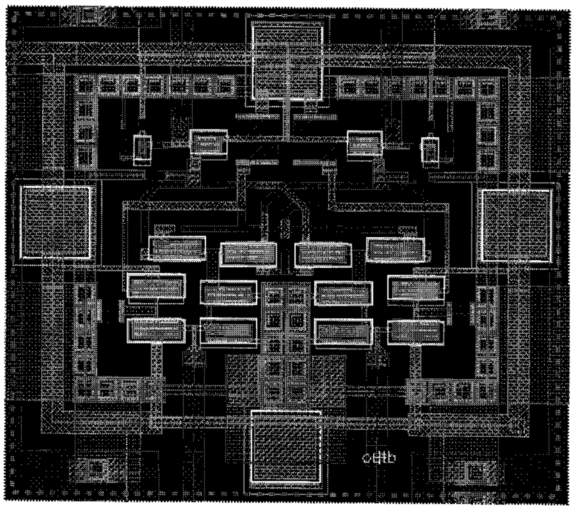
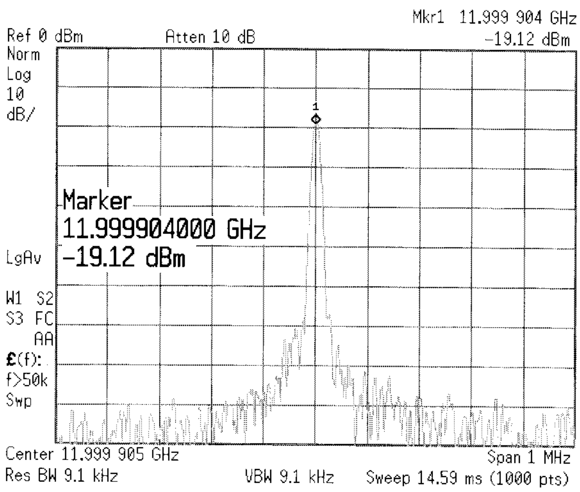
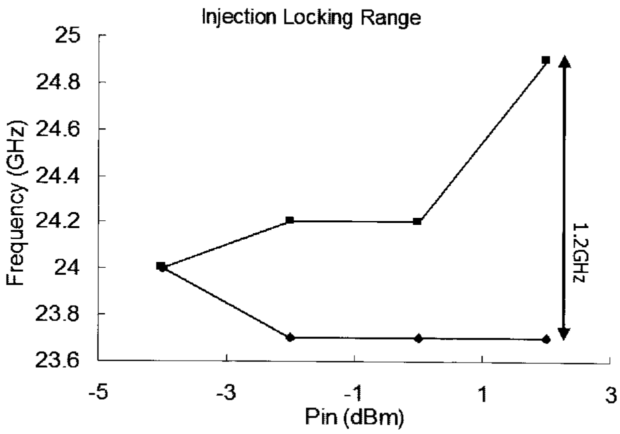


Fig. 7. Layout of RFD.



(a)



(b)

Fig. 8. (a) Output spectrum and (b) Injection locking characteristic of RFD.

the mixer and amplifier has phaseshift less than 180 degree due to parasitic between collector and base. Besides, the interconnections between mixer and amplifer sets finite amount of phaseshift which, in turns, make hard to get exact phaseshift needed. Thus, in this work the in-phase condition is established by cross connecting the differential output to RF input as shown in Fig. 5. Simulated loopgain, shown in Fig. 6, have magnitude slightly larger than 1 and exact 360 degree phaseshift at half of 24 GHz input.

From the measurement, it is found that the frequency divider has 1.2 GHz(5%) bandwidth around 24 GHz input when the input power is 2 dBm. The measurement results are shown in Fig. 8. The current consumption is measured to be 44 mA under 3 V bias condition including input and output buffer amplifier for measurement purpose. Size of RFD core is 220 x 170 μm^2 (Fig. 7).

2.3 12 GHz to 1.5 GHz Static Frequency Divider

The frequency divider following RFD is static divider which has dividing ratio of 8. The divider is implemented by cascading 3 ECL latch, implemented as shown in Fig. 9(b), based divide by 2 circuits(Fig. 9(a)). ECL logic is capable of high speed operation thank to its high beta and switching speed. The layout of the divider is shown in Fig. 10. The core of the divider occupies area of 450µm x 200µm. The fabricated static frequency divider is operated up to 12.5 GHz in on-wafer measurement. Simulated waveform and measured output spectrum are shown in Fig. 11 and 12 respectively. The divide-by-8 circuit consumes 22mA from 3V power supply. The power consumption is relatively higher than CMOS based logic. Therefore, one should determine the dividing ratio of HBT ECL logic divider down to upper speed limit of available CMOS logic.

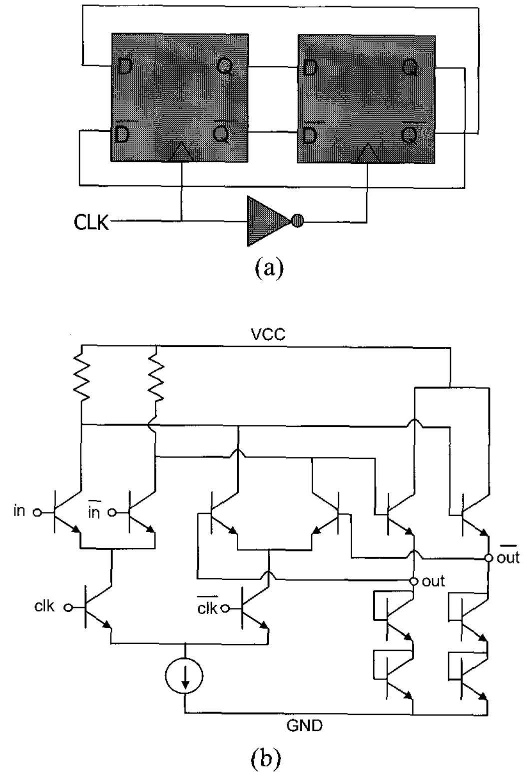


Fig. 9. (a) Block diagram of static divider based on latch and (b) Schematic of the latches.

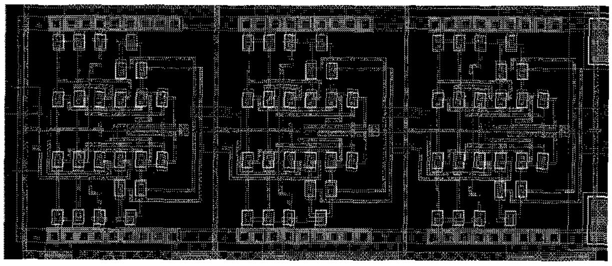


Fig. 10. Layout of static divider.

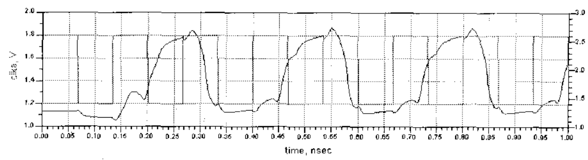


Fig. 11. Simulated output waveform of divide-by-2 circuit.

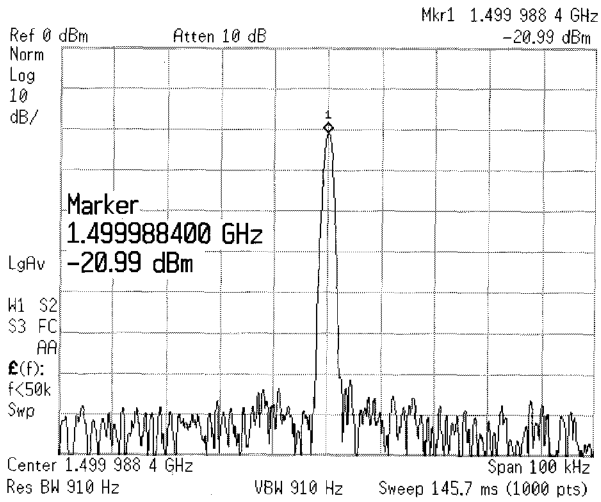


Fig. 12. Measured output spectrum of static frequency divider.

III. CONCLUSIONS

Circuit blocks for 24 GHz PLL are developed by using commercially available low cost 0.5 μm SiGe HBT technology. They are 24 GHz VCO, 24 GHz to 12 GHz regenerative frequency divider and 12 GHz to 1.5 GHz static frequency divider. The measurement results showed successful demonstration of designed circuits. These circuit blocks can be used to form 24 GHz PLL for various application including short range automotive radar systems. Further integration in scaled down HBT or BiCMOS processes can realize smaller size and lower power PLLs.

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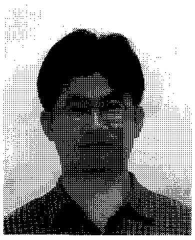

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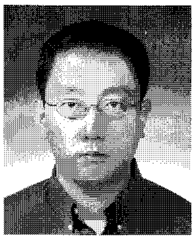

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amplifier design company, which is now fully owned by Avago Technologies. He holds more than 20 patents on RF MEMS and power amplifier technology. He was the recipient of Presidential Young Investigator award from Korean government in 2006.