Efficiency Improvement of HBT Class E Power Amplifier by Tuning-out Input Capacitance

Ki Young Kim, Ji Hoon Kim, and Chul Soon Park

Abstract—**This paper demonstrates an efficiency improvement of the class E power amplifier (PA) by tuning-out the input capacitance (C_{IN}) of the power HBT with a shunt inductance. In order to obtain high output power, the PA needs the large emitter size of a transistor. The larger the emitter size, the higher the parasitic capacitance. The parasitic C_{IN} affects the distortion of the voltage signal at the base node and changes the duty cycle to decrease the PA's efficiency. Adopting the L-C resonance, we obtain a remarkable efficiency improvement of as much as 7%. This PA exhibits output power of 29 dBm and collector efficiency of 71 % at 1.9 GHz.**

Index Terms—**Class E, hetero-junction bipolar transistor, monolithic microwave integrated circuit, power amplifier**

I. INTRODUCTION

The class E PA which was firstly introduced [1] for constant envelope signal amplification has garnered much more attention for the power efficient transmission of non-constant envelope mobile communications such as CDMA employing EER and polar transmitter [2]. Adopting the class E PA, we can obtain much higher efficiency than that of the linear PA which has a smart function of the bias control circuit [3,4]. The HBT class E PAs operating at mobile communication frequency were researched with output power of 21~27 dBm [5-7] and the PAs have emitter size of 896 μm^2 for 21 dBm and 1620 μm^2 for 24 dBm. For 1 W output power we should use emitter size of 3000~4000 μm^2 [8] which has maximum input parasitic capacitance of 30~40 pF which is a simulated value at 1.9 GHz frequency. When we enlarge the transistor's emit size to increase output power, the input parasitic capacitance grows proportional to the emit size. However, the output power increment is not effective in comparison with the increase of input parasitic capacitance. The large input capacitance will reduce and distort the input signal applied to the amplifier which degrades the collector efficiency of the amplifier. Since the equation of class E operation assumes that the input signal has a sinusoidal wave, it is difficult to explain the effect of non-ideal input signal with the input capacitance (C_{IN}). Our previous work proposed a solution to cancel out input capacitance for efficiency improvement [9], and this paper will analyze the new class E operation with the effect of the increased input capacitance (C_{IN}) for the high output power level.

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II. PARASITIC CAPACITANCE ANALYSIS OF CLASS E HBT POWER AMPLIFIER

A conventional HBT class E PA is shown in Fig. 1. The C_{BE} and C_{CE} mean the base-emitter and collector-emitter parasitic capacitance, respectively. The C_{added} means the additional chip capacitance. The output circuit is composed of a switch capacitor (C_{CE} + C_{added}), an LC filter and a transformer. Conventionally, it is assumed that an input signal is an ideally sinusoidal wave. But with increasing C_{BE}, the voltage signal at the base node

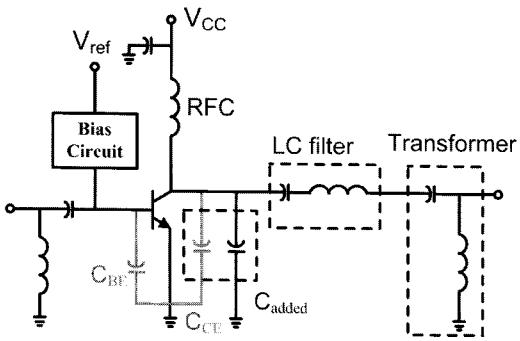


Fig. 1. Conventional HBT class E PA with parasitic capacitance.

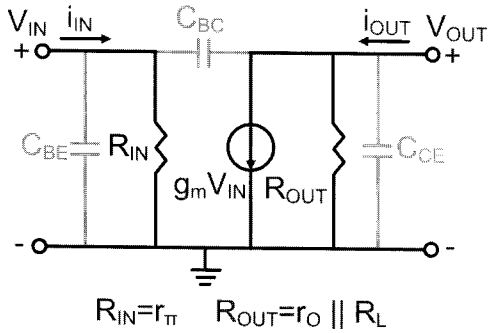


Fig. 2. HBT equivalent circuit with parasitic capacitance.

will be distorted according to the charge and discharge effect from C_{BE}. The distortion will affect the switching duty cycle and degrade the PA's efficiency.

Fig. 2 shows the HBT equivalent circuit with parasitic capacitance for the class E power amplifier. In order to simplify the analysis of C_{BE} effect, we use the small-signal equivalent circuit. The value of C_{BE} depends on the emitter size of the HBT main transistors. The input resistance (R_{IN}) is the base-emitter resistance, which is around 10 Ω at the emitter size for 1W when the switch is on. The collector-emitter capacitance (C_{CE}) will be counted as a component of shunt switch capacitance. Using the y-parameter, we can obtain the values of parasitic C_{BE} and C_{CE}.

$$Y_{11}=\frac{i_{IN}}{V_{IN}}\left(atV_{OUT}=0\right)=\frac{i_{IN}}{i_{IN}\left\{r_{\pi}\,\|\,\frac{1}{j\omega\left(C_{BE}+C_{BC}\right)}\right\}} \tag{1}$$

$$Y_{22}=\frac{i_{OUT}}{V_{OUT}}\left(atV_{IN}=0\right)=\frac{i_{OUT}}{i_{OUT}\left\{\left(r_{O}\,\|\,R_{L}\right)\|\,\frac{1}{j\omega\left(C_{CE}+C_{BC}\right)}\right\}} \tag{2}$$

$$Y_{12}=\frac{i_{IN}}{V_{OUT}}\left(atV_{IN}=0\right)=\frac{i_{IN}}{i_{IN}\left(\frac{1}{j\omega C_{BC}}\right)}=j\omega C_{BC} \tag{3}$$

$$C_{BE}=\frac{imag\left(Y_{11}+Y_{12}\right)}{\omega} \tag{4}$$

$$C_{CE}=\frac{imag(Y_{22}+Y_{12})}{\omega} \tag{5}$$

As shown in Equation (4-5), C_{BE} and C_{CE} can be expressed in imaginary values of y-parameter. C_{CE} and C_{added} can be used without any compensation and we can focus on only the C_{BE} effect. We simulated the value of each parasitic capacitance and the relation between maximum output power and efficiency for the conventional class E PA according to the variable HBT emitter sizes at 1.9 GHz as shown in Fig.3. Even though the large emitter size can give high power capability, the collector efficiency decreases significantly because of the input signal distortion according to the high C_{BE} value.

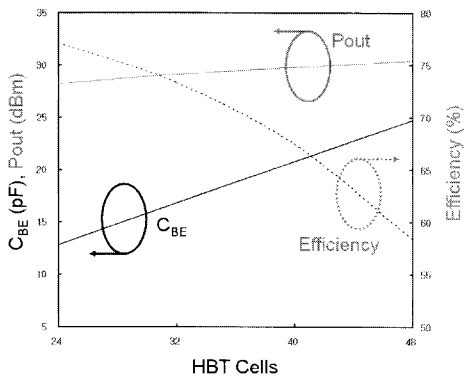


Fig. 3. Simulated C_{BE}, Pout and efficiency for different number of HBT cells.

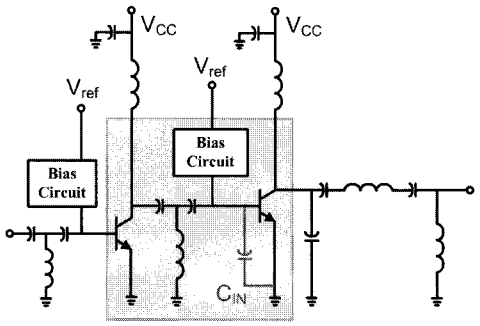
III. Input Signal Analysis of Class E HBT Power Amplifier

In the previous paragraph, we discussed the efficiency decrease according to the average C_{BE} increase. Now, we will discuss the time domain analysis for the relation between input voltage signal (V_{IN}) at the base node and input parasitic capacitance (C_{IN}) at the base node and discuss their effects on ideal class E operation. Fig. 4(a)

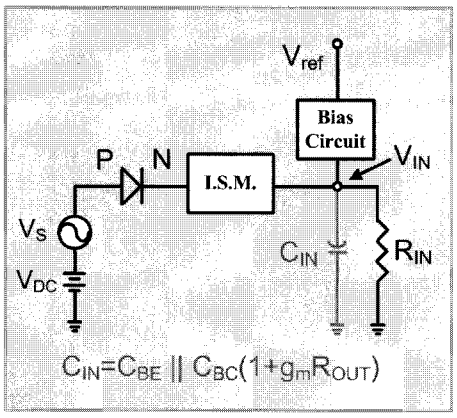
shows the conventional two-stage class E PA and the shadow box in Fig. 4(a) can be represented equivalently with Fig. 4(b). The base-collector of the drive-stage HBT can be represented with PN diode. R_{IN} means the input resistance (r_π) of the power-stage HBT and C_{IN} means the input capacitance which is combined with C_{BE} and $C_{BC}(1+g_mR_{OUT})$. The value of C_{BC} is about a tenth of the C_{BE} value and g_mR_{OUT} is smaller than 0.5. Therefore the C_{BE} can be a dominant part of C_{IN}. The impedance of the bias circuit and inter-stage matching circuit can be assumed as open and short, respectively, at the fundamental frequency. Finally, the circuit in Fig. 4(b) can be operated as a peak rectifier circuit. The V_{IN} keeps sinusoidal wave at zero value of C_{IN}. However, for the increased C_{IN} cases, the V_{IN} will be distorted by alternating charge and discharge from C_{IN}.

Fig. 5(a) shows the time domain analysis of the ideal sinusoidal V_{IN} for 32 HBT cells. C_{IN} and R_{IN} will be changed with the values of V_{IN}. In order to simplify the analysis, we assume that both C_{IN} and R_{IN} have two different values: on-state and off-state according to the V_{IN} values. Fig. 5(b) shows the time domain analysis of the C_{IN} and R_{IN} which are calculated with the on-state when V_{IN} has a maximum value and the off-state when V_{IN} has a minimum value.

As shown in Fig. 5(b), C_{IN} has a maximum value of 31.1 pF and R_{IN} has a minimum value of 10 Ω at the on-state. The discharge of C_{IN} which starts at the point of V_{IN}=MAX will distort the waveform of V_{IN} as shown in Fig. 6. This distortion by discharge of C_{IN} will change the duty cycle (D) which is the ratio of on/off-state and ideally have 0.5. Finally, the duty cycle grows proportional to the input parasitic capacitance. If the on-state will be changed to the off-state at the point V_{IN}=MID, we will assume that the time at V_{IN}=MID is t.

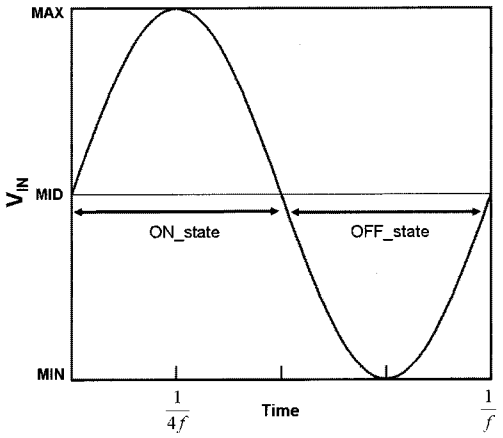


(a)

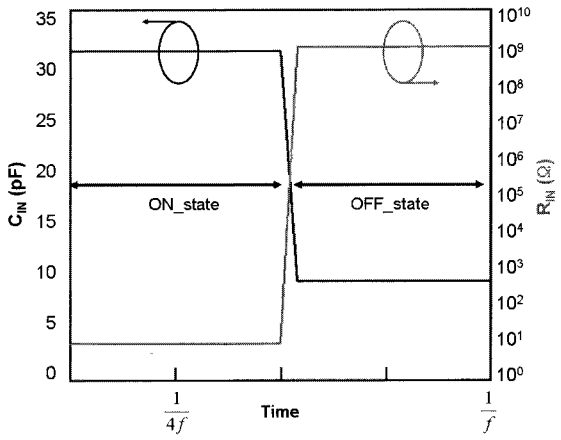


(b)

Fig. 4. Two-stage class E power amplifier: (a) Basic circuit. (b) Equivalent circuit.



(a)



(b)

Fig. 5. Time domain analysis for 32 HBT cells: (a) ideal V_{IN}. (b) C_{IN} and R_{IN}.

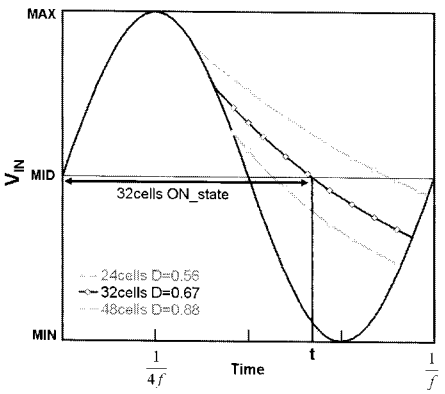


Fig. 6. Time domain analysis of real VIN for different number of HBT cells.

According to below equations, we will define the relation between the duty cycle (D) and input parasitic capacitance (C_{IN}).

$$V_{IN} = V_{MAX} \exp\left[-\frac{\left(t-\frac{1}{4f}\right)}{R_{IN}C_{IN}}\right] = \frac{1}{2}V_{MAX} \tag{6}$$

$$\frac{\left(t-\frac{1}{4f}\right)}{R_{IN}C_{IN}} = \ln 2 \tag{7}$$

$$t = \ln 2 \cdot R_{IN}C_{IN} + \frac{1}{4f} \tag{8}$$

The period of on-state for class E operation is 2πD and the period of on-state and off-state is 2π. The relation between t and duty cycle (D) can be represented with (9) and the duty cycle (D) can be derived with a function of C_{IN} in (10).

$$t : \frac{1}{f} = 2\pi D : 2\pi \tag{9}$$

$$D = 0.25 + \ln 2 \cdot R_{IN}C_{IN}f \tag{10}$$

The simulated values of maximum C_{IN} when the switch is on are 23.4/31.1/46.7 pF and the duty cycle (D) are 0.56/0.67/0.88 for 24/32/48 cells as shown in Fig. 6. In conclusion, the larger the emitter size of HBT, the higher the parasitic capacitance (C_{IN}). Therefore, the duty cycle (D) increases to higher than 0.5 and the efficiency decreases as shown in Fig. 7. In the next chapter, we will discuss the efficiency improvement

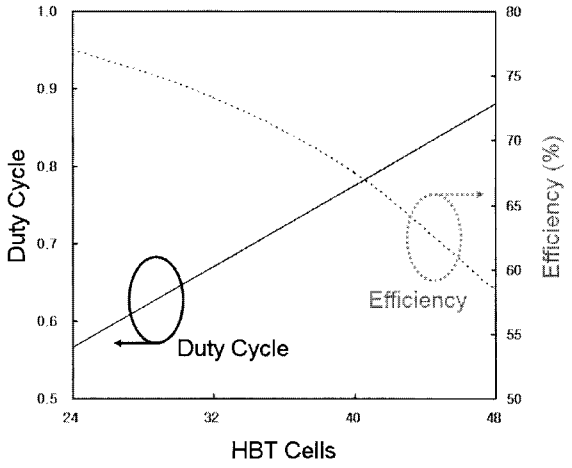


Fig. 7. Duty cycle and simulated efficiency for different number of HBT cells.

technique with the C_{BE} compensation circuit which is composed of an LC resonator.

IV. Proposed CBE Compensation Circuit for High Efficiency and High Power Class E Amplifier

The proposed class E power amplifier compensating the input capacitance (C_{IN}) is shown in Fig. 8. In order to satisfy the high power capability and the high efficiency at the same time, it is necessary to eliminate the effect of C_{IN}. The HBT emitter size is 2560 μm^2 (32 cells) for output power of 29 dBm. In order to cancel out C_{IN}, an inductor L_{added} has been added for L-C resonance at the 1.9 GHz operation frequency.

With adding an LC resonance circuit, the impedance of Z_{LC} will be very high as shown in Fig. 9. Therefore, the distortion effect will be remedied and the input voltage V_{IN} will be compensated with an ideal sinusoidal

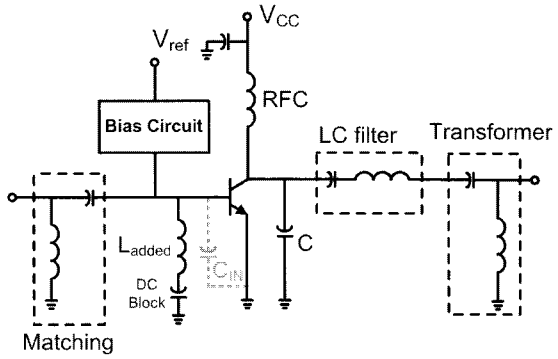


Fig. 8. Proposed class E PA with CIN compensation circuit.

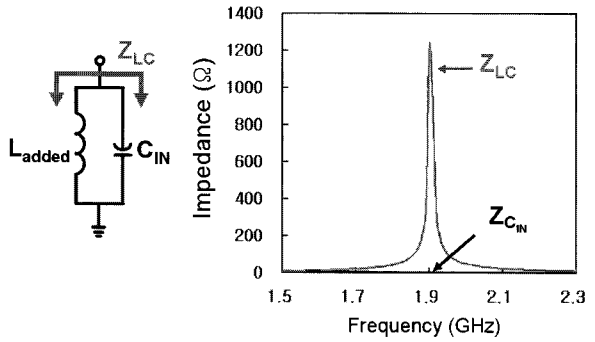


Fig. 9. LC resonance circuit and its impedance as a function of frequency.

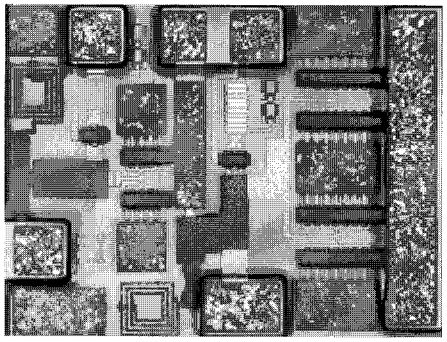


Fig. 10. Chip photograph of two-stage MMIC class E PA.

wave. Since a conventional input matching circuit is made only for reducing the signal return loss and the circuit cannot compensate the high C_{IN} effect, this resonance circuit is required.

A photograph of this MMIC PA is shown in Fig. 10. The MMIC includes matching networks for input, inter-stage and bias circuits. Output matching components are composed of off-chip capacitors and inductors. L_{added} for compensation and DC block capacitor are composed of bonding wire and off-chip capacitor, respectively. The chip size is as small as 0.890 X 0.670 mm^2. This MMIC was fabricated using commercially available 2 μm emitter width InGaP/GaAs HBT technology, which is comprised of units with 80 μm^2 emitter area. Each emitter area in the drive and power amplifier is 640 μm^2 and 2560 μm^2, respectively.

Fig. 11 shows the measurement results of the power gain and input return loss for the two-stage power amplifier with a supply of 3.4 V. The power gain is over 15 dB at 1.9 GHz. The quiescent currents of drive and power stage are 4 mA (for class AB) and 2 mA (for class E), respectively. Fig. 12 shows the measurement results of the output power and collector efficiency at 1.9 GHz. The maximum output power is 28.5 dBm for the conventional case and 29 dBm for the compensation case. The collector efficiency at 27 dBm output power is 64 % for the conventional case and 71 % for the compensation case. Even though the measured efficiency is lower than the simulated efficiency, we can confirm the improvement by the C_{IN} compensation of the LC resonance circuit.

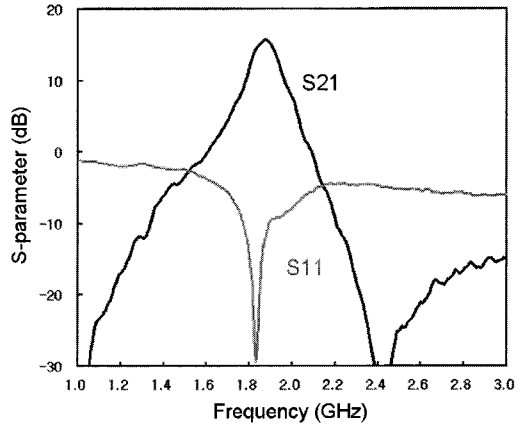


Fig. 11. Measured gain (S21) and input return loss (S11).

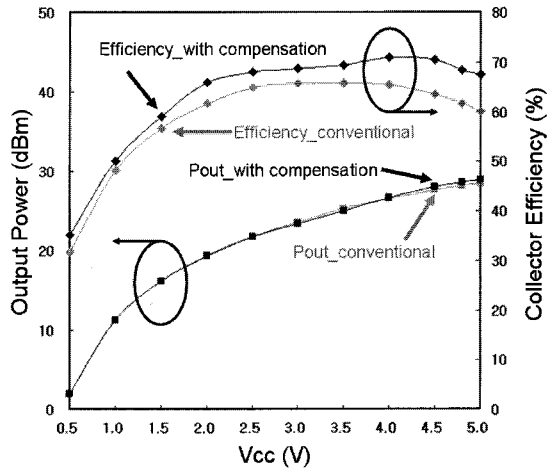


Fig. 12. Measured output power and collector efficiency.

V. CONCLUSIONS

We analyze the new class E operation with the effect of the increased input capacitance (C_{IN}) for the high output power level and demonstrate the efficiency improvement of the class E PA having a parasitic capacitance compensation circuit. Using an LC resonance circuit in which the C_{IN} can be tuned out at the wanted frequency, we obtain 7 % efficiency improvement at a similar output power level.

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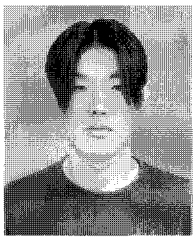

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