A Delta-Sigma Fractional-N Frequency Synthesizer for Quad-Band Multi-Standard Mobile Broadcasting Tuners in 0.18-μm CMOS

Jaewook Shin, Jongsik Kim, Seungsoo Kim, and Hyunchol Shin

Abstract—**A fractional-N frequency synthesizer supports quadruple bands and multiple standards for mobile broadcasting systems. A novel linearized coarse tuned VCO adopting a pseudo-exponential capacitor bank structure is proposed to cover the wide bandwidth of 65 %. The proposed technique successfully reduces the variations of KVCO and per-code frequency step by 3.2 and 2.7 times, respectively. For the divider and prescaler circuits, TSPC (true single-phase clock) logic is extensively utilized for high speed operation, low power consumption, and small silicon area. Implemented in 0.18-μm CMOS, the PLL covers 154 ~ 303 MHz (VHF-III), 462 ~ 911 MHz (UHF), and 1441 ~ 1887 MHz (L1, L2) with two VCO's while dissipating 23 mA from 1.8 V supply. The integrated phase noise is 0.598 and 0.812 degree for the integer-N and fractional-N modes, respectively, at 750 MHz output frequency. The in-band noise at 10 kHz offset is -96 dBc/Hz for the integer-N mode and degraded only by 3 dB for the fractional-N mode.**

Index Terms—**Delta-Sigma, Fractional-N Frequency, Synthesizer, Quad-band, mobile broadcasting tuners**

I. INTRODUCTION

Mobile broadcasting system is gaining a substantial market share these days. One of the issues in implementing the system is that many different standards at different frequency bands exist worldwide because of the regional situations and legacy techniques. Table 1 lists major mobile broadcasting systems and their frequency bands. In Europe, DVB-H and DAB are serviced in UHF band. L1 band currently used for DAB service is also considered to be reallocated for DVB-H service. In Korea, T-DMB is serviced in VHF-III. In US, L2 band at 1672.5 MHz with 5 MHz bandwidth is allocated for DVB-H. MediaFLO operates from 698 to 746 MHz. In Japan, ISDB-T is serviced in VHF and UHF bands. In order to cope with the multi-standard multi-band situations worldwide, modern mobile tuner IC's need to support them seamlessly. In that regard, previous tuner IC's and their embedded frequency synthesizers showed limited frequency coverage as mostly focusing on dual-band operation [1-6].

Table 1. Worldwide Mobile Broadcasting Systems.

Band (MHz)	T-DMB	DAB	DVB-H	MediaFLO	ISDB-T
VHF-III	174 ~ 216	174 ~ 240	170 ~ 230		
UHF-IV/V			470 ~ 862(EU)	698 ~ 746	470 ~ 770
L1	1452 ~ 1492	1452 ~ 1492	1452 ~ 1492		
L2 (US L-Band)	1670 ~ 1675(US)				

In this work, we present a CMOS fractional-N frequency synthesizer that supports all the quadruple bands that are currently allocated worldwide for mobile broadcasting. The supported quad-bands are VHF-III of 170 ~ 240 MHz, UHF of 470 ~ 862 MHz, L1 of 1450 ~ 1492 MHz, and L2 of 1670 ~ 1675 MHz. Architecture and circuit techniques to realize this PLL are described in this paper.

II. ARCHITECTURE

Integer-N architecture adopted for the mobile tuners in [5, 6] is not suitable for supporting the multiple bands

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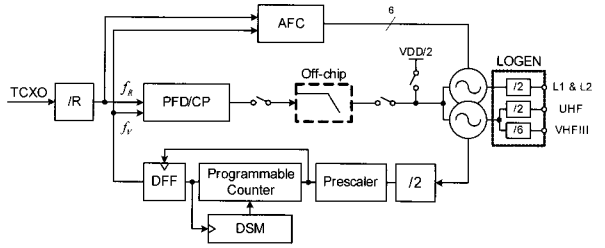


Fig. 1. Frequency synthesizer architecture.

and multiple standards. Therefore, fractional-N architecture with a third-order multi-bit delta sigma modulator (DSM) is realized. Fig. 1 shows the PLL architecture. Two VCO's cover the quad-band; a high-band VCO (VCOH) covering 2900 ~ 3350 MHz and a low-band VCO (VCOL) covering 940 ~ 1724 MHz. LOGEN block generates LO signals, in which the divide-by-6 is used for the VHF band and the divide-by-2's are used for L1/L2 and UHF bands. These divider circuits are based on the current-mode logic (CML) DFF for simple I/Q generation. Meanwhile, the divide-by-2 and the 4/5 dual-modulus prescaler in the feedback path are designed by utilizing true-single-phase-clock (TSPC) logic. A DFF after the programmable counter synchronizes its output to the prescaler output. This re-timing block significantly eliminates the accumulated phase noise created by the asynchronous programmable counter. Automatic frequency control (AFC) block is based on the pulse-counting and comparison method. The number of the pulse-counting and comparison operation is programmable so that the lock time can be optimized. Typical AFC search time for the 6-bit coarse tuning is less than 150 μsec. A third order loop filter is used, of which only three components are implemented off chip.

III. Building Block Design

3.1 Wideband VCO with Linearized Coarse Tuning

Fig. 2 shows the VCO circuit schematic. A regulating amplifier is employed to reduce the power supply sensitivity of the VCO and thereby its phase noise contribution. Reference voltage V_{REF} is generated by a replica circuit with a bandgap reference current. The simulated output noise of the bandgap circuit is 12.2 and 10.9 nV/√Hz at 100 kHz and 1 MHz, respectively. A low pass filter of R_5 and C_5 is employed to further suppress the noise transferred from the regulator.

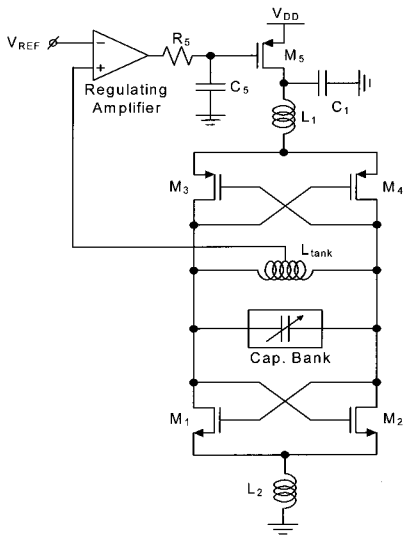


Fig. 2. VCO circuit schematic.

Conventional binary weighted cap bank is utilized for the VCOH whose fractional bandwidth is about 25 %. However, for the VCOL whose fractional bandwidth is over 70 % considering PVT variations, the conventional cap bank cannot be used due to the extremely wide tuning range. The K_{VCO} and the frequency step per a cap bank code vary over 10 times. Such a big K_{VCO} variation makes difficult optimal design of the PLL loop characteristics, possibly leading to severe degradation of phase noise and lock time in some channels. The big variation of the per-code frequency step also prohibits optimal design of AFC search time because the number of pulse-counting must be set unnecessarily high enough to detect the smallest frequency step. Hauspie et al. proposed a combined tuning technique of capacitor bank, varactor, and active core size to address these problems [7]. However, we found that the method showed very limited effects for such a wide bandwidth of this work due to the conventional binary-weighted cap bank structure.

Here we propose a novel pseudo-exponential cap bank structure. Fig. 3 shows the structure. It consists of a subsection cap bank, a variable-slope linear cap bank, and a varactor bank. Fig. 4 illustrates the effects of the proposed cap bank by comparing the coarse tuning characteristics that can be obtained by the proposed and the conventional cap bank structures. Since the VCO output frequency is determined by $1/(2\pi\sqrt{LC})$, it would be ideal to make the total capacitance of a cap bank vary in an exponential form of n^{-2} with respect to the cap bank code n. However, this is not practical for real implementation because of the

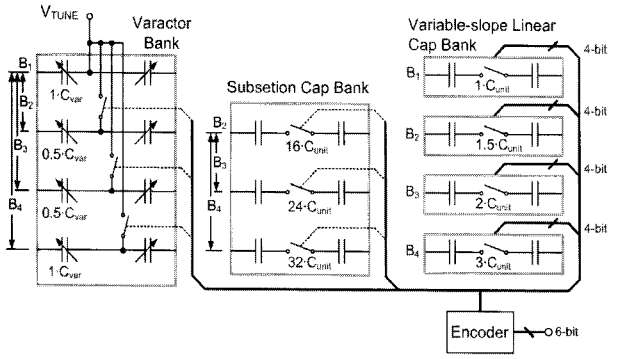


Fig. 3. Pseudo-exponential capacitor bank structure.

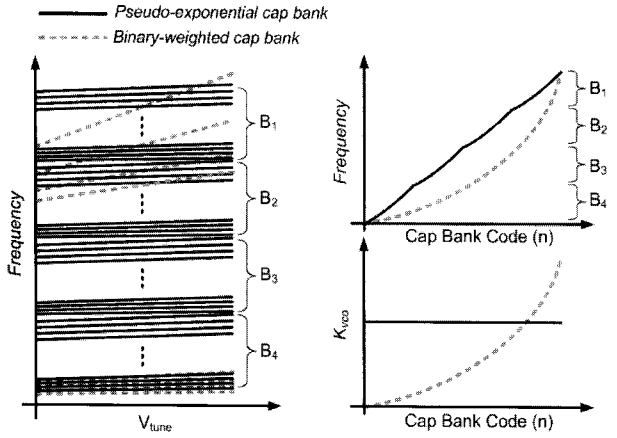
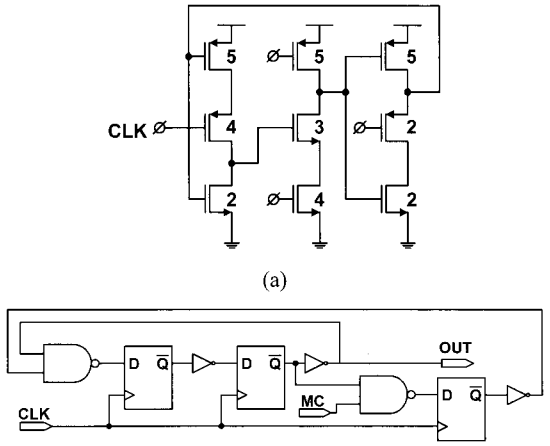


Fig. 4. Comparison of coarse tuning characteristics by the conventional binary-weighted cap bank and the proposed pseudo-exponential cap bank structure. (a) Frequency tuning characteristics. (b) Frequency and K_{vco} variation against the cap bank tuning code at a fixed V_{tune}.

extremely huge ratio of the maximum and minimum capacitances (e.g. 64^2 for 6-bit coarse tuning in VCO).

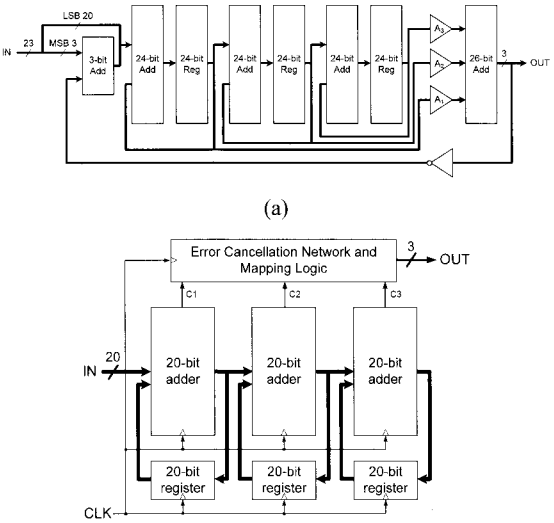
Thus, we mimic the n^{-2}-dependency by using a pseudo-exponentially varying capacitance. As shown in Fig. 4, the total tuning range is divided into four subsections (B_n). Within each subsection, capacitance varies linearly with a different slope. The slope is determined by the different unit capacitance which varies from $1 \cdot C_{unit}$ to $3 \cdot C_{unit}$ in each subsection. During the inter-subsection transitions, the cumulative capacitance is re-adjusted in the subsection cap bank to make the total capacitance vary smoothly. Also, the varactor capacitance is adjusted in each subsection by the varactor bank in order to keep the K_{VCO} constant. This proposed structure is adopted for the wideband VCOL, which is referred to as VCOL-LCT. By using this structure, the coarse tuning characteristics are dramatically linearized.



(a)

(b)

Fig. 5. (a)TSPC divide-by-2 circuit and (b) TSPC 4/5 prescaler logic diagram.



(a)

(b)

Fig. 6. Logic block diagram of designed delta-sigma modulators with 20-bit resolution. (a) 3rd-order 3-bit single-loop CIFF and (b) MASH-111.

3.2 Divide-by-2, 4/5-Prescaler, and PFD in TSPC logic

The divide-by-2 and 4/5 dual-modulus prescaler in the feedback path are realized in the TSPC logic. Fig. 5(a) shows the circuit schematic of the divide-by-2, where the FET widths are shown while the gate length is minimum 0.18 μm. The widths are optimized for high speed operation and large swing by trading off the self-capacitance and the driving capability. The same DFF is also used for the dual-modulus prescaler, whose circuit is shown in Fig. 5(b). In the simulation, the maximum operation frequencies of the divide-by-2 and the prescaler are 6 GHz and 3.5

GHz in the worst condition, while they goes up to 9 GHz and 4.5 GHz in the typical condition. Moreover, the current consumption of the prescaler is only 0.8 mA. We have found that the TSPC logic dramatically reduces the power consumption and silicon area compared to the conventional CML logic. The TSPC logic DFF is also used in the PFD circuit in order to minimize the timing mismatch of the UP/DN pulses.

3.3 Delta-Sigma Modulator

In general, DSM poses significant impacts on the phase noise performance of the PLL. We implement two types of DSM: a 3rd-order 3-bit single-loop DSM of CIFF (cascaded integrators with distributed feedforward) type which is similar to that in [8] and MASH-111 with 20-bit resolution. Fig. 6 shows the block structures of single-loop modulator and MASH-111. In single-loop modulator, the coefficients A_1, A_2, and A_3 are 2, 1.5, and 0.5, respectively. Fig. 7 shows the simulated PSDs (power spectral density) of each modulator. It is clearly seen that both are non-tonal. Fig. 8 compares NTFs (noise transfer function) of MASH-111 and single-loop modulator. It clearly exhibits the great difference of the NTF's of the two DSMs. According to the linear analysis results, the maximum and integral quantization noises of the implemented single-loop architecture are found to be considerably less than the conventional MASH-111 structure, only about 40 % and 28 %, respectively. Time-domain simulation is also performed to examine the dynamic range. Fig. 9 shows the internal node values in the DSM with respect to the input value. As can be seen, the dynamic range of this architecture is about -2.5 ~ +2.0, which is significantly larger than the conventional MASH-111 whose dynamic range is only -0.5 ~ +0.5. The time-domain simulation also shows the number of output levels is only about 4 while that of the MASH-111 is 8, possibly leading to less noise folding and lower in-band noise. For these advantages, the single-loop CIFF architecture is chosen in this work.

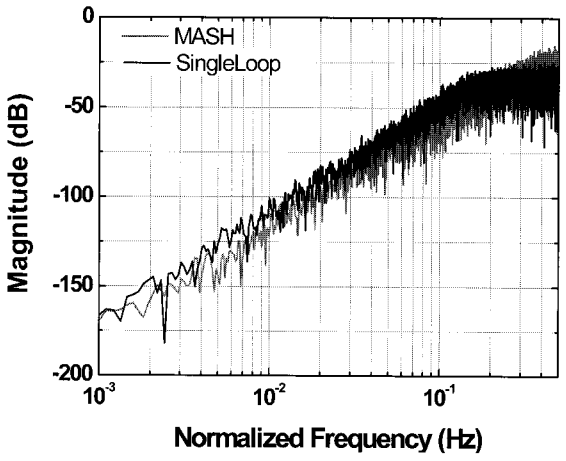


Fig. 7. Simulated power spectral density of MASH-111 and single-loop delta-sigma modulators.

IV. Measurement Results

The frequency synthesizer was fabricated in a 0.18-μm RF CMOS process. Fig. 10 shows the chip micrograph. The die area is 2.5×2.5 mm^2. It is packaged in a 40-pin leadless plastic chip carrier (LPCC) and tested on an evaluation printed circuit board with a 1.8-V supply. It dissipates 21 mA for UHF/L1/L2 bands and 23 mA for VHF band. The slight additional currents at VHF band is consumed by the divider-by-6 in the LOGEN block.

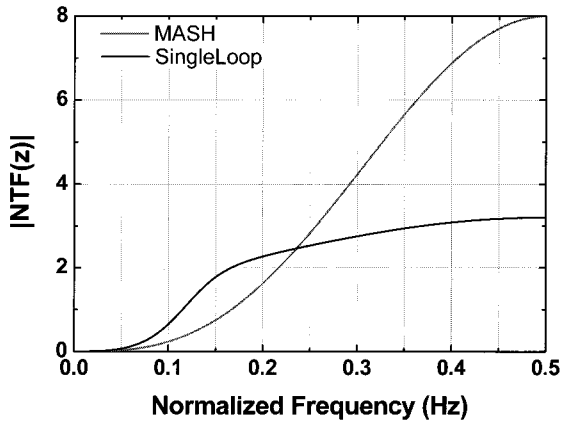


Fig. 8. Noise transfer function of MASH-111 and single-loop delta-sigma modulators.

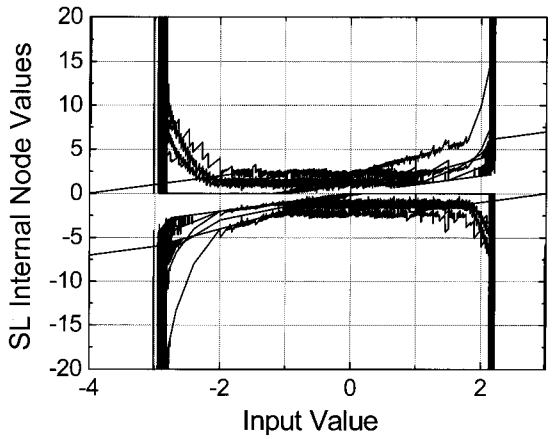


Fig. 9. Dynamic range simulation of the single-loop delta-sigma modulator.

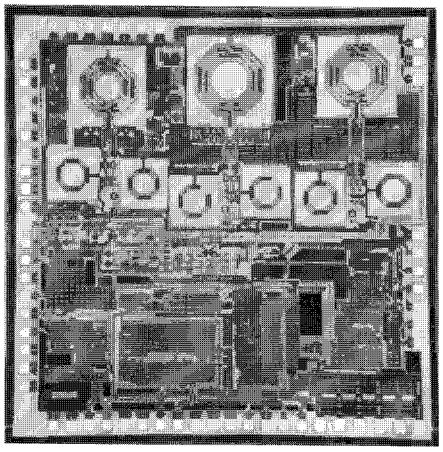


Fig. 10. Chip micrograph.

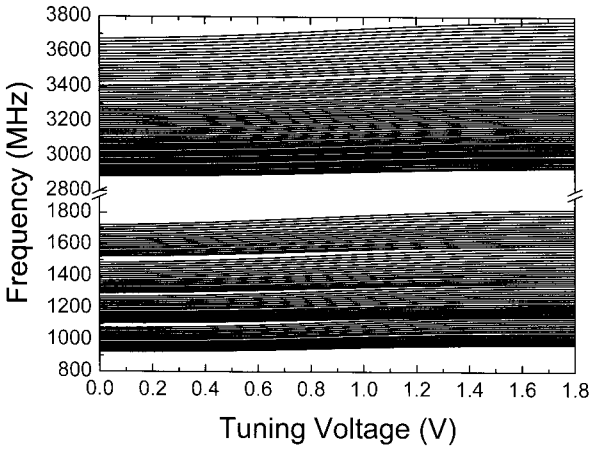


Fig. 11. Measured frequency tuning characteristics of the low-band and high-band VCO's.

Fig. 11 shows the measured frequency tuning ranges of the VCOH and VCOL-LCT which are 2882 ~ 3775 MHz and 924 ~ 1823 MHz, respectively. They successfully cover the target ranges. The measured phase noises are -90 dBc/Hz at 100 kHz offset and -122 dBc/Hz at 1.45 MHz offset for the 3 GHz output frequency in the VCOH, and -110 dBc/Hz at 100 kHz offset and -135 dBc/Hz at 1.45 MHz offset for the 1-GHz output frequency in the VCOL-LCT.

In order to examine the effects of the proposed pseudo-exponential cap bank structure, a test VCO with the conventional cap bank structure is also fabricated and compared. Fig. 12 shows the measured coarse tuning characteristics of VCOL and VCOL-LCT. For the VCOL, the ranges of the K_{VCO} and the frequency step are 23 ~ 123 MHz/V and 5 ~ 29 MHz/code, respectively. For the VCOL-LCT, they are reduced to 37 ~ 72 MHz/V and 9 ~ 16 MHz/code at V_{tune} = 0.9 V. Thus the variation of

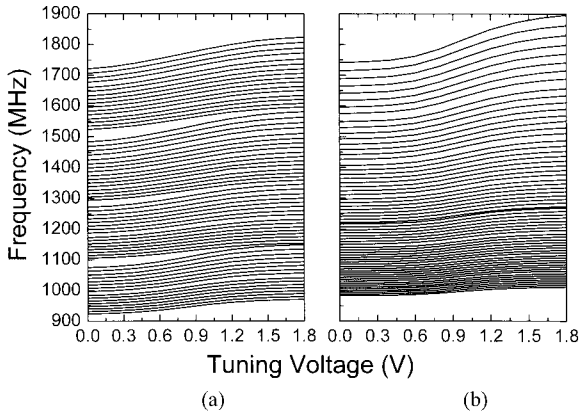


Fig. 12. Measured frequency tuning characteristics of the low band VCO with (a) the proposed pseudo-exponential cap bank and (b) the conventional binary weighted cap bank.

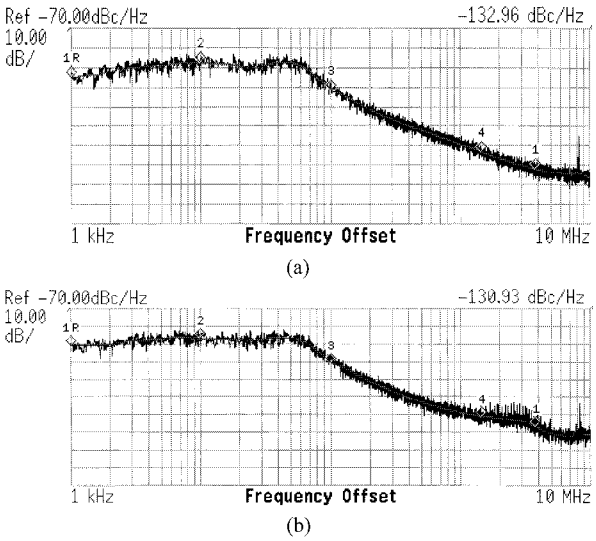


Fig. 13. PLL phase noise measurement. (a) Integer-N mode at 825.6 MHz. (b) Fractional-N mode at 827.5 MHz.

K_{VCO} is reduced from 530 % to 190 % and the variation of the frequency step is reduced from 580 % to 180 %. They correspond to 3.2- and 2.7-times reduction, respectively.

Fig. 13 shows the measured phase noise of the PLL. In the measurement, the loop bandwidth is 70 kHz, the reference frequency is 19.2 MHz, and the charge pump current is 2 mA. Fig. 13(a) is for the integer-N mode with the output frequency of 825.6 MHz and Fig. 13(b) is for the fractional-N mode with the output frequency of 827.52 MHz where the DSM output value is +0.1. The in-band noise at 1 kHz is -95 dBc/Hz for the integer-N mode and becomes -91.2 dBc/Hz for the fractional-N mode, which is only 3.8-dB degradation. The phase noises at 100 kHz and 1.45 MHz offsets are -101.7 and -132.9 dBc/Hz for the integer-N mode, and -100.9 and -130.9 dBc/Hz for the fractional-N mode. In the fractional-

N mode, residual quantization noise is slightly observed at around 2 MHz offset. Integrated phase noise is a crucial factor affecting the signal-to-noise ratio in OFDM signal. The phase noise integrated from 1 kHz to 3.8 MHz is measured to be 0.807 degree (-37.0 dBc) and 0.910 degree (-35.9 dBc) for the integer-N and fractional-N modes, respectively. At lower output frequencies, the phase noise performances become better. For instance, at an output frequency of 500 MHz, the integrated phase noise is measured to be 0.145 and 0.244 degree for the integer-N and fractional-N modes, respectively. It successfully meets the DVB-H requirement of -33 dBc [5]. Meanwhile, the reference and fractional spur are measured to be lower than -70 dBc and -50dBc, respectively. The lock time is measured to be less than 150 μsec including the 6-bit AFC search time.

V. CONCLUSIONS

A CMOS fractional-N frequency synthesizer to support the quadruple bands and multiple standards for mobile broadcasting systems has been presented. The novel linearized coarse tuned VCO with a pseudo exponential capacitor bank structure is proposed to cover the wide bandwidth. Implemented in 0.18-μm CMOS technology, the PLL successfully covers 154 ~ 303 MHz (VHF), 462 ~ 911 MHz (UHF), and 1441 ~ 1887 MHz (L1, L2) with satisfactory phase noise performances.

ACKNOWLEDGMENTS

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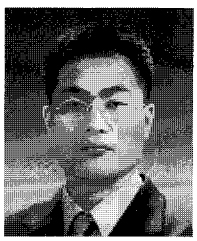

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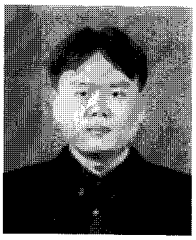

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