A New Scan Chain Fault Simulation for Scan Chain Diagnosis

Sunghoon Chun, Taejin Kim, Eun Sei Park, and Sungho Kang

Abstract—**In this paper, we propose a new symbolic simulation for scan chain diagnosis to solve the diagnosis resolution problem. The proposed scan chain fault simulation, called the SF-simulation, is able to analyze the effects caused by faulty scan cells in good scan chains. A new scan chain fault simulation is performed with a modified logic ATPG pattern. In this simulation, we consider the effect of errors caused by scan shifting in the faulty scan chain. Therefore, for scan chain diagnosis, we use the faulty information in good scan chains which are not contaminated by the faults while unloading scan out responses. The SF-simulation can tighten the size of the candidate list and achieve a high diagnosis resolution by analyzing fault effects of good scan chains, which are ignored by most previous works. Experimental results demonstrate the effectiveness of the proposed method.**

Index Terms—**Scan chain based test, Symbolic simulation, Scan chain diagnosis**

I. INTRODUCTION

Scan chains are instantiated in an integrated circuit (IC) design to provide better controllability and observability of functional logic for structural test and design debug. During IC test, the scan chains themselves are tested to assure that they function properly. In addition, reduced scan chain yield can impact IC manufacturing yields. As a result, methods that facilitate scan chain diagnosis are important component to improve the yield.

Scan chain fault diagnosis is the process of identifying the defective scan cell in a scan chain. Several methods have been proposed to diagnose scan chain failures. Previous scan chain fault diagnosis methodologies are classified into two categories. The first category is hardware-based methods [1-4], which needs hardware modification beyond the basic scan design through special scan cell design or additional circuitry. These special designs are then used to facilitate the scan chain diagnosis process. However, these techniques may not be acceptable because of their area overhead, performance penalty and occurrence possibilities of other faults caused by additional circuits.

Scan chain fault diagnosis is the process of identifying the defective scan cell in a scan chain. Several methods have been proposed to diagnose scan chain failures. A number of hardware-based methods were proposed in the literature [1-4]. However, these techniques may not be acceptable because of their area overhead, performance penalty and occurrence possibilities of other faults caused by additional circuits.

The second category is software-based diagnosis method [5-11]. The first step of most software-based methods is, using flush test patterns [6], to identify faulty scan chains and determine the fault model for each faulty scan chain. Next, the defective scan cells are isolated using the sequential ATPG or logic simulation with unknown values. In [5], sequential ATPG techniques were used in order to set the scan cells to specific values and the diagnosis information is collected during unloading of the scan cells. However, the use of sequential ATPG techniques leads to significant complexity and time consuming.

Manuscript received Nov. 3, 2007; revised Nov. 30, 2007.
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Instead of using sequential ATPG techniques, logic simulation and matching algorithm were used to find the best possible faulty scan cell [6,7]. However, since they use logic simulation without the effects caused by faulty scan cells, they could not achieve high diagnosis resolution and lead to time consuming. To tighten the bounds of candidate scan cells quickly, the Jump simulation is proposed in [8]. Although the jump simulation method quickly identifies a pair of precise upper and lower bounds for high diagnosis resolution, the jump simulation technique is applicable to single faults but has limitations for multiple faults in the scan chain. In addition, though most recent circuits have multiple scan chains not a single scan chain to reduce test application time and the test complexity, previous software-based diagnosis methods could not efficiently use the faulty information in good scan chains which are not contaminated by the faults while unloading scan out responses.

To alleviate these problems, we propose a new symbolic simulation method for scan chain diagnosis, called the SF-simulation. The basic idea of the SF-simulation is to simulate with the faulty probabilities of a set of candidate faulty scan cells in a bounded range and to analyze the effects caused by the faults of faulty scan cells in good scan chains. Therefore, for scan chain diagnosis, since we can use the faulty information in good scan chains which are not contaminated by the faults in the faulty scan chain while unloading scan out responses, the scan chain diagnosis using the SF-simulation can achieve high diagnosis resolution for a single fault as well as multiple faults.

The organization of this paper is as follows. In Section 2, we propose a new scan chain fault simulation for the scan chain diagnosis to enhance the scan chain diagnosis resolution for single and multiple faults in the scan chain. Section 3 presents experimental results of ISCAS '89 and ITC '99 benchmark circuits to demonstrate the effectiveness of the proposed method. Finally, the last section concluded this paper.

II. The Proposed Scan Chain Fault Simulation

The proposed symbolic simulation method for scan chain diagnosis, called the SF-simulation, consists of two procedures: 1) SF pattern maker and 2) SF symbolic simulation. The proposed method takes the circuit description and its scan chain design as the input.

Before the SF-simulation, the scan chains are tested using flush test patterns to determine the faulty scan chain as the initial procedure of the scan chain diagnosis. In addition, for a single fault assumption, the fault type is identified during flush test. First procedure of the SF-simulation, the SF pattern maker, is to inject the new scan cell fault values proposed to represent the information of the fault candidate scan cell into the faulty scan chain in order to consider the effect of the faulty scan cell in the faulty scan chain. Next, the logic simulation with the new scan cell fault values, the SF symbolic simulation, is performed to apply the effect of faulty scan cell to the CUT.

Fig. 1 shows the procedure of the proposed symbolic simulation method for the scan chain diagnosis and the overall flow chart of the scan chain diagnosis.

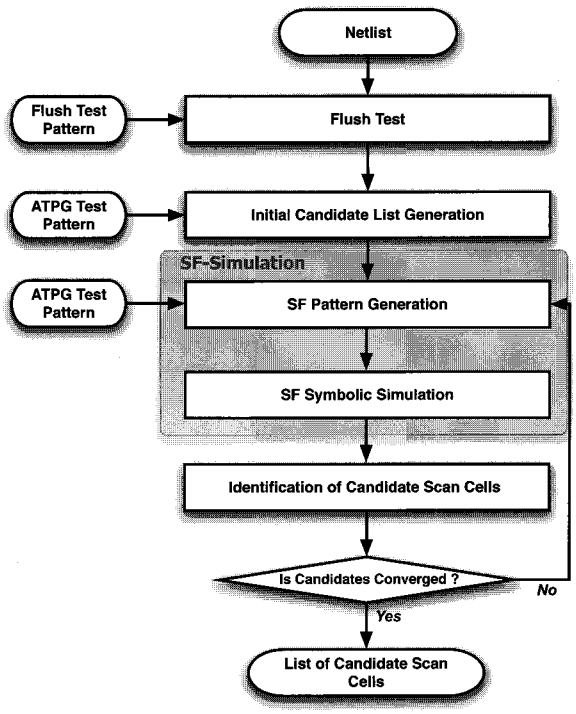


Fig 1. Overall procedure of scan chain diagnosis using the SF-simulation.

2.1 The SF Pattern Generation

Initially, to determine the faulty scan chain, flush test patterns which are special test patterns used in [6] are applied in this paper. In faulty scan chain, by comparing

the faillog response and the original logic simulation response, the upper bound calculation [7] is applied in order to generate the initial candidate list and to reduce symbols for the proposed symbolic simulation.

After generating the initial candidate list, to consider the effect of the faulty scan cell in the candidate list and to more exactly identify the location of the faulty scan cell using the information of good scan chains, a new symbolic simulation method, SF-simulation(Scan cell Fault simulation), is proposed for scan chain diagnosis. The SF-simulation differs from the conventional fault simulation, because it assumes that there are faults only in the scan chain and all the logics except the faulty scan chain are fault free. Therefore, for the SF-simulation, faults are inserted only to the scan cells in the candidate list and then fault free circuit N is simulated, while, for the conventional fault simulations, the fault free circuit N is transformed to the circuit N_f created by the logic fault f in the target fault lists and then the faulty circuit N_f is simulated. For the conventional fault simulations, it is very time consuming operation since the simulation time depends heavily on the number of target faults. However, for the proposed symbolic simulation, it is a very simple operation since the faulty scan chain model S_f is transformed to apply the effect of the faulty scan cell in the faulty scan chain, and just a single logic simulation is performed.

The proposed SF-simulation consists of two phases. First, to consider the effect of the faulty scan cell in the faulty scan chain, the new scan cell fault values proposed to represent the information of the fault candidate scan cell are injected into the faulty scan chain. Next, the logic simulation with the new scan cell fault values is performed to apply the effect of faulty scan cell to the CUT.

In addition to the logic states {0, 1, X}, we introduce a new symbolic logic state SF_i, which means the location of fault candidate scan cell, that is, the ith scan cell in the faulty scan cell for considering the effect of faults in the faulty scan chain and for distinguishing the location of the faulty scan cell. Fig. 2 shows how to inject a new symbol into the faulty scan chain. Note that a test pattern included in the new symbolic logic states SF_i is called an SF pattern.

	Candidate Scan Cells					Stuck-at 1			
Scan Cell Index	SC_1	SC_2	SC_3	SC_4	SC_5	SC_6	SC_7	SC_8	SC_9
Good Test Pattern	0	1	1	0	1	0	0	0	1
Real Scan-In Pattern	0	1	1	0	1	1	1	1	1
SF Pattern	SF_1	SF_2	SF_3	SF_4	SF_5	SF_6	1	1	1
1st SF Pattern	SF_1	SF_2	SF_3	X	X	X	1	1	1
2nd SF Pattern	X	X	X	SF_4	SF_5	SF_6	1	1	1

Fig 2. An example of a SF pattern.

In Fig. 2, if a test pattern applied after the calculation of the candidate list is "011010001", then the actually loaded test pattern to the faulty scan chain may be "011011111". It is clear that the test response for the loaded scan-in pattern is different from the simulation response of the original test pattern which does not consider the effect of the faulty scan cell SC_6. Therefore, there are significant mismatches between the simulation result and the unloaded test response in the faulty scan chain as well as in good scan chain. It diminishes the precision of the scan chain diagnosis. To alleviate this problem, new states, SF_1~SF_6, are injected to the candidate scan cells in the candidate list. In addition, the test pattern values from SC_7 to last scan cell SC_9 are set to the faulty value since they are located after the candidate list and they are affected by the last faulty cell during the scan-in shifting. Therefore, the simulation results with the SF pattern are similar to the faillog response and the SF states can help to reduce the number of the fault candidates since some SF states can be propagated to scan-out responses of good scan chains or primary outputs.

The proposed SF-simulation has a disadvantage. This simulation requires many symbols for SF values in the candidate list when the size of the candidate window is quite large. The worst case is when the upper bound is the last cell of the faulty scan chain. Since the usage of many symbols enlarges the calculation of symbolic simulation, it can make the symbolic simulation not so effective. To alleviate this problem, we use the binary or quartering division that is performed by ruling out half or quarter of the current candidate list at each SF-simulation. For binary division, as shown in Fig. 2, the candidate list is divided by half of its size and then the SF values and the don't care values are injected into the foregoing part of the divided candidate list and the remaining part, respectively. After that the simulation responses of the 1st SF patterns are stored, the "X" values and the SF values are injected into the foregoing part and the remaining part, respectively.

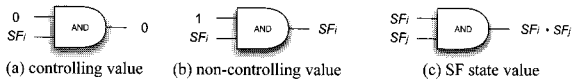
2.2 The SF Symbolic Simulation

After injecting the SF states in the faulty scan chain, the logic simulation with the SF pattern is performed. For the logic simulation, we propose a heuristic method for three reasons; 1) to easily evaluate logic values, {0, 1, X, SFi}, 2) to reduce the memory size for the evaluation of the SF states and 3) to simplify the analysis to diagnose the faulty scan chain.

In general, a gate output value is determined by the controlling value if there is an input signal at a minimum, which has the controlling value. Otherwise, the gate is evaluated like a buffer or an inverter. Similarly, as shown in Fig. 3(a), the specified value is propagated to the output of the gate when the input signal is a SF state and the input signal of the remaining input signals is a controlling value. If all the side input signals except one input which has a SF state have non-controlling value, the gate output value is determined by the value of the SF state (Fig. 3(b)). In addition, the output value is evaluated for the product of the SF state values if there are two SF input signals or more for any gate types (Fig. 3(c)). If the evaluation results of two SF input signals are propagated to the primary outputs or to the scan outputs as logical forms or CNF forms, such as $SF_i \& SF_k$, then a big memory size would be required and the computation complexity to analyze the SF evaluation results propagated to the outputs would be enormously increased. Therefore, we use the product forms of the SF state values as the SF evaluation method.

Using this implementation method for the SF values with ATPG patterns, the original logic values, {0, 1, X} and the SF values can be propagated to the primary outputs and the scan cells and then the simulated output values can be stored as the SF response.

Definition 1: (SF response) The SF response of a scan chain is the value combination of SF-simulated outputs after the SF simulation with a SF pattern.



(a) controlling value (b) non-controlling value (c) SF state value

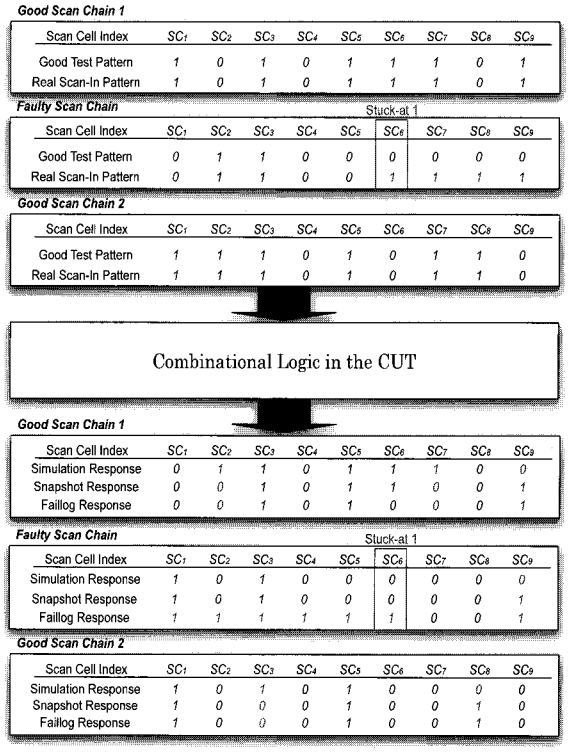
Fig 3. The SF value implementation according to the side input.

In the binary division case of the SF pattern, therefore, two SF-simulations are performed and two SF responses are stored per test pattern. These SF responses are used to determine the candidate scan cells by the diagnosis method.

2.3 Identification of Candidate Scan Cells

To identify the location of the faulty scan cell, three output responses must be compared: (1) simulation response set R_{sim}, (2) faillog response set R_{fail} and (3) SF response set R_{SF}. In this procedure, the output responses of the good scan chains should be used, while the information of the faulty scan chain is used in the procedure of generating candidate scan cell window.

As shown in Fig. 4, the faillog responses are different from the simulation responses in the faulty scan chain as well as the good scan chains because the faulty scan cell affects the scan-in pattern and then the effects of the faulty scan cell are propagated to both the faulty scan chain and the good scan chains. For example, in good scan chain 1 of Fig. 4, the simulation values of SC_2, SC_7 and SC_9 are contrary to real scan-out values.



Good Scan Chain 1

Scan Cell Index	SC_1	SC_2	SC_3	SC_4	SC_5	SC_6	SC_7	SC_8	SC_9
Good Test Pattern	1	0	1	0	1	1	1	0	1
Real Scan-In Pattern	1	0	1	0	1	1	1	0	1

Faulty Scan Chain — Stuck-at 1

Scan Cell Index	SC_1	SC_2	SC_3	SC_4	SC_5	SC_6	SC_7	SC_8	SC_9
Good Test Pattern	0	1	1	0	0	0	0	0	0
Real Scan-In Pattern	0	1	1	0	0	1	1	1	1

Good Scan Chain 2

Scan Cell Index	SC_1	SC_2	SC_3	SC_4	SC_5	SC_6	SC_7	SC_8	SC_9
Good Test Pattern	1	1	1	0	1	0	1	1	0
Real Scan-In Pattern	1	1	1	0	1	0	1	1	0

Combinational Logic in the CUT

Good Scan Chain 1

Scan Cell Index	SC_1	SC_2	SC_3	SC_4	SC_5	SC_6	SC_7	SC_8	SC_9
Simulation Response	0	1	1	0	1	1	1	0	0
Snapshot Response	0	0	1	0	1	1	0	0	1
Faillog Response	0	0	1	0	1	0	0	0	1

Faulty Scan Chain — Stuck-at 1

Scan Cell Index	SC_1	SC_2	SC_3	SC_4	SC_5	SC_6	SC_7	SC_8	SC_9
Simulation Response	1	0	1	0	0	0	0	0	0
Snapshot Response	1	0	1	0	0	0	0	0	1
Faillog Response	1	1	1	1	1	1	0	0	1

Good Scan Chain 2

Scan Cell Index	SC_1	SC_2	SC_3	SC_4	SC_5	SC_6	SC_7	SC_8	SC_9
Simulation Response	1	0	1	0	1	0	0	0	0
Snapshot Response	1	0	0	0	1	0	0	1	0
Faillog Response	1	0	0	0	1	0	0	1	0

Fig. 4. An example of the faillog responses.

Definition 2: (Propagated Fault Effects) The effects of the scan cell faults can be propagated to the faulty scan chain as well as the good scan chains. These effects are defined as the propagated fault effects (PFEs). Therefore, the good simulation responses of the good scan chains differ from both the snapshot responses and the faillog responses of them. Assuming that the circuit logics excluded in scan chains are fault-free, the errors of these mismatch locations (PFEs) must be caused by the faulty scan cell.

Using the SF-simulation, the information of the candidate scan cells can be propagated to the primary outputs and scan chain outputs and these output values are stored as the SF response set R_{SF}. Fig. 5 shows an example of the SF response set in the same case of Fig. 4.

As shown in Fig. 5, the SF values can be propagated to good scan chains and these values are key values for identifying the faulty scan cell in the candidate scan cell window in our proposed method.

Definition 3: (Propagated SF values) In SF responses, if only one SF_i value, not the product value of two or more SF values, is propagated to a good scan chain, this value is defined as a propagated SF value (PSFs). Note that the PSF in the faulty scan chain is not available because the value of the same location in the faillog response is affected by the faulty scan cell during the scan-out operation. In Fig. 5, SF_2 and SF_6 in the good scan chain 1 are the propagated SF values.

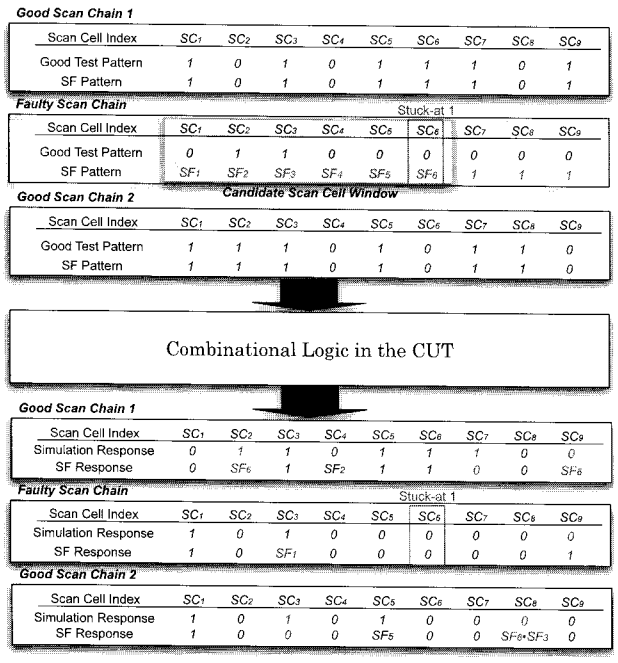


Fig. 5. An example of the SF response set R_{SF}.

Using the PFEs and the PSFs, we can reduce the list of candidate scan cells. Through comparing PFEs and the PSFs and the matching algorithm, we can determine final candidate scan cells which are significantly reduced than previous works. Since the matching algorithm based scan chain diagnosis method is not the scope of this paper, we omit the explanation of the matching algorithm with the SF responses in this paper.

III. EXPERIMENTAL RESULTS

To determine the effectiveness of the SF-simulation method, experiments were performed on ISCAS '89 and ITC '99 benchmark circuits of various sizes. A commercial tool that supports the scan chain insertion was used and an in-house tool that supports the combinational pattern generation was used as the ATPG engine. Note that scan chains for each circuit are inserted by using the commercial tool, the LBISTArchitect [12] in Mentor Graphics with the TSMC 0.25μm library. The proposed scan chain diagnosis method was implemented in C, and experiments were performed on a Blade 2000 system.

First we evaluate the ability of the diagnosis using the SF-simulation. Table 1 shows the size of the candidate list and the diagnosis resolution of the proposed scan chain diagnosis against the previous methods [7]. For the benchmark circuits, we injected 100 randomly selected

Table 1. Comparison of diagnosis resolutions for a single fault (average)

Circuits	# of scan chains	# of scan cells	DR [7]	DR [SF-Sym]	DA [7]	DA [SF-Sym]	CPU time (secs)
s5378	10	23	5.9	1.2	1	1	< 1
s9234	10	25	5.8	1.3	1	1	4
s13207	10	79	15.4	1.6	1	1	13
s15850	10	69	7.2	1.3	1	1	16
s38417	10	175	14.5	1.2	1	1	24
s38584	10	173	11.7	1.5	1	1	21
b10	2	12	1.2	1	1	1	< 1
b11	2	19	1	1	1	1	< 1
b12	5	26	2.4	1.1	1	1	< 1
b13	5	13	3.5	1.3	1	1	< 1
b14	10	30	2.5	1	1	1	20
b15	10	52	7.6	1.6	1	1	19

defects in scan chains and ran a simulation to obtain the fail log file. Table 1 shows the effectiveness of the diagnosis method using the SF-simulation for a single fault in a scan chain. Note that DR (diagnosis resolution) is defined as the size of the candidate list and DA in Table 1 is the diagnosis accuracy which means the probability of a real defect in the generated candidate list.

As shown in Table 1, for the proposed diagnosis method using the SF-Simulation, the number of candidate scan cells is significantly reduced. The smallest diagnosis resolution corresponds to b10, b11 and b14 circuits with a value of 1 and the largest to the circuit s13207 and b15 with a value of 1.6. Although all the injected real defects for simulation can be found in the generated candidate lists, the size of the fault candidate list for the proposed method is smaller than half of that of [7]. In addition, for the proposed method, the number of scan cells with the highest rank is one or two and this highest ranked scan cell is the location of the real injected fault. Therefore, even for a single fault, the proposed method is proven to be a more attractive method than the previous ones. Since the probability of the faulty effect in the fault site to be propagated to output responses is increased in larger VLSI circuits, the effectiveness of the proposed method for a single fault has grown increasingly greater as the size of the circuit is increased.

Fig. 6 illustrates the number of candidates versus the number of simulations for s38584 benchmark circuit, one of the largest circuits in ISCAS '89 benchmark circuits, to show the effectiveness of the SF-simulation. As shown in Fig. 4, the SF-simulation can significant reduce the number of simulations than that of [7]. In [7], over 1000 simulations are required to achieve the converged candidate list in this experiment. This means that the diagnosis using the SF-simulation can identify

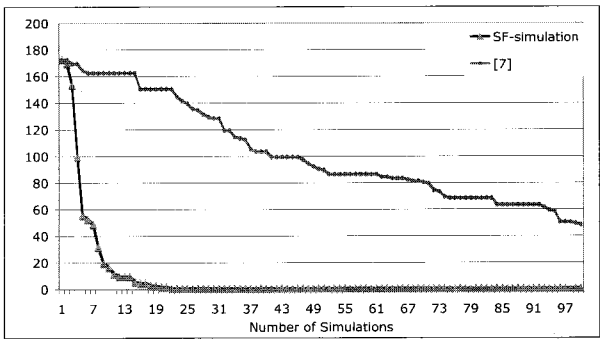


Fig. 6. The number of simulations for s38584.

the candidate scan cells quickly and precisely.

Finally, we performed the experiment with various conditions to demonstrate the effectiveness of the proposed diagnosis method for multiple faults in the benchmark circuit s38584. We applied 100 modified ATPG patterns and injected various fault models to compare exact locations of injected faults and candidate scan cells in the candidate list obtained from the proposed method. Table 2 shows that the experimental results of the proposed diagnosis method for five cases.

As shown in Table 2, all the injected fault models are listed in our candidate lists. In Table 2, columns 8 and column 9 present the size of the candidate list obtained from the proposed method and the probability of injected faults in the top 5 ranks of the candidate list, respectively.

For five cases, although some high scored candidate scan cells are not the real injected fault models, most high scored candidate scan cells are matched to the real injected fault models. This shows the effectiveness of the proposed technique to determine the locations of real defects in the scan chain. However, there are still several problems in our diagnosis method. For triple faults or more in the same faulty scan chain, the size of the candidate list is still large. In addition, the entire fault

Table 2. Experimental result for multiple faults in a scan chain.

Case	Scan cell index	Injected fault type	Scan cell index	Injected fault type	Scan cell index	Injected fault type	Size of candidate list	DR of top 5
1	10	Stuck-at 1	53	Stuck-at 0	-	-	6	1
2	34	Slow-to-Rise	72	Stuck-at 1	-	-	15	1
3	19	Slow-to-Fall	67	Stuck-at 1	154	Stuck-at 0	12	1
4	100	Stuck-at 0	124	Slow-to-Rise	171	Stuck-at-1	25	1
5	1	Hold Time	50	Fast-to-Fall	150	Stuck-at 0	38	0.66

types of the candidate scan cells cannot be identified in the proposed diagnosis technique. However, as an enhancement in the future, our diagnosis method using the SF-simulation is improved by the usage of the backtracing technique.

IV. CONCLUSIONS

This paper presents a new scan chain fault simulation method for the scan chain diagnosis. The proposed scan chain simulation method for scan chain diagnosis consists of two procedures: 1) SF pattern generation and 2) SF symbolic simulation.

The basic idea of the proposed scan chain fault simulation is to simulate with the faulty probabilities of a set of candidate faulty scan cells in a bounded range and to analyze the effects caused by the faults of faulty scan cells in good scan chains. Therefore, for scan chain diagnosis, since we can use the faulty information in good scan chains which are not contaminated by the faults in the faulty scan chain while unloading scan out responses, the scan chain diagnosis using the proposed simulation can achieve high diagnosis resolution for a single fault as well as multiple faults.

Experimental results show that the scan chain diagnosis using the proposed simulation can achieve high diagnosis resolution and high diagnosis accuracy for all benchmark circuits. In addition, the proposed method can significantly reduce the number of simulations for precise scan chain diagnosis. Therefore, the proposed symbolic simulation is very useful for fast and precise scan chain diagnosis.

ACKNOWLEDGMENTS

This work was supported by the Korea Science and Engineering Foundation Grant funded by the Korea government (MOST) (No. R01-2006-000-11038-0).

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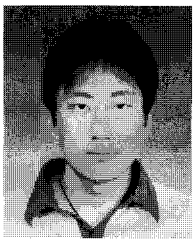

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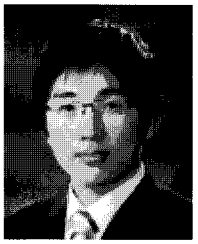

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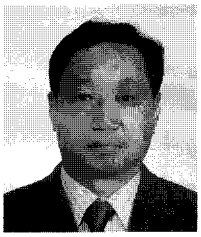
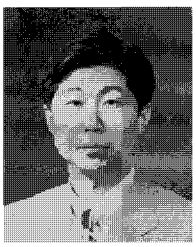


Eun Sei Park received the B.S. degree from Seoul National University, the M.S. degree from Korea Advanced Institute of Science and Technology, and the Ph.D. degree from the University of Texas at Austin, Autin, Texas, USA. Currently, he is a research professor of BK21 TMS Information Technology Center at Yonsei University, Seoul, Korea. Previously, he has been involved in many academic and industrial positions including Hanyang University, VeraTest, Inc., Mentor Graphics, Inc., Magma Design Automation, Inc., ETRI, and Motorola, Inc in Korea and USA.

Dr. Park was a recipient of the Best Paper Award (Honorable Mention) from the 1988 IEEE International Test Conference. His research interest include testing, design-for-test, and CAD of VLSI systems.



Sungho Kang received the B.S. degree from Seoul National University, Seoul, Korea, and the M.S. and Ph.D. degrees in electrical and computer engineering from The University of Texas at Austin.

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