Short Channel Analytical Model for High Electron Mobility Transistor to Obtain Higher Cut-Off Frequency Maintaining the Reliability of the Device

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Abstract—A comprehensive short channel analytical model has been proposed for High Electron Mobility Transistor (HEMT) to obtain higher cut-off frequency maintaining the reliability of the device. The model has been proposed to consider generalized doping variation in the directions perpendicular to and along the channel. The effect of field plates and different gate-insulator geometry (T-gate, etc) have been considered by dividing the area between gate and the high band gap semiconductor into different regions along the channel having different insulator and metal combinations of different thicknesses and work function with the possibility that metal is in direct contact with the high band gap semiconductor. The variation obtained by gate-insulator geometry and field plates in the field and channel potential can be produced by varying doping concentration, metal workfunction and gate-stack structures along the channel. The results so obtained for normal device structure have been compared with previous proposed model and numerical method (finite difference method) to prove the validity of the model.

Index Terms—Gate-insulator geometries, field plate, gate-stack, retrograde doping, metal workfunction, cut-off frequency, breakdown voltage, hot-carrier effect, Field engineering, DIBL, threshold voltage.

I. INTRODUCTION

An InGaAs/InAlAs high electron mobility transistor (HEMT) on InP substrate has shown the excellent high speed characteristics due to the enhanced electron's mobility and the increased conduction band discontinuity. Ever since its introduction the challenges among the researchers are to increase the reliability of the device without finding the middle ground for the operating speed of the device. Several approaches have been proposed for MOSFET, MESFET, HEMT etc following different criterion for reliability, speed and their applications. Among them the most common approaches are variation of doping concentration, variation of metal workfunction, gate-stack variation and the variation of gate-insulator geometries or field plates engineering [1-33]. The T-gate geometry has generally been used for higher cut-off frequency performance due to the use of upper and lower gate electrode offering lower gate resistance and capacitance to the device [33-45]. The enhancement of these variations includes improved breakdown voltage, current voltage swing, linearity, efficiency, stability, reliability by suppressing phenomenon, namely surface traps effects, hot-carriers effects, current collapse, gate leakage, junction leakage, subthreshold leakage and DC-to-RF dispersion.

To study all these devices a generalized short channel model has been proposed in this paper considering doping variation in the directions perpendicular and along the channel, where region between gate and the high band gap semiconductor is divided into different regions along the channel having different insulator and metal combinations of different thicknesses and work

function considering the possibility that metal may be in direct contact with the high band gap semiconductor. From this model we have discuss L-gate, Γ-gate, T-gate, Inverse-T (IT) gate and normal recess gate structures. Similar variation in the field and channel potential can be produced by varying doping concentration, gate-stack variation and metal workfunction along the channel. The results so obtained for normal device structure have been compared with previous proposed model and numerical simulation (Finite Difference Method) to prove the validity of the model.

II. SHORT-CHANNEL THRESHOLD VOLTAGE MODEL

Fig. 1 shows the cross-sectional view of HEMT structure together with conduction band diagram for the case of mobile carriers. Basic HEMT structure used in the analysis consists of undoped InGaAs layer to form the 2DEG channel; an InAlAs Si-doped layer followed by gate-insulator geometry. The gate geometry is such that the portion between the gate and semiconductor is divided into m_l-regions along the channel having different insulator (ε_{Iz}) and metal combinations of different thicknesses (t_{Iz}) and work function (ϕ_b) considering the possibility that metal may be in direct contact with the high band gap semiconductor. Furthermore, the high band gap semiconductor has been divided into $m_l \times n_l$ regions having different doping concentration along the channel and to the depth of the semiconductor. To include the HEMT structure the raised potential (Δ) is considered at the heterointerface [47] and is given by

$$\Delta = \Delta E_c - k_1 \qquad (1)$$

in which, ΔE_c is the conduction band discontinuity and k_l is the subthreshold factor arises due to quantization of carriers at the heterointerface.

1. Two-dimensional Potential Analysis

Short-channel effects can be modeled by solving the two-dimensional potential distribution in the fully depleted InAlAs layer (Fig. 1) from the 2-D Poisson
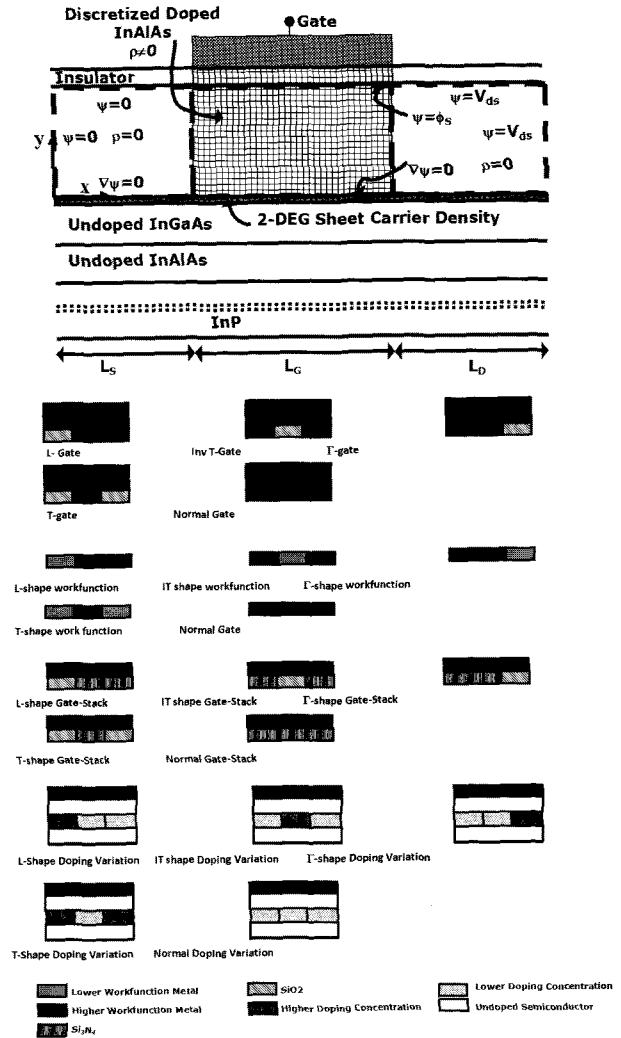

Fig. 1. Cross-sectional view of different Gate-Insulator Geometric Discretized doped High Electron Mobility Transistor along with various device structures showing variation of gate-insulator geometry, doping variation, gate-stack variation and work function variations.

equation, written as

$$\nabla^2 \Psi(x,y) = \frac{-\rho(x,y)}{\varepsilon_o \varepsilon_S} \qquad (2)$$

and is subjected to the following boundary conditions

$$\psi(0,y)=0, \psi(x,d_T)=0, \frac{\partial\psi(x,y)}{\partial y}\bigg|_{y=0} \qquad \vee \qquad 0 \le x \le L_S$$

$$\frac{\partial\psi(x,y)}{\partial y}\bigg|_{y=0}=0, \psi(x,d)=\phi_s\big|_p \qquad \vee \qquad L_S \le x \le L_S + \sum_0^{m_l} L_G\big|_i$$

$$\psi(L,y)=V_{DS}, \frac{\partial\psi(x,y)}{\partial y}\bigg|_{y=0}=0, \psi(x,d_T)=V_{DS} \quad \vee \quad L_S + \sum_0^{m_l} L_G\big|_i \le x \le L_S + \sum_0^{m_l} L_G\big|_i + L_D$$

$$(3)$$

in which ϕ_s is the surface potential at the oxide-semiconductor interface and is given by

$$\phi_s\big|_p = V_{GS} - \phi_{ms}\big|_p + V_I\big|_p$$

where $\phi_{ms}\big|_p$ is the workfunction difference between bulk semiconductor and the gate electrode, $V_I\big|_p \left(= \frac{qt_I}{\varepsilon_o\varepsilon_I}\left(\sum_{i=1}^{n_1-1}N_{p,i}d_i + N_q\left(d_T - \sum_{i=1}^{n_1-1}d_i\right)\right)\right)$ is the voltage drop across the insulator. ε_S and ε_I is the dielectric permittivity of *InAlAs* and insulator; V_{GS} and V_{DS} is the gate voltage and drain voltage; $\Psi(x, y)$ is the 2-D potential distribution and $\rho(x, y)$ is the charge density distribution given by

$$\rho_{p,q} = \begin{cases} 0 & \vee & 0 \le x \le L_S \\ qN_{p,q} & \vee & L_S \le x \le L_S + \sum_{i=1}^{p}L_G\big|_i \\ 0 & \vee & L_s + \sum_{i=1}^{p}L_G\big|_i \le x \le L_s + \sum_{i=1}^{p}L_G\big|_i + L_d \end{cases}$$

$$\vee \quad \sum_{j=1}^{q-1}d_j \le y \le \sum_{j=1}^{q}d_j \tag{4}$$

The solution of the 2-D Poisson's equation in a finite region can be obtained by means of Green's theorem [48].

$$\psi(x,y) = \int G(x,y,x',y')\cdot\frac{\rho(x',y')}{\varepsilon_o\varepsilon_S}.dv' + $$
$$\int\left[G(x,y,x',y')\cdot\frac{\partial\psi}{\partial n'} - \frac{\partial G}{\partial n'}.\psi(x',y')\right].ds' \tag{5}$$

where (x, y) and (x', y') denotes the field and source point coordinates, respectively; G is the Green's function and is given by

$$G(x,y,x',y') = \frac{2}{d_T}\cdot\sum_n \sin[k_n.(y-d_T)].\sin[k_n.(y'-d_T)].F_I(x,x',k_n)$$

$$G(x,y,x',y') = \frac{2}{L}\cdot\sum_m \sin(k_m.x).\sin(k_m.x').F_{II}(y,y',k_m) \tag{6}$$

where $F_I(x, x', k_n)$ and $F_{II}(y, y', k_m)$ are

$$F_I(y,y',k_n) = \begin{cases} \dfrac{\sinh(k_n.x).\sinh[k_n.(L-x')]}{k_n.\sinh(k_n.L)} & \vee & x < x' \\ \dfrac{\sinh(k_n.x').\sinh[k_n.(L-x)]}{k_n.\sinh(k_n.L)} & \vee & x > x' \end{cases}$$

$$F_{II}(y,y',k_m) = \begin{cases} \dfrac{\cosh(k_m.y).\sinh[k_m.(d_T-y')]}{k_m.\cosh(k_m.d_T)} & \vee & y < y' \\ \dfrac{\cosh(k_m.y').\sinh[k_m.(d_T-y)]}{k_m.\cosh(k_m.d_T)} & \vee & y > y' \end{cases} \tag{7}$$

$$k_n = \left(n-\frac{1}{2}\right).\frac{\pi}{d_T}, \ k_m = \frac{m.\pi}{L}, \ \text{where} \ L = L_s + \sum_{i=1}^{m_1}L_G\big|_i + L_d$$

and $d_T = \sum_{i=1}^{n_1}d_i$, n and m are integers and are greater than zero and. Substituting (7) into (5) and solving, we obtain

$$\psi(x,y) = \frac{2.q}{\varepsilon_o\varepsilon_S.L}\sum_m \sin(k_m.x).\sum_{k=1}^{m_1}\frac{\cos\left(k_m.\sum_{i=1}^{k-1}L_G\big|_i\right)-\cos\left(k_m.\sum_{i=1}^{k-1}L_G\big|_i\right)}{k_m}.\frac{d_T}{\int_0^{}}N_{k,j}.F_{II}dy'$$

$$+\frac{2}{L}\sum_m \frac{\sin(k_m.x).\cosh(k_m.y)}{\cosh(k_m.d)}.\int_0^{L}\psi(x',d_T).\sin(k_m.x').dx'$$

$$-\frac{2}{L}\sum_m \frac{\sin(k_m.x).\sinh[k_m.(d_T-y)]}{k_m.\cosh(k_m.d_T)}.\int_0^{L}\frac{\partial\psi(x',y')}{\partial y'}\bigg|_{y'=0}.\sin(k_m.x').dx'$$

$$+\frac{2}{d_T}\sum_n \frac{\sin[k_n.(y-d_T)].\sinh[k_n.(L-x)]}{\sinh(k_n.L)}.\int_0^{d_T}\psi(0,y').\sin[k_n.(y'-d_T)].dy'$$

$$+\frac{2}{d_T}\sum_n \frac{\sin[k_n.(y-d_T)].\sinh(k_n.x)}{\sinh(k_n.L)}.\int_0^{d_T}\psi(L,y').\sin[k_n.(y'-d_T)].dy' \tag{8}$$

where $\psi(x', y')$ and $\dfrac{\partial\ \psi(x', y')}{\partial\ y'}$ represent the potential and normal electric field at the boundaries. The corresponding values of integrals are given in Appendix-*A*.

III. CUT-OFF FREQUENCY MODEL

Drain current in Region-z for linear region of device operation is given by [49-51]

$$I_{ds}\big|_z = \frac{Wq\mu_o}{C_z B_z^{\ 2}}\frac{(f[y(V_{1z})]-f[y(V_{0z})])}{\left(L_z + \frac{\mu_o(V_{1z}-V_{oz})}{v_{sat}}\right)} \tag{9}$$

where $z = 1$ to m_1 ($m_1 = 3$) and

$$y(V_z) = (\beta_z k_2)^2 + 4\beta_z (1 + \beta_z k_3)(V_{gs} - V_{off}|_z - k_1 - V_z - I_{ds} R_s)$$

in which $A_z = -\beta_z k_2$; $B_z = 2(1 + \beta_z k_3)$; $C_z = -4\beta_z(1 + \beta_z k_3)$ and the values of V_{1z} and V_{oz} for various regions are $(m_1 = 3)$

$V_{11} = V_1$ and $V_{01} = 0$(Region-I)

$V_{12} = V_2$ and $V_{02} = V_1$(Region-II)

$V_{13} = V_{ds} - I_{ds}(R_s + R_d)$ and $V_{03} = V_2$(Region-III)

$$(10)$$

$$\beta_z = \frac{\varepsilon_o.\varepsilon_S}{q\left(d_T + \frac{\varepsilon_S.t_{Iz}}{\varepsilon_{Iz}}\right)} \quad \text{and} \quad V_{off}|_z \text{ is the threshold}$$

voltage for Region-m_1 of planar doped structure and can be expressed as

$$V_{off}|_z = \phi_{ms} - \Delta E_c - \frac{q.N_D.d_a^{\,2}}{2.\varepsilon_o.\varepsilon_s}\left(1 + \frac{2.d_i}{d_a}\right) - \frac{q.N_D.t_{Iz}.d_a}{\varepsilon_o.\varepsilon_{Iz}} + k_1$$

$$(11)$$

For current continuity in these regions, current flowing through all the regions is same i.e.

$$I_{ds}|_1 = I_{ds}|_2 = I_{ds}|_3 = I_{ds} \qquad (12)$$

the expression of drain current for generalized gate geometry can be obtained by using (9), (10), (11) and (12). The variation can be considered by altering the doping concentration or dielectric constant of the insulator or thickness of the insulator (for gate insulator geometry) or workfunction of the metal in various regions.

Capacitance Model

The charge associated with the gate terminal in Region-z is given as

$$Q_g|_z = -Q_t|_z + qW \int_{L_{z-1}}^{L_z} n_s(x)|_z \, dx \qquad (13)$$

where x is any position along the channel relative to the source side $(x=0)$ and for pulsed doped structure $Q_t|_z = qWL_z N_D W$. As n_s is related to the channel potential so the integral in (13) is first transformed into

channel potential by using the expression of drain current

$$I_{ds} = qW \, n_s(x)|_z \, v_s$$

Now using the following velocity field relationship

$$v_s = \begin{cases} \dfrac{\mu_o E}{1 + \dfrac{E}{E_c}} & if \quad E \le E_c \\[4mm] \mu_o E_c & if \quad E \ge E_c \end{cases}$$

in the linear region

$$dx = \left(\frac{qWn_s\mu_o}{I_{ds}} - \frac{1}{E_c}\right)dV$$

and on solving, we get

$$Q_g|_z = -Q_t|_z + qW \int_{V_{z-1}}^{V_z} n_s(V)|_z \left(\frac{qW\,n_s(V)|_z\,\mu_o}{I_{ds}} - \frac{1}{E_c}\right)dV \qquad (14)$$

The corresponding gate-source capacitance is given by

$$C_{gs}|_z = \frac{-q^2 W^2 \mu_o}{I_{ds}^{\,2}} \frac{\partial I_{ds}}{\partial V_{gs}}\bigg|_{V_{gd}} \left(f_1[y(V_z)] - f_1[y(V_{z-1})]\right) -$$

$$C.f_2[y(V_z)].dy_g(V_z) + C.f_2[y(V_{z-1})].dy_g(V_{z-1}) \qquad (15)$$

Where

$$dy_g(V) = 1 - \frac{\partial V}{\partial V_{gs}}\bigg|_{V_{gd}} - R_s \frac{\partial I_{ds}}{\partial V_{gs}}\bigg|_{V_{gd}}$$

$$f_1(y) = \frac{1}{C_z B_z^{\,4}}\left(A_z^{\,4}y + \frac{8A_z^{\,3}y^{3/2}}{3} + 3A_z^{\,2}y^2 + \frac{8A_z y^{5/2}}{5} + \frac{y^3}{3}\right)$$

$$f_2(y) = \frac{qW\,n_s|_z}{C}\left(\frac{qW\,n_s|_z\,\mu_o}{I_{ds}} - \frac{1}{E_c}\right)$$

and gate-drain capacitance is given by

$$C_{gd}\Big|_z = \frac{-q^2 W^2 \mu_o}{I_{ds}^2} \frac{\partial I_{ds}}{\partial V_{gd}}\Big|_{V_{gs}} \left(f_1\left[y(V_z)\right] - f_1\left[y(V_{z-1})\right] \right) -$$

$$C.f_2\left[y(V_z)\right].dy(dV_z) + C.f_2\left[y(V_{z-1})\right].dy(dV_{z-1}) \tag{16}$$

Where

$$dy(dV) = -dV - g_m R_s$$

The resultant gate to source and gate-drain capacitance can be represented as series and parallel combination of insulator (C_{I1}, C_{I2} and C_{I3}) and depletion capacitances (C_{R1}, C_{R2} and C_{R3}) ($C_{gd}|_z$ and $C_{gs}|_z$) in various regions as shown in Fig. 2 and is simplified as

$$C_{gs}\Big|_T, C_{gd}\Big|_T = \frac{C_{I1}C_{R1}}{C_{I1}+C_{R1}} + \frac{C_{I2}C_{R2}}{C_{I2}+C_{R2}} + \frac{C_{I3}C_{R3}}{C_{I3}+C_{R3}} \tag{17}$$

in which $C_{Iz} = \dfrac{\varepsilon_o \varepsilon_{Iz}\left(L_z + {}^{t_{Iz}}\!/_2\right)W}{t_{Iz}}$ [] and C_{R1}, C_{R2} and

C_{R3} can be easily found by using (15), (16) and (17).

Cut-off frequency

The cut-off frequency of the device can be obtained by

$$f_T = \frac{g_m}{2\pi\left(C_{gs}\Big|_T + C_{gd}\Big|_T\right)} \tag{18}$$

where g_m is the transconductance of the device and can be calculated by differentiating (12) with respect to gate voltage at constant drain voltage.

III. RESULTS AND DISCUSSION

Different gate-insulator geometries, doping variation, gate-stack variation and using combination of metal gate electrode having different workfunction has widely been used for improving device performance and reliability of the device. To study all these devices a generalized short channel model has been proposed in this paper. From this model different gate-insulator geometry like L-gate, Γ-gate, T-gate, Inverse-T gate and normal recess gate structures (as shown in Fig. 1) has been discussed. Similar variation in the field and channel potential can be produced by varying doping concentration, metal workfunction along the channel and gate-stack variation
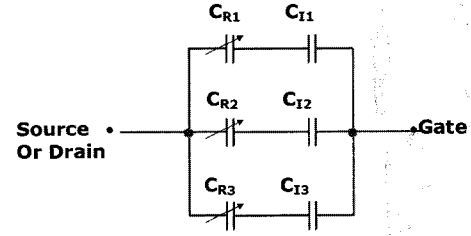

Fig. 2. Equivalent capacitance model for different gate insulator geometries.

Table 1. Value of parameters used in the analysis

Parameters	Value	Parameters	Value
d_1	20 Å	t_I	t_I, Variable
d_2	100 Å	ϕ_b	ϕ_b, Variable
d_3	100 Å	ε	ε_I, Variable
N_1	Undoped	ϕ_b [Low]	0.2 eV
N_2	N_d, Variable	ϕ_b [High]	0.4 eV
N_3	Undoped	ε_I [Low]	3.9 [SiO$_2$]
N_d [High]	3×10^{24} m^{-3}	ε_I [High]	7.5 [Si$_3$N$_4$]
N_d [Low]	2×10^{24} m^{-3}	t_I[Low]	Zero
L_g	0.25μm	t_I [High]	200 Å
μ_o	1 m^2/V-sec	v_{sat}	3.2×10^5 m/sec
R_s	0.3 Ω	R_d	1 Ω
W	50 μm		

along the channel. All these structure have been compared at constant upper gate length divided into three equal regions (m_I=3) to produce various gate geometries as shown in Fig. 1 and pulsed doped structure (n_I=3) has been considered. The parameters used for the analysis are tabulated in Table.1.

The DIBL effect and variation of threshold voltage have been studied for gate-insulator geometries through Fig. 3. The variation of channel potential with normalized distance along the channel for various gate-insulator geometries (N-Gate, L-gate, Γ-gate, T-gate and IT-gate) for two different channel length (0.1μm and 0.25μm) and drain voltages (0V and 2.0V) have been plotted in Fig. 3. Similar variation has been found for gate-stack variation, doping concentration variation and metal workfunction variation. All these variation have been compared with numerical simulation (Finite Difference Method) under similar boundary conditions to prove the validity of our model. The results so obtained from the numerical simulation and from the analysis are found in excellent agreement with each other. Comparing the results of minimum channel potential for 0.1μm and 0.25μm gate length from Fig. 3 (a & b) for normal gate structure, it is found that the
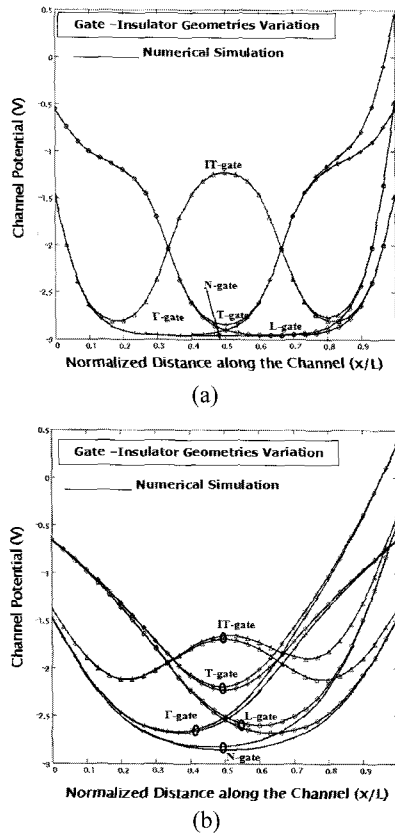
(a)

(b)

Fig. 3. Variation of channel potential with normalized distance along the channel for various gate-insulator geometries (N-Gate, L-gate, Γ-gate, T-gate and IT-gate) for two different channel length (0.1μm and 0.25μm) and drain voltages (0V and 2.0V).

device having gate length of 0.1μm (L/d =4.545) have DIBL effects whereas it is completely missing in device with gate length of 0.25μm (L/d =11.364). It can also be seen from Fig .3 (a) that device having gate-insulator geometry of IT-gate or T-gate have raised minimum potential for gate length of 0.25μm thereby increasing the threshold voltage of the device even at zero drain bias. Figure also shows that these devices have no variation with drain voltage. So we can say that these devices do not suffer from DIBL effects but have threshold voltage increment in the case for 2D analysis as compared to 1D analysis. Increasing the length of the device completely eliminated this effect. Thus we can say that using geometries like IT-gate and T-gate increases the L/d ratio for correct estimation of threshold voltage from 1D analysis. Decreasing the gate length to 0.1μm increases this effect (Fig. 3(b)). Furthermore, this effect can also be seen in the case of L-gate and Γ-gate geometries. Figure also shows that the
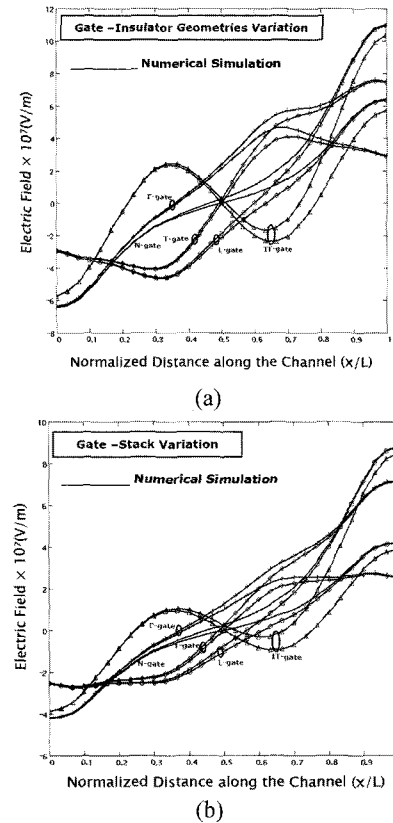

(a)

(b)

Fig. 4. (a)Variation of Electric Field with normalized distance along the channel for various gate-insulator geometries (N-Gate, L-gate, Γ-gate, T-gate and IT-gate) for channel length of 0.1μm and drain voltages (0V and 2.0V).

Γ-gate structure has reduced DIBL effects in comparison to normal gate structure; T-gate has also reduced DIBL effect but not more in comparison to Γ-gate; IT-gate has completely eliminated this effect; L-gate has increased DIBL effect in comparison to normal gate structure. But in all the cases, minimum channel potential is found to be raised in comparison to normal gate structure even at zero drain bias and has different value of threshold voltage predicted from 1D analysis and 2D analysis.

The influence of these variations on hot-carriers effects has been discussed in Fig. 4 where variation of electric field has been plotted under the gate with normalized distance along the channel. The maximum value of electric field can be seen at the edges of the gate electrode for normal gate structure for zero drain voltage. With the increase in drain voltage the maximum value of electric field increases at the drain edge keeping constant value at the source end. The maximum value of electric field in the channel depends on the field at the surface and the doping concentration

of the device leading to this channel, whereas the field at the surface depends on the doping concentration at the surface, thickness and properties of the insulator and metal workfunction. Electric field at the source end depends on the gate voltage of the device and has no influence of drain voltage. So for designing the device for higher ON-state breakdown voltage engineering at drain end is necessary, whereas for designing the device for higher OFF-state breakdown voltage designing at both the ends are necessary. The variation of electric field for L-gate geometry clearly shows the decrease in electric field at the source end but have same value at drain end in comparison to the normal gate structure. The Γ-gate geometry shows the decrease in the maximum value of electric field at the drain end in comparison to the normal gate structure. T-gate structure shows decrease in the maximum electric field at both source and drain end. Inverse T-gate also shows the decrease in maximum value of electric field at both the ends but lesser in comparison to T-gate and Γ-gate and only at shorter gate length. Increasing the gate length gives overlapped electric field characteristics with normal gate structures. Thus T-gate and Γ-gate are only geometries useful for decreasing the hot carriers effects. T-gate can be used for enhancing the characteristics for both ON-state and OFF-state conditions whereas Γ-gate can only be used for enhancing the characteristics for ON-state conditions. Similar effects can be seen from the variation of gate-stack [Fig. 4(b)] or by variation of metal workfunction or doping concentration variation for L-shape, Γ-shape, T-shape and IT-shape profile. The only difference in characteristics is that doping concentration variation affects the field upto the channel, whereas gate-insulator geometry, gate-stack variation and metal workfunction affected the surface of the semiconductor and the effect will be passing on to the channel. Further enhancement in the characteristics can be expected by choosing combination of gate-insulator variation with gate-stack variation or metal workfunction variation or doping concentration variation or combination of all depending on the choice of other parameters.

The influence of these variations on speed of the device has been discussed in Fig. 4 where variation of cut-off frequency, gate capacitance and transconductance has been plotted with gate voltage. Increasing the doping
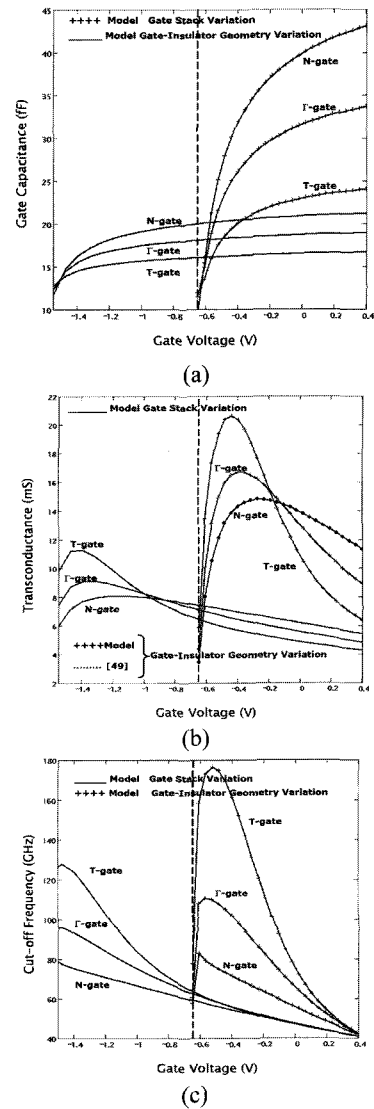

(a)

(b)

(c)

Fig. 5. (a) Variation of Gate Capacitance with gate voltage for various Gate-insulator geometries and Gate-stack (N-Gate, Γ-gate and T-gate) for channel length of 0.25μm. (b) Variation of Transconductance with gate voltage for various Gate-insulator geometries and Gate-stack (N-Gate, Γ-gate and T-gate) for channel length of 0.25μm. (c). Variation of Cut-off Frequency with gate voltage for various Gate-insulator geometries and Gate-stack (N-Gate, Γ-gate and T-gate) for channel length of 0.25μm.

concentration at the drain end at Metal-semiconductor interface, decreases the field at the surface of the semiconductor but eventually decrease the mobility of the device in the enhancement mode device as channel is formed at the surface of the semiconductor. Whereas in the buried channel device or HEMT device the surface doping has negligible influence on mobility but have same influence of the electric field in the channel. But even ignoring the effect of mobility variation in the

semiconductor such variation will not give rise to enhance characteristics as it increases the gate-capacitance of the device with transconductance, which will lead to same value of cut-off frequency. The depth of the doping causes the increase in transconductance and gate-capacitance in the same proportion with the increased effect of mobility degradation (for non heterostructure devices). Similar effect can be seen by comparing the characteristics of metal workfunction variation except for the effect of mobility degradation. But due to insulator capacitance in series with semiconductor capacitance, as in the case of gate-insulator geometries and gate-stack variation, causes decrease in the equivalent gate capacitance of the device with increased transconductance, which will lead to increased cut-off frequency. So gate-insulator geometries and gate-stack variation is the more useful variation as far as speed of the device is concerned and has been analyzed through Fig. 5. The maximum values of cut-off frequency obtained from the analysis are 176GHz, 111GHz and 82GHz for T-gate-insulator geometry, Γ-gate-insulator geometry and Normal-gate geometry HEMT respectively whereas 127GHz, 96GHz and 81GHz for T-shape gate-stack, Γ- shape gate-stack and Normal-gate-stack MISHEMT.

IV. CONCLUSIONS

A comprehensive short channel analytical model has been proposed in this paper considering device having generalized doping variation in both directions with the channel, where area between gate and the high band gap semiconductor is divided into different regions along the channel having different insulator and metal combinations of different thicknesses and work function considering the possibility that metal may be in direct contact with the high band gap semiconductor. From this model we have discuss L-gate, Γ-gate, T-gate, Inverse-T gate and normal recess gate structures to obtain higher cut-off frequency maintaining the reliability of the device for same channel length. Similar variation in the field and channel potential can be produced by varying doping concentration, metal workfunction and gate-stack structures along the channel. The results so obtained for normal device structure have been compared with previous proposed

model and numerical method (finite difference method) to prove the validity of the model. From the analysis it is found that such variations suppress the DIBL effect but eventually raises the minimum channel potential in comparison to normal gate structure even at zero drain voltage thereby increasing the threshold voltage of whole device in comparison to 1D threshold voltage of the device, thus creating the need of 2D analysis. Γ-gate variation is useful for enhancing the ON-state breakdown voltage, whereas T-gate is useful for enhancing both the ON-state and OFF-state breakdown voltage of the device. Doping variation affects the device from surface of the semiconductor to the channel whereas the gate-insulator variation or the gate-stack variation or the metal workfunction variation only affect the surface of the semiconductor and the effect have been passed on to the channel. Gate-stack variation and gate-insulator geometry variation increases the cut-off frequency of the device by decreasing the gate-capacitance and increasing the transconductance of the device whereas for metal workfunction variation and doping concentration variation the value of cut-off frequency is found to be the same or lesser in comparison to normal structure.

ACKNOWLEDGMENTS

APPENDIX A

$$\int_0^{d_T} N_{k,j}.F_{II}.dy' = \frac{\sinh\left[k_m\left(d_T-y\right)\right]}{k_m.\cosh\left(k_m.d_T\right)} \cdot \left\{ \sum_{j_i=1}^{i-1} N_{k,j} \left[\frac{\sinh\left(k_m\sum_{i=1}^{j_i-1}d_i\right)-\sinh\left(k_m\sum_{i=1}^{j_i}d_i\right)}{k_m} \right] \right.$$

$$+ N_{k,j}\left[\frac{\sinh(k_m.y)-\sinh\left(k_m\sum_{i=1}^{i-1}d_i\right)}{k_m}\right]\right\} - \frac{\cosh(k_m.y)}{k_m.\cosh(k_m.d_T)}\cdot\left\{\frac{N_{k,j}}{k_m}\left[\cosh\left(k_m\left(d_T-\sum_{i=1}^{j}d_i\right)\right)\right]\right.$$

$$-\cosh\left[k_m\left(d_T-y\right)\right]\right] - \sum_{j_i=1}^{n-1}N_{k,j_i+1}\cdot\left[\frac{\cosh\left(k_m\left(d_T-\sum_{i=1}^{j_i-1}d_i\right)\right)-\cosh\left(k_m\left(d_T-\sum_{i=1}^{j_i}d_i\right)\right)}{k_m}\right]\right\}$$

$$\vee \quad \sum_{i=1}^{l-1} d_i \le y \le \sum_{i=1}^{l} d_i \tag{A-1}$$

$$\int_0^L \psi(x',0).\sin(k_m.x').dx' = \sum_{b=1}^{ml} \phi_s\big|_b . \left[\frac{\cos\left(k_m \sum_{i=1}^{b-1} Ll_i\right) - \cos\left(k_m \sum_{i=1}^{b} Ll_i\right)}{k_m} \right]$$

$$V_{DS} \left[\frac{\cos\left(k_m\left(L_S + \sum_{i=1}^{m_1} L_G\big|_i\right)\right) - \cos\left(k_m\left(L_S + \sum_{i=1}^{m_1} L_G\big|_i + L_D\right)\right)}{k_m} \right] \tag{A-2}$$

$$\int_0^L \frac{\partial \psi(x',y')}{\partial y'}\bigg|_{y'=0} .\sin(k_m.x').dx' = 0 = \int_0^{d_T} \psi(0,y').\sin\big[k_n.(y'-d_T)\big].dy' \tag{A-3}$$

$$\int_0^{d_T} \psi(L,y').\sin\big[k_n.(y'-d_T)\big].dy' = -\frac{V_{ds}}{k_n} \tag{A-4}$$

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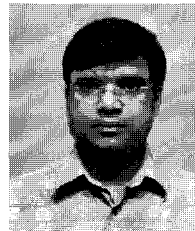
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