Analytical Characterization of a Dual-Material Double-Gate Fully-Depleted SOI MOSFET with Pearson-IV type Doping Distribution

Alok Kushwaha*, Manoj K. Pandey*, Sujata Pandey*, and Anil K. Gupta**

Abstract—**A new two-dimensional analytical model for dual-material double-gate fully-depleted SOI MOSFET with Pearson-IV type Doping Distribution is presented. An investigation of electrical MOSFET parameters i.e. drain current, transconductance, channel resistance and device capacitance in DM DG FD SOI MOSFET is carried out with Pearson-IV type doping distribution as it is essential to establish proper profiles to get the optimum performance of the device. These parameters are categorically derived keeping view of potential at the center (ϕ_c) of the double gate SOI MOSFET as it is more sensitive than the potential at the surface (ϕ_s). The proposed structure is such that the work function of the gate material (both sides) near the source is higher than the one near the drain. This work demonstrates the benefits of high performance proposed structure over their single material gate counterparts. The results predicted by the model are compared with those obtained by 2D device simulator ATLAS to verify the accuracy of the proposed model.**

Index Terms—**Double Gate (DG), Dual Material (DM), Fully Depleted (FD), Radio Frequency (RF), Silicon-on-Insulator (SOI), Short Channel Effects (SCEs)**

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I. INTRODUCTION

Silicon-on Insulator (SOI) MOS devices are given much attention owing to their advantage of higher circuit speed, greater immunity to radiation induced errors, lower power consumption, attenuated short channel effects and compatibility with existing IC fabrication process [1]-[2]. The understanding and the optimization of the electrical properties of SOI MOSFET's necessitate the development of reliable analytical models.

It has been demonstrated that the dual gate (DG) SOI MOSFET structure is an effective means to overcome the short channel effects, due to the screening of the drain voltage by the second gate (step function profile) but does not improve the electron transport efficiency [3]-[6]. Gate transport efficiency is related to the average electron transport velocity traveling through the channel which is further related to the electric field distribution along the channel. In a MOSFET, electrons enter into the channel initially with a low velocity and gradually accelerated towards the drain. The electrons move fast in the region near drain but comparatively slow in the region near the source. Therefore, the performance of the device is affected by a relatively slow electron drift velocity in the channel near the source.

The RF performance of the MOSFET depends greatly on impurity profile (lightly doped), especially in the conducting region. The simplicity of the calculation justifies the use of symmetric Gaussian distribution although is accurate to first order only [7]. However, the exact distribution is highly asymmetric having large tailing effect near the surface. To overcome this problem along with back surface leakage [8], we considered the doping profile as Pearson-IV distribution which is based on four moments approach and match exactly well with

the actual distribution.

Yan et al. [9] assumed that the punch-through current flows along the surface, which is invalid for a double-gate SOI MOSFET for the following reasons. The maximum potential at the SOI MOSFET center, ϕ_c, is more sensitive to gate length than that at the surface, ϕ_s. Furthermore, the absolute value of ϕ_c is different than that of ϕ_s [10], meaning that the punch-through current dominantly flows at the SOI center.

Some models have been previously established for the DM DG SOI MOSFET but do not considered the exact doping distribution and the concept of potential at the center [11]-[12].In this paper a new structure called a dual material double gate fully depleted SOI MOSFET with Pearson-IV type doping distribution is proposed to circumvent the above mentioned problems (i.e. gate transport efficiency and exact doping distribution). The proposed structure has two metals in the gate (both side) M1 and M2 with different work functions. Here, the work function of metal gate M1 is greater than the work function of metal gate M2 for n-channel MOSFET and vice-versa for a p-channel MOSFET. In this structure, the peak electric field at the drain side is reduced, which ensures that the average electric field under the gate is increased that shows greater control of gate over the conductance of the channel so as to increase the gate transport efficiency. The RF performance of MOSFET, fabricated by ion-implantation, depends on the carrier concentration profiles as a function of depth into the active layer. Optimum performance of the device is achieved by considering the Pearson-IV type doping distribution.

Since ϕ_c should be relevant to the punch-through current, we obtained the relation between ϕ_s and ϕ_c. All other parameters are also derived by considering the potential at the center (ϕ_c) as well as surface potential (ϕ_s).

A 2-D analytical model using Poisson's equation has been presented for the drain current leading to the transconductance and channel resistance for the Pearson-IV type doping distribution based DM DG FD SOI MOSFET. Along with this, the device capacitance is also discussed. The accuracy of the model is verified by comparing its results with the simulation results using the device simulator ATLAS.

II. Model Formulation

1. Analytical Model for Drain Current

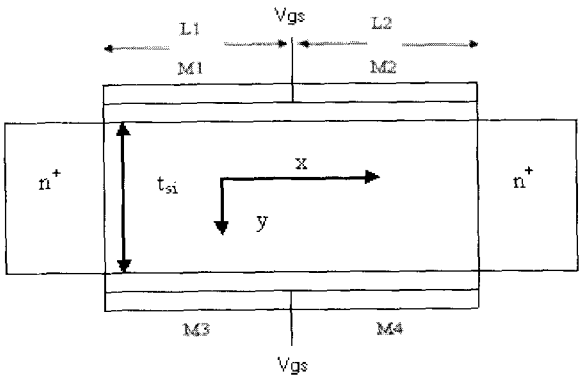

Fig.1. Cross-sectional view of DM DG FD SOI MOSFET.

Fig.1. shows the cross-sectional view of the Pearson-IV DM DG FD SOI MOSFET. The front gate consists of dual materials M1 and M2 of length L_1 and L_2. The back gate consists of dual materials M3 (= M1) and M4 (= M2) of length L_1 and L_2. Neglecting the fixed oxide charges effect, for a strongly inverted n-type double gate SOI MOSFET the current [13] in the channel $(L_g = L_1 + L_2)$ is given by

$$I_{DS1} = W.\mu_{n1}(x).Q_{n1}(x).\frac{d\phi_{C1}(x)}{dx}; \quad \text{for} \quad 0 \le x \le L_1 \qquad (1)$$

and

$$I_{DS2} = W.\mu_{n2}(x).Q_{n2}(x).\frac{d\phi_{C2}(x)}{dx}; \quad \text{for} \quad L_1 \le x \le L_g \qquad (2)$$

Where I_{DS1} is current under $M1$ & $M3$ for $0 \le x \le L_1$ and I_{DS2} is the current under $M2$ & $M4$ for $L_1 \le x \le L_g$ controlled from the front gate as well as the back gate. Both are then combined for the final drain current, i.e. I_{DS} for complete channel length, L_g. W is the channel width, $\mu_{n1}(x)$ and $\mu_{n2}(x)$ are the mobilities of electrons [13]-[14] for $0 \le x \le L_1$ and $L_1 \le x \le L_g$, given by

$$\mu_{n1}(x) = \frac{\mu_{no}}{\sqrt{1 + \left\{\frac{E_1(x)}{E_c}\right\}^2}}$$

and

$$\mu_{n2}(x)=\frac{\mu_{no}}{\sqrt{1+\left\{\frac{E_2(x)}{E_c}\right\}^2}}$$

where μ_{no} is the low field mobility[15], E_c is the critical field and $E_1(x)$ & $E_2(x)$ [14] are the fields given by

$$E_c = 6.01\times 10^2 T^{3/2};\ E_1(x)=\frac{C_{OX}.\{V_{Fb12}-V_{GS}+\phi_{C1}(x)\}}{\varepsilon_{SI}}$$

$$\& \ E_2(x)=\frac{C_{OX}.\{V_{Fb22}-V_{GS}+\phi_{C2}(x)\}}{\varepsilon_{SI}}$$

Here V_{Fb12} and V_{Fb22} are flatband voltages [16], $\phi_{C1}(x)$ and $\phi_{C2}(x)$ are the potential at the center of the channel, developed because of different material M1 (=M3) and M2 (=M4) under the front (and back) gate. These are related to surface potentials, $\phi_{S1}(x)$ and $\phi_{S2}(x)$ through [16]

$$\phi_{S1}(x)=\frac{1}{1+\frac{\varepsilon_{ox}.t_{si}}{4.\varepsilon_{si}.t_{ox1}}}\left\{\phi_{C1}(x)+\frac{\varepsilon_{ox}.t_{si}.V'_{GS11}}{4.\varepsilon_{si}.t_{ox1}}\right\}$$

$$\Rightarrow \frac{d\phi_{C1}(x)}{dx}=(1+A_1).\frac{d\phi_{S1}(x)}{dx}$$

$$\phi_{S2}(x)=\frac{1}{1+\frac{\varepsilon_{ox}.t_{si}}{4.\varepsilon_{si}.t_{ox1}}}\left\{\phi_{C2}(x)+\frac{\varepsilon_{ox}.t_{si}.V'_{GS22}}{4.\varepsilon_{si}.t_{ox1}}\right\}$$

$$\Rightarrow \frac{d\phi_{C2}(x)}{dx}=(1+A_1).\frac{d\phi_{S2}(x)}{dx},$$

where $A_1=\frac{\varepsilon_{ox}.t_{si}}{4.\varepsilon_{si}.t_{ox1}}$,

The surface potentials equations [16] in case of the Pearson-IV DM DG FD SOI MOSFET after solving for Poisson's equation under certain boundary conditions [16] are given as

$$\phi_{S1}(x)=\frac{1}{1+A_1}\left[\begin{array}{l}\{(1+A_1)V'_{GS1}\}-\frac{q.N_a\left(\frac{t_{si}}{2}\right)}{\varepsilon_{si}}\lambda^2+\\ A1_{11}.\exp\left(\frac{x}{\lambda}\right)+B1_{11}.\exp\left(\frac{-x}{\lambda}\right)\end{array}\right]$$

for $0\le x\le L_1$ under M1

$$\phi_{S2}(x)=\frac{1}{1+A_1}\left[\begin{array}{l}\{(1+A_1)V'_{GS2}\}-\frac{q.N_a\left(\frac{t_{si}}{2}\right)}{\varepsilon_{si}}\lambda^2+\\ A2_{22}.\exp\left\{\frac{(x-L_1)}{\lambda}\right\}+B2_{22}.\exp\left\{\frac{-(x-L_1)}{\lambda}\right\}\end{array}\right]$$

for $L_1\le x\le L_1+L_2$ under M2

Also the potential at the center [16] of the channel is given by

$$\phi_{c1}(x)=\{(1+A_1)V'_{GS1}-A_1.V'_{GS11}\}-\frac{q.N_a\left(\frac{t_{si}}{2}\right)}{\varepsilon_{si}}\lambda^2+$$
$$A_{11}.\exp\left(\frac{x}{\lambda}\right)+B_{11}.\exp\left(\frac{-x}{\lambda}\right)$$

for $0\le x\le L_1$ under M1

$$\phi_{c2}(x)=\{(1+A_1)V'_{GS2}-A_1.V'_{GS22}\}-\frac{q.N_a\left(\frac{t_{si}}{2}\right)}{\varepsilon_{si}}\lambda^2+$$
$$A_{22}.\exp\left\{\frac{(x-L_1)}{\lambda}\right\}+B_{22}.\exp\left\{\frac{-(x-L_1)}{\lambda}\right\}$$

for $L_1\le x\le L_1+L_2$ under M2

The comparison between potentials at the center and surface is shown in Fig. 2.

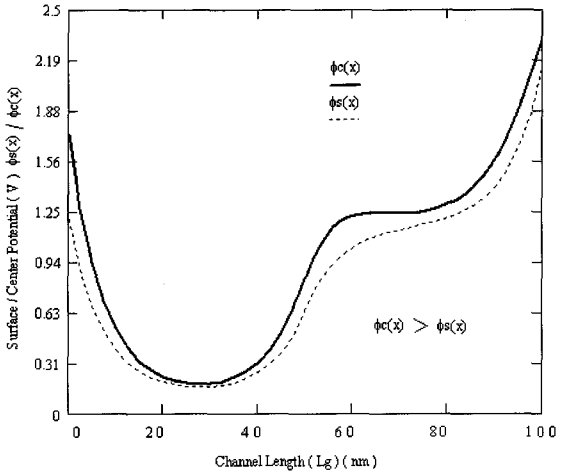

Fig.2. Surface and center potential profiles of Pearson-IV DM DG FD SOI MOSFETs. Other parameters are $V_{DS}=0.75V$, $\phi_{M1}=5V$, $\phi_{M2}=4.17\,V$, $t_{SI}=12\,nm$, $t_{oxf}=t_{oxb}=2\,nm$, $V_{GS}=0.15V$, $L_1=L_2=50\,nm$.

In the above expression for surface potential, $N_a\left(\frac{t_{si}}{2}\right)$ is the Pearson-IV type doping distribution [12] dependent on the silicon film thickness t_{si}. In the current equations (1) and (2), inversion layer charges are given by

$$Q_{n1}(x)=2.\{Q_{S1}(x)-Q_{D1}\} \tag{3}$$

for $0 \le x \le L_1$ under M1

and $Q_{n2}(x)=2.\{Q_{S2}(x)-Q_{D2}\}$ (4)

for $L_1 \le x \le L_1+L_2$ under M2

Here inversion layer charges are double as contributed through both sides, $Q_{S1}(x)$, $Q_{S2}(x)$ and Q_{D1}, Q_{D2} are the surface charges and depletion layer charges respectively, given by [17]

$$Q_{S1}(x)=-C_{OX}.\{V_{GS}-V_{FB12}-\phi_{C1}(x)\} \tag{5}$$

for $0 \le x \le L_1$ under M1 and

$$Q_{S2}(x)=-C_{OX}.\{V_{GS}-V_{FB22}-\phi_{C2}(x)\} \tag{6}$$

for $L_1 \le x \le L_1+L_2$ under M2

IIIy, $Q_{D1}=C_{OX}.(V_{FB12}-V_{TH}+\phi_F)$ (7)

and $Q_{D2}=C_{OX}.(V_{FB22}-V_{TH}+\phi_F)$ (8)

Substituting the values of $Q_S(x)$ and Q_D from (5)-(8) into (3)-(4) and integrating (1) and (2), by taking limits V_{bi} and $V_{bi}+V_{DS}$, the final expression for I_{DS1} and I_{DS2} is given by

$$I_{DS1}=\frac{2.W.\mu_{no}.C_{OX}}{L_1.(d_3)^{\frac{3}{2}}}\times(1+A_1)\times \left\{(d_2+d_4).\ln\left(\frac{c_1+c_2}{c_{11}+c_{22}}\right)-c_2+c_{22}\right\}$$

for $0 \le x \le L_1$

Where $d_2=V_{GS}-V_{TH}+\phi_F$, $d_4=V_{FB12}-V_{GS}$

$$d_3=\frac{1.02\times10^{-13}.C_{OX}}{(\varepsilon_{SI})^2},\quad c_1=\left\{d_3.d_4+d_3.\left(V_{bi}+\frac{V_{DS}}{2}\right)\right\},$$

$$c_2=\sqrt{1+d_3.(d_4)^2+2.d_3.d_4.\left(V_{bi}+\frac{V_{DS}}{2}\right)+d_3.\left(V_{bi}+\frac{V_{DS}}{2}\right)^2}\times\sqrt{d_3}$$

$$c_{11}=\{d_3.d_4+d_3.(V_{bi})\}$$

$$c_{22}=\sqrt{1+d_3.(d_4)^2+2.d_3.d_4.(V_{bi})+d_3.(V_{bi})^2}\times\sqrt{d_3}$$

and

$$I_{DS2}=\frac{2.W.\mu_{no}.C_{OX}}{L_2.(d_3)^{\frac{3}{2}}}\times(1+A_1)\times \left\{(d_2+d'_4)\ln\left(\frac{c'_1+c'_2}{c'_{11}+c'_{22}}\right)-c'_2+c'_{22}\right\}$$

for $L_1 \le x \le L_1+L_2$

here $d'_4=V_{FB22}-V_{GS}$, $c'_{11}=\left\{d_3.d'_4+d_3.\left(V_{bi}+\frac{V_{DS}}{2}\right)\right\}$,

$$c'_{22}=\sqrt{1+d_3.(d'_4)^2+2.d_3.d'_4.\left(V_{bi}+\frac{V_{DS}}{2}\right)+d_3.\left(V_{bi}+\frac{V_{DS}}{2}\right)^2}\times\sqrt{d_3}$$

$$c'_1=\{d_3.d'_4+d_3.(V_{bi})\}$$

$$c'_2=\sqrt{1+d_3.(d'_4)^2+2.d_3.d'_4.(V_{bi}+V_{DS})+d_3.(V_{bi}+V_{DS})^2}\times\sqrt{d_3}$$

The drain to source current in n-channel of Pearson-IV DM DG FD SOI MOSFET is shown in Fig. 3.

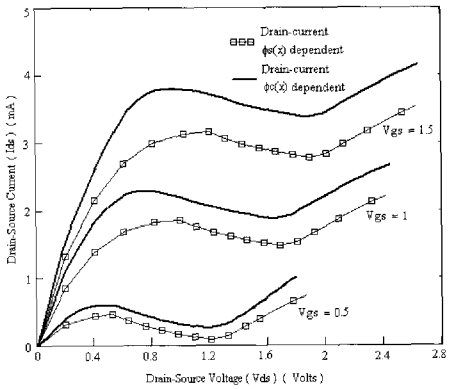

Fig. 3. Drain current based on different potential (i.e. surface and center) on various gate-source voltages for a channel length $L=100\,nm$. Other parameters are $t_{SI}=12nm$, $t_{oxf}=t_{oxb}=2nm$, $L_1=L_2=50nm$, $\phi_{M1}=5.25\,V$, $\phi_{M2}=4.17\,V$.

2. Transconductance

The transconductane of the channel of Pearson-IV DM DG FD SOI MOSFET is obtained by differentiating the drain current with respect to the gate voltage, Vgs and is given as

$$g_m = \left(\frac{dI_{DS}}{dVgs}\right)\Big|Vds = const.$$

As the drain current, I_{DS} is distributed into I_{DS1} and I_{DS2}, so is the g_m $(i.e. g_{m1} \text{ and } g_{m2})$. On solving g_{m1} for $0 \le x \le L_1$ and g_{m2} for $L_1 \le x \le L_1 + L_2$, we get

$$g_{m1} = \left(\frac{dI_{DS1}}{dVgs}\right)\Big|Vds = const.$$

$$g_{m1} = \frac{2.W.\mu_{no}.C_{OX}}{L_1.(d_3)^{\frac{3}{2}}} \times (1 + A_1) \times \left\{(d_2 + d_4).(c_{111}) + \left(\frac{c_1}{c_2} - \frac{c_{11}}{c_{22}}\right).\sqrt{d_3}\right\}$$

here,

$$c_{111} = \frac{\left(d_3 + \frac{\sqrt{d_3}.c_{11}}{c_{22}}\right).d_3}{c_{11} + c_{22}.\sqrt{d_3}} - \frac{\left(d_3 + \frac{\sqrt{d_3}.c_1}{c_2}\right).d_3}{c_1 + c_2.\sqrt{d_3}} \text{ and}$$

$$g_{m2} = \left(\frac{dI_{DS2}}{dVgs}\right)\Big|Vds = const.$$

$$g_{m2} = \frac{2.W.\mu_{no}.C_{OX}}{L_2.(d_3)^{\frac{3}{2}}} \times (1 + A_1) \times \left\{(d_2 + d'_4).(c_{222}) + \left(\frac{c'_1}{c'_2} - \frac{c'_{11}}{c'_{22}}\right).\sqrt{d_3}\right\}$$

here, $c_{222} = \dfrac{\left(d_3 + \frac{\sqrt{d_3}.c'_{11}}{c'_{22}}\right).d_3}{c'_{11} + c'_{22}.\sqrt{d_3}} - \dfrac{\left(d_3 + \frac{\sqrt{d_3}.c'_1}{c'_2}\right).d_3}{c'_1 + c'_2.\sqrt{d_3}}$

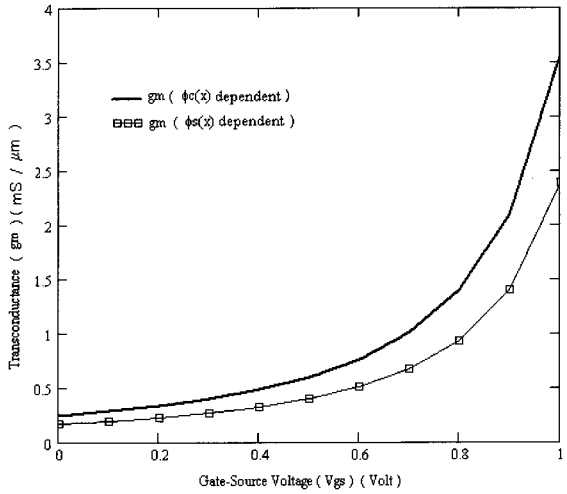

Fig. 4. Transconductance based on different potential (i.e. surface and center) . Other parameters are $L_1 = L_2 = 50\,nm$, $\phi_{M1} = 5.25V$, $\phi_{M2} = 4.17\,V$, $t_{SI} = 12\,nm$, $t_{oxf} = t_{oxb} = 2\,nm$, $V_{DS} = 1V$

The transconductance of Pearson-IV DM DG FD SOI MOSFET is shown in Fig. 4.

3. Channel Resistance

Channel resistance is important in the design of a high frequency, low-voltage devices. This can be obtained by inverse of the differentiation of the drain current with respect to drain voltage.

$$r_{ds} = \left(\frac{dI_{DS}}{dV_{DS}}\right)^{-1}\Big|Vgs = const.$$

On solving r_{ds1} for $0 \le x \le L_1$ and r_{ds2} for $L_1 \le x \le L_1 + L_2$, we get

$$r_{ds1} = \left(\frac{dI_{DS1}}{dV_{DS}}\right)^{-1}\Big|Vgs = const.$$

$$r_{ds1} = \left[\frac{2.W.\mu_{no}.C_{OX}}{L1.(d_3)^{\frac{3}{2}}} \times (1 + A_1) \times \left\{(d_2 + d_4).(c'_{111}) - \left(\frac{c_1}{2.c_2}\right).\sqrt{d_3}\right\}\right]^{-1}$$

here $c'_{111} = \dfrac{\left(\dfrac{d_3}{2} + \dfrac{\sqrt{d_3}.c_1}{c_2}\right).d_3}{c_1 + c_2.\sqrt{d_3}}$

$$r_{ds2} = \left(\frac{dI_{DS2}}{dV_{DS}}\right)^{-1}\Bigg|_{Vgs=const.}$$

$$r_{ds2} = \left[\frac{2.W.\mu_{no}.C_{OX}}{L2.(d_3)^{\frac{3}{2}}} \times (1+A_1) \times \left\{(d_2 + d'_4)(c'_{222}) + \left(\frac{c'_{11}}{2.c'_{22}} - \frac{c'_1}{2.c'_2}\right).\sqrt{d_3}\right\}\right]^{-1}$$

where

$$c'_{222} = \frac{\left(\dfrac{d_3}{2} + \dfrac{\sqrt{d_3}.c'_1}{2.c'_2}\right).d_3}{c'_1 + c'_2.\sqrt{d_3}} - \frac{\left(\dfrac{d_3}{2} + \dfrac{\sqrt{d_3}.c'_{11}}{2.c'_{22}}\right).d_3}{c'_{11} + c'_{22}.\sqrt{d_3}}$$

The channel resistance of Pearson-IV DM DG FD SOI MOSFET is shown in Fig. 5.

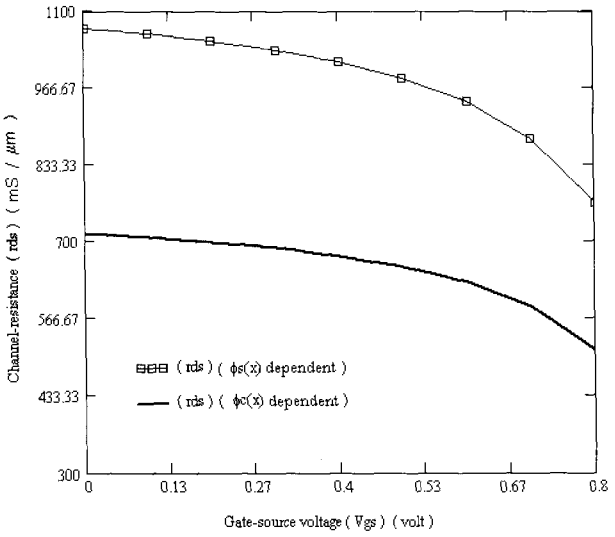

Fig. 5. Channel resistance based on different potential (i.e. surface and center) . Other parameters are $L_1 = L_2 = 50nm$, ϕ_{M1}=4.77V , ϕ_{M2} =4.17V , t_{SI} =12nm, $t_{oxf} = t_{oxb} = 2nm$, V_{DS} = 0.5V .

4. Device Capacitance

An equivalent circuit of a DM DG FD SOI MOSFET for its capacitance determination is shown in Fig. 6.

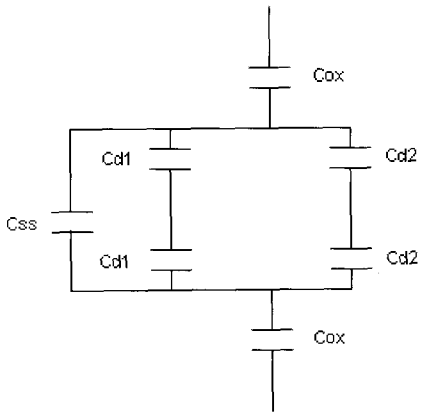

Fig. 6. Equivalent circuit of a DM DG FD SOI MOSFET.

The depletion charge [17] in double gate SOI MOSFET is given by $Q_{d1} = \sqrt{2.q.N_a\left(\frac{t_{SI}}{2}\right).\varepsilon_{SI}}.\sqrt{\phi_{C1}(x)}$

for $0 \le x \le L_1$ and

$$Q_{d2} = \sqrt{2.q.N_a\left(\frac{t_{SI}}{2}\right).\varepsilon_{SI}}.\sqrt{\phi_{C2}(x)}$$

for $L_1 \le x \le L_1 + L_2$

The depletion layer capacitance is differentiation of Q_{d1} and Q_{d2} with respect to V_{GS}. Therefore

$$C_{d1} = \frac{dQ_{d1}}{dVgs} = \sqrt{\frac{q.N_a\left(\frac{t_{SI}}{2}\right).\varepsilon_{SI}}{2.\phi_{C1}(x)}}.\frac{d\phi_{C1}(x)}{dVgs}$$

$$= \sqrt{\frac{q.N_a\left(\frac{t_{SI}}{2}\right).\varepsilon_{SI}}{2.\phi_{C1}(x)}} \times (1+A1) \times \frac{d\phi_{S1}(x)}{dVgs};$$

and

$$C_{d2} = \frac{dQ_{d2}}{dVgs} = \sqrt{\frac{q.N_a\left(\frac{t_{SI}}{2}\right).\varepsilon_{SI}}{2.\phi_{C2}(x)}}.\frac{d\phi_{C2}(x)}{dVgs}$$

$$= \sqrt{\frac{q.N_a\left(\frac{t_{SI}}{2}\right).\varepsilon_{SI}}{2.\phi_{C2}(x)}} \times (1+A1) \times \frac{d\phi_{S2}(x)}{dVgs};$$ where

$$\frac{d\phi_{S1}(x)}{dVgs} = 1+\frac{E_2-E_3}{E_1}.\exp\left(\frac{x}{\lambda}\right)+\frac{E_3-E_5}{E_1}.\exp\left(-\frac{x}{\lambda}\right)$$

for $0 \le x \le L_1$ and

$$\frac{d\phi_{S2}(x)}{dVgs} = 1+\frac{E_2-E_3}{E_1}.\exp\left(\frac{x-L_1}{\lambda}\right)+\frac{E_3-E_5}{E_1}.\exp\left(-\frac{(x)-L_1}{\lambda}\right)$$

for $L_1 \le x \le L_1+L_2$

here $E1=\exp\left(\frac{Lg+L_2}{\lambda}\right)-\exp\left(\frac{-Lg+L_2}{\lambda}\right)$;

$E2=\exp\left(\frac{-Lg+L_2}{\lambda}\right)$; $E3=\exp\left(\frac{Lg-L_1}{\lambda}\right)$;

$E5=\exp\left(\frac{Lg+L_2}{\lambda}\right)$

Total capacitance from the equivalent circuit is given by

$$C_T=\frac{C_{OX}.(C_{DP}+C_{SS})}{C_{OX}+2.(C_{DP}+C_{SS})};$$

where $C_{DP}=\frac{C_{D1}}{2}+\frac{C_{D2}}{2}$

and the interface capacitance C_{SS} is given by $C_{SS}=q.N_{SS}$, where N_{SS} is the interface state density The depletion layer capacitance of Pearson-IV DM DG FD SOI MOSFET is shown in Fig. 7.

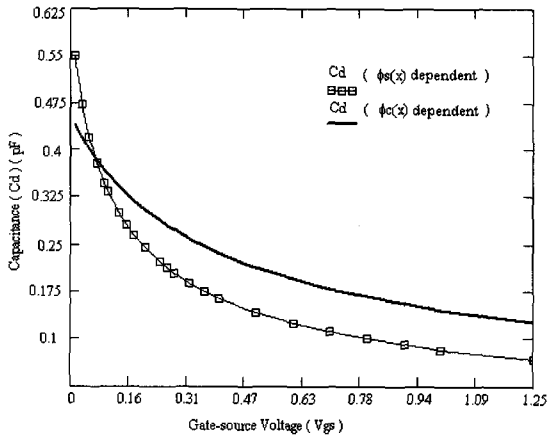

Fig. 7. Depletion layer capacitance based on different potential (i.e. surface and center). Other parameters are $L_1=L_2=50nm$, $t_{SI}=12nm$, $t_{oxf}=t_{oxb}=2nm$, $V_{DS}=0.5V$, $\phi_{M2}=4.17\,V$, $\phi_{M1}=4.77V$.

III. Results And Discussion

The 2-D device simulator ATLAS was used to verify the proposed P-IV based DM DG FD SOI MOSFET. The base of our device model is that it has considered the doping distribution *i.e.* $N_a(y)\big|_{y=t_{SI}}$, dependent on the thickness of the silicon film through Pearson-IV distribution. It gives more accurate picture of the device instead of considering doping distribution constant *i.e.* N_a. Along with this, all parameters i.e. drain current, transconductance, channel resistance, depletion layer capacitance were calculated keeping potential at the center in view instead of surface potential (Fig. 3-7). Because of double gate, main consideration must be on potential at the center, ϕ_c, than at the surface, ϕ_s, which is required in case of single gate MOS. In our device, ϕ_c is greater than ϕ_s as shown in the Fig. 2.

Fig. 8 shows the variation of drain-source current with drain-source voltage for various gate voltages. It is further compared with simulated data of dual material double gate model and double gate model. DM DG MOSFET shows a definite enhancement over simple DG MOSFET because of the difference in work function of the materials. Also by considering the Pearson-IV doping distribution a remarkable increase in drain current is observed. For a slight change in skewness, a large change

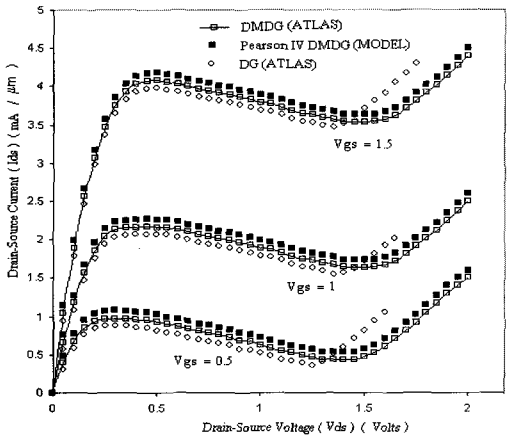

Fig. 8. $I_{DS}-V_{DS}$ characteristics of the Pearson-IV DM DG and DG FD SOI MOSFETs for a channel length $L_g=0.1\,\mu m$. Other parameters are $L_1=L_2=50nm$, $V_{DS}=0.5\,V$, $\phi_{M1}=5.25V$, $\phi_{M2}=4.17\,V$, $t_{SI}=12nm$, $t_{oxf}=t_{oxb}=2nm$.

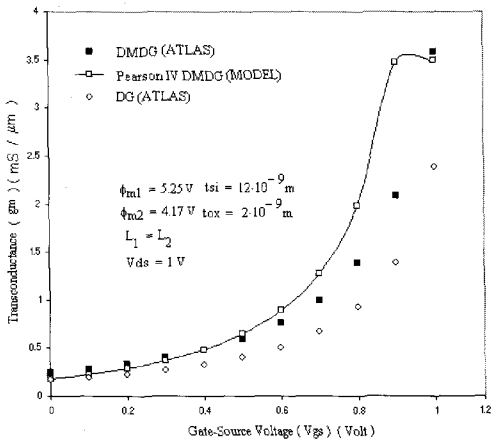

Fig. 9. Transconductance g_m for Pearson-IV DM DG and DG FD SOI MOSFETs for a channel length $L_g = 0.1\,\mu m$.

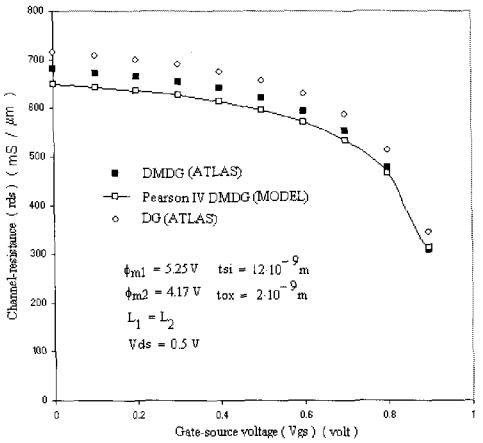

Fig. 10. Channel resistance r_{ds} for Pearson-IV DM DG and DG FD SOI MOSFETs for a channel length $L_g = 0.1\,\mu m$.

in drain current is noticed. So, these moments, skewness and kurtosis are important in device modeling and cannot be neglected.

Fig. 9 is the plot of channel transconductance with gate voltage and compared with simulated data. The transconductance increases with increase in gate voltage because of the increased number of carriers moving through center of the channel. In Fig. 10 the variation of channel resistance with V_{gs} is shown and compared with simulated data. As we increase the V_{gs}, channel resistance decreases because of the more energy implants move towards drain. Fig. 11 shows the capacitance with gate-source voltage. The capacitance increases with decrease in V_{gs} because of the excess majority carriers accumulating under the gate when we decrease the V_{gs}.

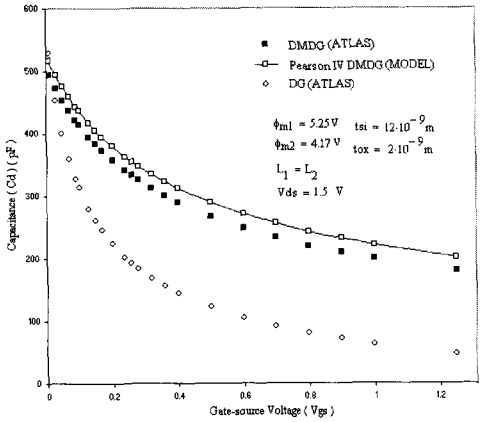

Fig. 11. Depletion layer capacitance for Pearson-IV DM DG and DG FD SOI MOSFETs for a channel length $L_g = 0.1\,\mu m$.

IV. CONCLUSIONS

For the first time, we have examined the effectiveness of the Pearson-IV type doping distribution and the potential at the centre of the channel of DM DG FD SOI MOSFET to extract the true picture of the device and comparing the results with the ATLAS simulations. Our results also established that the concept of DM DG (symmetric device) in a fully depleted SOI MOSFET minimizes the SCEs because of the step function profile of the channel potential.

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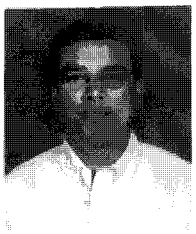

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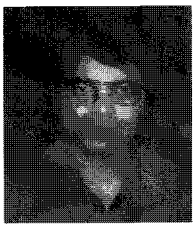

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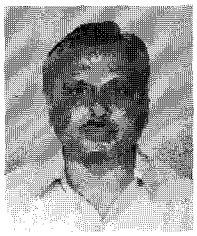

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