PWM/PFM Dual Mode SMPS Controller IC for Active Forward Clamp and LLC Resonant Converters

Jeongin Cheon and Changwoo Ha

Abstract—The desin and implementation of a CMOS analog integrated circuit that provides dual-mode modulations, PWM for active clamp reset converter and PFM for LLC resonant converter, is described. The proposed controller is capable of implementing programmable soft start and current-mode control with compensating ramp for PWM and frequency shifting soft start for PFM. Also it provides delay time for both modes. PWM mode is implemented by active clamp reset converter and PFM mode is implemented by LLC resonant convereter, respectively. The chip is fabricated using the 0.6um high voltage CMOS process.

Index Terms—PWM/PFM controller, AFC, LLC

I. INTRODUCTION

Recently power supplies are required wider dynamic range and higher efficiency. One of the solutions of these requirements is to use two types of converters at one power system. At large load current conditions pulse width modulation (PWM) is used to achieve high efficiency. In the other hand, at light load current conditions or at standby time pulse frequency modulation (PFM) is used.

We present a SMPS controller IC operating dual modes, PWM mode for active clamp converter and PFM mode for LLC resonant converter. Therefore this controller IC enables to achieve active clamp converter and LLC in one system with switching the mode.

Switching between PWM mode and PFM mode may be accomplished by monitoring the output voltage and the output current [1].

However, we implemented two converters for each mode, performed the full circuit simulation.

II. ARCHITECTURE OF DUAL MODE CONTROLLER IC

The proposed controller IC provides two modulation methods, PWM and PFM one of which is selected by switching MODE pin. Fig. 1 shows the overall block diagram which consists of clock generator, reference and bias block, PWM block, PFM block and driver block.

To provide the dual modulation modes the oscillator is comprised of an oscillation block in which current controlled clock signal is generated and a function selection block in which the modulation mode of the oscillator is selected and the oscillation parameters are determined. The charge and discharge currents are correlated in order to improve the duty ratio of oscillator. They may be used to achieve power protections. The resistor Rdel manipulates the turn-on delay time of the two gate drive outputs which operates in both PWM and PFM modes.
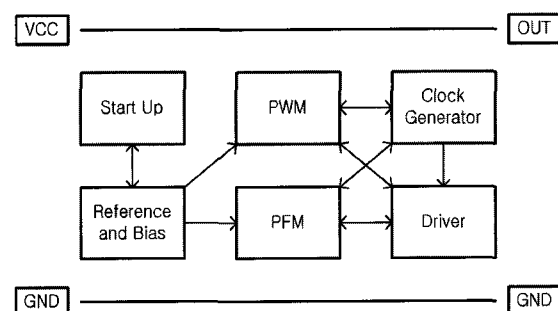

Fig. 1. Architecture of Dual Mode Controller.

1. Operation in PWM mode(ACF mode)

The system block diagram of the controller IC in PWM mode is shown Fig. 2.

With the PWM mode selected the controller operates an active clamp forward (ACF) converter. External resistances Rt1 and Rt2 are used to define the amount of current which charges and discharges the capacitance Ct with setting the oscillation frequency and maximum duty ratio.

Peak current-mode control, soft start, voltage feedback and other logics for PWM in the PWM block are also activated by selecting the PWM mode. Peak current-mode control uses a slope compensation which adds the compensating ramp to current sense input [2]. The slope of compensating ramp can be determined by external resistance Rslope to set the slope between $0.5 \leq m \leq 1$. The capacitor Css sets soft start time. Soft start in the PWM mode to prevent the output overshoot during the initial start-up gradually increases the duty ratio. FB pin senses output voltage signal fed back from secondary side output voltage. Duty ratio is modulated by comparing the current sensing signal from the primary side and the output voltage signal fed back from the secondary side to the primary side by optocoupler.
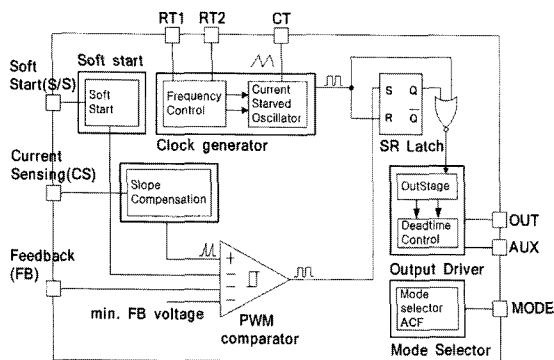

Fig. 2. Operating Block in ACF(PWM) mode.

2. Operation in PFM mode(LLC mode)

The system block diagram of the controller IC in PWM mode is shown Fig. 3. With the PFM mode selected the controller operates an LLC resonant converter with an accurate 50% duty ratio. The functions of Rt1 and Rt2 are changed as the mode is changed. Rt1 and Rt2 determine the initial charge and discharge
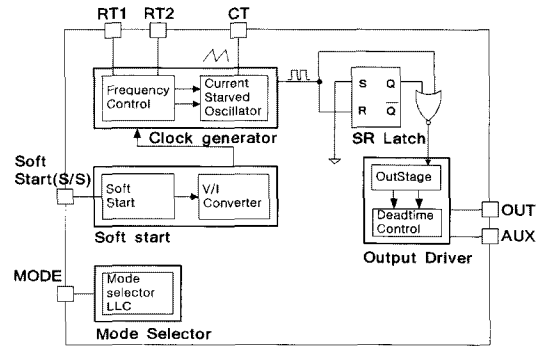

Fig. 3. Operating Block in LLC(PFM) mode.

current and the minimum charge and discharge current of Ct, and as a result they set the initial frequency and the minimum frequency, respectively.

The Soft start in the PFM mode decreases the operation frequency as the capacitor Css is charged by a current which depends on Rt1. The functions of FB pin and CS pin are changed from the detection of output voltage into a latched shutdown and from the current detection into a restart.

III. CONTROLLER IC IMPLEMENTATION

The controller IC is implemented in a 0.6um CMOS process. The die photograph of the chip is shown in Fig. 4. The total chip area is 1600*2300.

In order to reduce the interference of the switching noise of the gate drive outputs, each block is surrounded by guard rings which are connected with ground and the oscillator is arranged far away from the driver block.

The driver block is designed as CMOS tapered buffers which have a scaling factor of 5 for a minimum power-delay product [3]. The output current driving capability of the driver block is also designed to drive a maximum current of 1A.
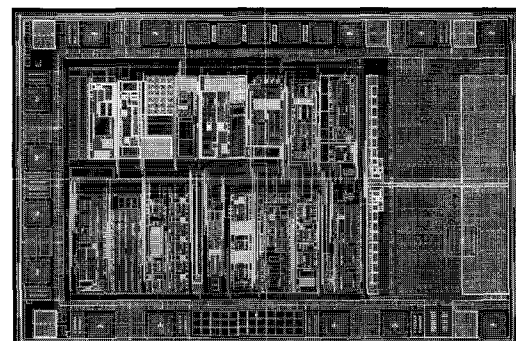

Fig. 4. SMPS controller chip Layout.

IV. TESTING RESULTS

The dual–mode SMPS controller IC was then evaluated for performance. The results verify (Fig. 5 thru 6) a designed duty and frequency in each mode.

Table 1. summarizes the application and the measured performance of the controller IC.

Table 1. Chip performance summary.

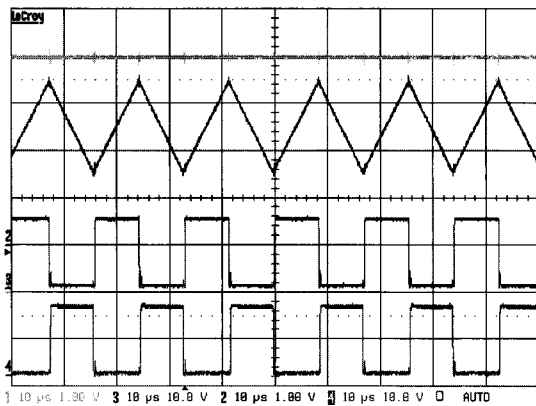| Vcc enable on voltage	10V
Reference voltage	5V
ACF mode operating frequency	80KHz
ACF mode max. duty cycle	70%
LLC mode minimum frequency	60KHz (RT2=50k)
LLC mode soft start frequency	120KHz(RT1=50k)
LLC mode duty cycle	50%
Output delay time	160ns (Rdel=100k)

Fig. 5. Experimental transient response in PFM mode.
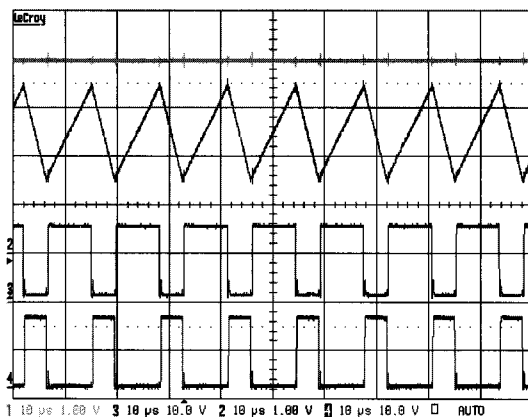a) duty cycle = 50%
b) minimum frequency = 60KHz

Fig. 6. Experimental transient response in PWM mode.
a) duty cycle = 70%
b) minimum frequency = 80KHz

V. CONCLUSIONS

This paper describes a dual mode SMPS controller IC for Active Clamp Forward converter and LLC resonant converter. The MagnaChip 0.6um CMOS technology is used to design and simulate the proposed controller. The controller IC has been developed which gives good performance-variable frequency range, programmable soft start-with Active Clamp Forward converter and LLC resonant converter system. Also, The controller IC which incorporates the dual mode operation system is easier to manufacture, has a higher reliability and is reduced in cost.

REFERENCES

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[2]   Fontan, A., Ollero, S.; de la Cruz, E.; Sebastian, J. "Peak current mode control applied to the forward converter with active clamp" *Power Electronics Specialists Conference, 1998. PESC 98 Record. 29th Annual IEEE*, vol. 1, pp.45-51, May 1998.

[3]   Jso-Sun Choi; Kwyro Lee; "Design of CMOS Tapered Buffer for Minimum Power-Delay Product", *Solid-State Circuits, IEEE journal*. vol. 29, pp.1142-1145, Sept. 1994.

Jeongin Cheon was born in Ul-san, kyungnam, Republic of Korea, 1976. He received the MA. degree in electrical engineering from Sogang University, Seoul, in 2004. He joined Samsung Electro-Mechanics. Co. as the analog asic designer, at 2004. During 2004-2005, he joined the project of the 3D motion sensor IC. And He designed Dual mode SMPS controller IC for PDP TV power supply at 2006. Now he challenge the new project for LED Driver and Integrated Power Controller.
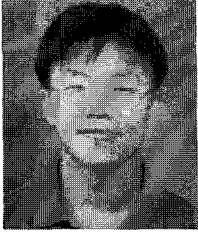
Changwoo Ha was born in masan, kyungnam, Republic of Korea, 1973. He received the MA. degree in electrical engineering from Hong Ik University, Seoul, in 2002. He joined Samsung Electro-Mechanics. Co. as the analog asic designer, at 2002. During 2002-2004, he designed photo-detection ic for Optical Disc. He designed pieazo actuator drive IC for mobile camera at 2005 and Dual mode SMPS controller IC for PDP TV power supply at 2006. Now he challenge the new project for LED Driver and Integrated Power Controller.