Influences of Trap States at Metal/Semiconductor Interface on Metallic Source/Drain Schottky-Barrier MOSFET

Won-Ju Cho

***Abstract*—The electrical properties of metallic junction diodes and metallic source/drain (S/D) Schottky barrier metal-oxide-semiconductor field-effect transistor (SB-MOSFET) were simulated. By using the abrupt metallic junction at the S/D region, the short-channel effects in nano-scaled MOSFET devices can be effectively suppressed. Particularly, the effects of trap states at the metal-silicide/silicon interface of S/D junction were simulated by taking into account the tail distributions and the Gaussian distributions at the silicon band edge and at the silicon midgap, respectively. As a result of device simulation, the reduction of interfacial trap states with Gaussian distribution is more important than that of interfacial trap states with tail distribution for improving the metallic junction diodes and SB-MOSFET. It is that a forming gas annealing after silicide formation significantly improved the electrical properties of metallic junction devices.**

***Index Terms*—metallic junction, Schottky barrier MOSFET, interface trap, forming gas annealing**

I. INTRODUCTION

As High-speed/high-density advanced metal–oxide–semiconductor (MOS) devices require extremely short channel lengths, the International Technology Roadmap for Semiconductors (ITRS) states that the semiconductor industry has "entered the era of material-limited device scaling" [1]. The conventional materials constituting the metal-oxide-semiconductor field-effect transistor (MOSFET) device have been extended to the performance limitations. In order to overcome such problems, new materials such as high-k gate insulators, strained-silicon substrates, metal gates, and metallic source/drain (S/D) junctions are under development. Especially, the use of metallic junction-based silicon devices is expected to be the post-CMOS device technology [2-5]. In metallic junction-based MOSFET, the conventional S/D impurity doping is replaced by the metal, typically silicide. There are numerous advantages in metallic S/D junctions, including low parasitic S/D resistance, low-temperature processing for S/D formation, elimination of parasitic bipolar action, and inherent physical scalability to sub-10-nm gate-length dimensions, which is due to the low resistance of metal and the atomically abrupt junctions formed at the silicide–silicon interface. Because the metallic junctions are formed at the interface of metal S/D and silicon substrates, the metallic S/D MOSFET device is known as a Schottky barrier MOSFET (SB-MOSFET). However, the reaction between metal and semiconductor causes the inhomogeneity of interface and generates a considerable quantity of trap states [6]. Therefore, in order to improve the performance of metallic junction devices, the insight into the interfacial properties of Schottky junction will be indispensable. Although the current–voltage (I–V) measurement method has been widely used to evaluate the trap states in Schottky junction [6,7], there are few works on the quantitative relationships between the trap states at the metal-silicide/silicon and the electrical characteristics of metallic S/D SB-MOSFET.

In this paper, the device simulations for the metallic

Manuscript received Apr. 12, 2007; revised , Jun. 4, 2007.
Department of Electronic Materials Engineering, Kwangwoon University 447-1, Wolgye-dong, Nowon-gu, Seoul, KOREA, 139-701
E-mail : chowj@kw.ac.kr

junction diodes and metallic S/D SB-MOSFET are carried out. The effects of interfacial trap states with the tail distributions at the band edge and the Gaussian distribution traps at the midgap on the electrical characteristics of metallic junction diodes and metallic S/D SB-MOSFET were calculated. Additionally, the Schottky junction diodes and SB-MOSFET were fabricated and the experimental results were compared with the simulated results.

II. Simulation and Experiment

The device simulation was carried out by taking into account the electron tunneling, the thermionic emission and the Schottky barrier lowering effects at the interface of metal-silicide/silicon. The current-voltage (I-V) characteristics of Schottky junction diodes were calculated as a function of metal work function. Based on the Schottky junction diodes, the electrical characteristics of SB-MOSFET were simulated. Because the microscopic inhomogeneity due to the silicide reactions between deposited metal and silicon substrate, a large number of interface trap states will be generated at the interface of metal-silicide/silicon and degrade the performance of metallic junction device. In order to estimate the effects of interface traps at the metal-silicide/silicon on the Schottky junction diodes and SB-MOSFET, the two types of interfacial trap distributions are assumed as shown in the Fig. 1.

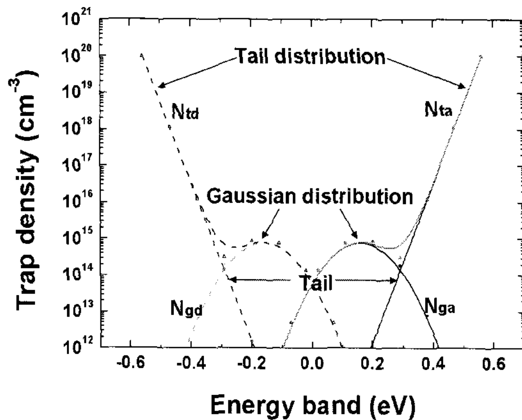


Fig. 1. Interface trap distributions at metal-silicide/silicon interface. N_{ta}: acceptor-type tail states, N_{td}: donor-type tail states, N_{ga}: acceptor-type Gaussian states, N_{gd}: donor-type Gaussian states.

It is assumed that the density of defect states (DOS) g(E) is composed of four band: two deep level bands modeled by Gaussian distribution and two tail bands[8-11].

$$g_{ta}(E) = N_{ta}\exp\left[\frac{E-E_c}{W_{ta}}\right] \quad (1)$$

$$g_{td}(E) = N_{td}\exp\left[\frac{E_v-E}{W_{td}}\right] \quad (2)$$

$$g_{ga}(E) = N_{ga}\exp\left[-\left[\frac{E_{ga}-E}{W_{ga}}\right]^2\right] \quad (3)$$

$$g_{gd}(E) = N_{gd}\exp\left[-\left[\frac{E-E_{gd}}{W_{gd}}\right]^2\right] \quad (4)$$

Here, E is the trap energy, E_c is conduction band energy, E_v is the valence band energy and the subscript (t, g, a. d) stand for tail, Gaussian (deep level), acceptor and donor states respectively. For an exponential tail distribution, the DOS is described by its conduction and valence band edge intercept densities N_{ta} and N_{td}, and by its characteristic decay energy W_{ta} and W_{td}. For Gaussian distribution, the DOS is described by its total densities of states N_{ta} and N_{td}, its characteristic decay energy W_{ga} and W_{gd}, and its peak energy distribution E_{ga} and E_{gd}. The effects of trap density with tail distribution or Gaussian distribution on the forward bias current or reverse bias current of Schottky junction diode were calculated. In case of SB-MOSFET, the trap positions as well as trap density can influence in the electrical characteristics. Therefore, we simulated the device performance by considering the position of trap position at the source junction or drain junction.

In order to confirm the validity of the device simulations, the Schottky junction diodes and metallic S/D SB-MOSFET were fabricated and the experimental results were compared with calculated results. Erbium is chosen as a metallic junction material, because it has low Schottky barrier height for electrons. The boron doped (100) p-type bulk silicon wafer with a resistivity of 10–20 Ω·cm was used for the erbium-silicided Schottky junction diode. After initial cleaning of Si wafer, 100-nm-thick SiO_2 layer was grown on the wafers using thermal oxidation and the active region of diode was opened using lithography and wet etching processes. The erbium-

silicide was formed by using sputtering and rapid thermal annealing (RTA) method at 500 °C for 5 min. The non-reacted erbium was then removed by using sulfuric peroxide mixture (SPM) solution (H_2SO_4:H_2O_2= 1:1) for 10 min. On the other hand, (100) p-type silicon-on-insulator (SOI) wafers were used as a starting material for fabrication of metallic S/D SB-MOSFET. The thickness of the SOI and buried oxide (BOX) layer was 100 nm and 200 nm, respectively. The gate oxide with a 5-nm-thickness was grown by thermal oxidation and the in-site phosphorus doped n-type poly-Si was deposited by LPCVD as a gate electrode. After formation of gate electrode with 2 to 20-μm-length, the gate sidewall spacer with a 30-nm-thickness was formed. Then, 100-nm-thick erbium layer was sputtered and the erbium-silicided source/drain regions were formed by RTA. Additionally, a forming gas anneal was carried out in 3% H_2 mixed gas in N_2, 450°C, 10m to improve the interface trap states.

III. RESULTS AND DISCUSSION

Fig. 2 shows the current-voltage (I-V) characteristics of metallic junction diodes (Schottky junction diodes) on the p-type silicon substrate as function of metal work function.

As shown in Fig. 2(a), the I-V curves are changed from the typical rectification characteristics to the ohmic behaviors as the work function of metal increases. A leakage current with reverse bias increases with metal work function as shown in Fig.2 (b). Therefore, in order to obtain a satisfactory rectification performance on the p-type silicon substrates, the acceptable metal work functions should be less than 4.5 eV.

Figure 3 shows the I-V curves of Schottky junction diodes as function of interface trap states density with the tail distributions (a) and with the Gaussian distributions (b). It is found that the ideality factor of forward bias current and the leakage current of reverse bias current increase with the interface trap states and the degradation of I-V curves are observed. Especially, the Gaussian traps located at the deep energy level considerably degrade the I-V curves. Therefore, we can conclude that the reduction of Gaussian trap distribution rather than the tail distribution is more effective to improve the Schottky junction properties.

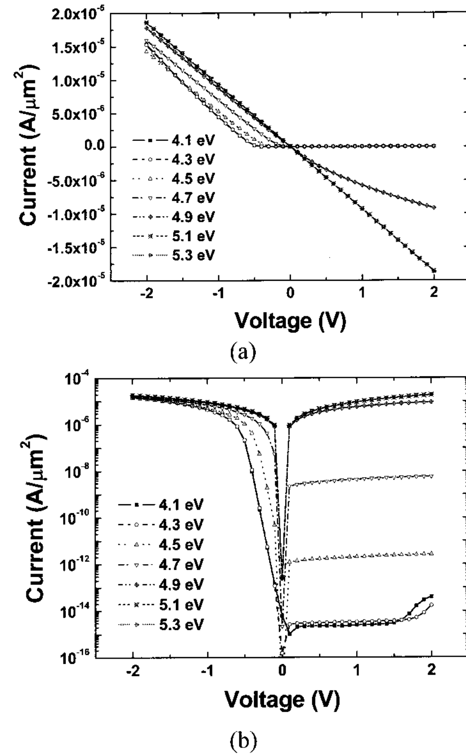


Fig. 2. Interface trap distributions at metal-silicide/silicon interface. N_{ta}: acceptor-type tail states, N_{td}: donor-type tail states, N_{ga}: acceptor-type Gaussian states, N_{gd}: donor-type Gaussian states.

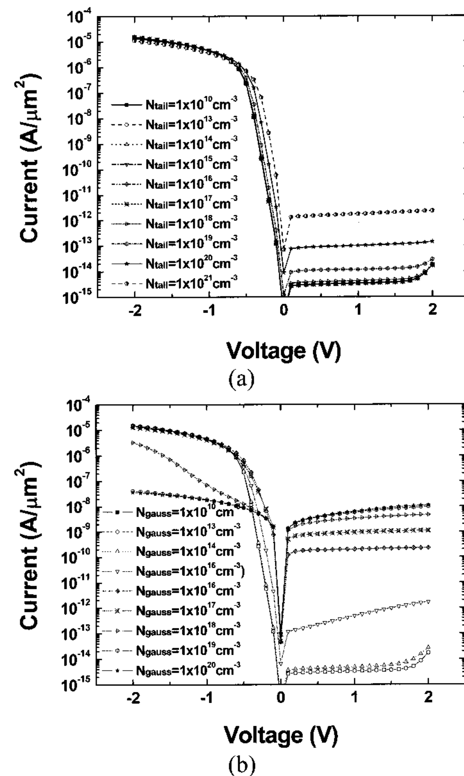
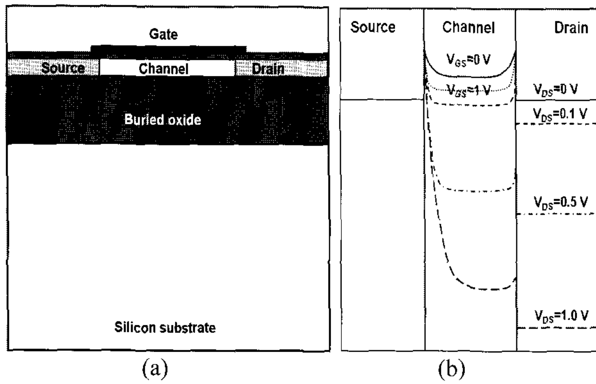
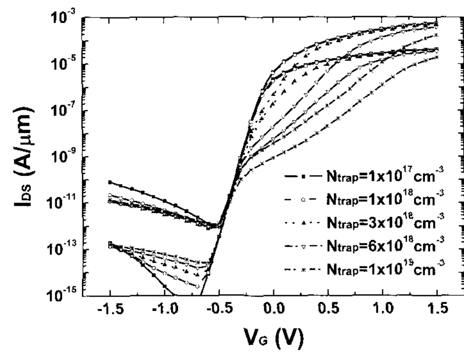


Fig. 3. Current-voltage characteristics of Schottky junction diodes as function of interface trap density. (a) tail distributions, (b) Gaussian distributions.



(a)

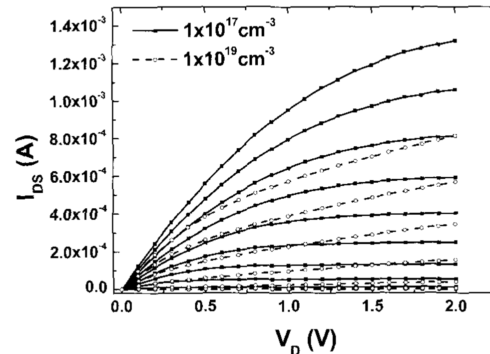


(b)

Fig. 4. Simulated device structure (a) and conduction band energy at the metal silicide-silicon interface along the channel direction for $N_a=10^{15}$ cm^{-3} as a function of gate voltage and drain voltage.

Fig. 4 shows the simulated metallic S/D SB-MOSFET device structure on SOI substrates (a), and the conduction band energy diagram at the metal silicide-silicon interface along the channel direction for $N_a=10^{15}$ cm^{-3} as a function of gate voltage and drain voltage (b). The work function of metallic S/D and the electron affinity of silicon are assumed as 4.3 eV and 4.01 eV, respectively. The single-gate SOI with silicide source/drain structure is used in the device simulation of SB-MOSFET to suppress the short channel effects. The gate oxide, the SOI layer and the buried oxide layer thicknesses are 4 nm, 10 nm and 100 nm, respectively. The source/drain junction depth is the same with the SOI layer thickness. The electrons in n-type metallic S/D SB-MOSFET tunneling through the Schottky barrier from the source to the channel are controlled by the voltage applied to the gate across the gate oxide. The carrier transport at the Schottky barrier is modeled by the combinations of the thermal emission current component and the tunneling current component. The Schottky barrier lowering due to the image force at the interface of metal/silicon is also included in the calculation.

Fig. 5 shows the current-voltage characteristics of SB-MOSFET as function of interface trap density. We assumed that the interface traps are distributed at both source and drain Schottky junctions. As shown in Fig. 5(a), the subthreshold curves are significantly distorted and the subthreshold swing degrades when the interface trap states density is larger than $1 \times 10^{18} cm^{-3}$. As a result, the device performance is considerably degraded as shown in Fig. 5(b).



(a) I_{DS}-V_G characteristics

(b) I_{DS}-V_D characteristics

Fig. 5. Current-voltage characteristics of SB-MOSFETs as function of interface trap density.

Fig. 6 shows the dependence of I_{DS}-V_G characteristics on the interface trap states position in SB-MOSFET. When the interface trap states located at the drain side, the degradation of IDS-VG characteristics is negligible. On the other hand, the interface trap states located at the source side, the degradation of IDS-VG characteristics can not be ignored. Therefore, it is noted that the reduction of interfacial trap states at the source side is more important for improving the metallic S/D SB-MOSFET.

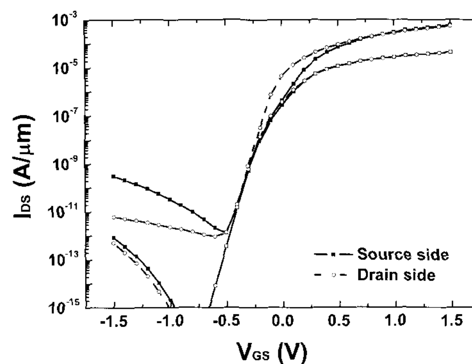


Fig. 6. Dependence of I_{DS}-V_G characteristics on interface trap states position of SB-MOSFET.

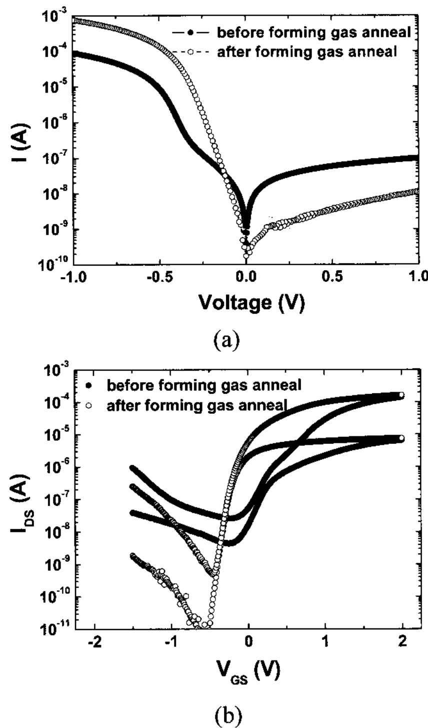


Fig. 7. Measured I-V characteristics of Erbium Schottky junction diode (a) and SB-MOSFET (b). Forming gas annealing in 3% H_2 mixed N_2, 450°C, 10m.

Fig. 7 shows the measured I-V characteristics of fabricated metallic junction diodes (a) and n-type metallic S/D SB-MOSFET (b). I-V curves of fabricated Schottky junction diode and SB-MOSFET revealed a high leakage current at the off-state and a low operating current at the on-state as shown by closed circles. It is found that a good agreement between the simulation and experiment was observed. We consider that the degradation of diode and SB-MOSFET characteristics is associated with the interface trap states at Schottky junctions. In order to decrease the interface trap density and to improve the electrical characteristics, a forming gas anneal was carried out in 3% H_2 mixed gas in N_2, 450°C, 10m. As a result, a significant improvement of device properties was achieved as shown by open circles. Therefore, it is concluded that the forming gas anneal after silicide formation is very effective for improve the Schottky junction diode and metallic S/D SB-MOSFET.

IV. CONCLUSIONS

The device characteristics of metallic junction diodes and metallic S/D Schottky MOSFET for post CMOS devices were simulated. The I-V characteristics of Schottky junction diodes were calculated as function of metal work function. Also, the effects of trap states at the metal-silicide/silicon interface of S/D junction were simulated by taking into account the tail distributions and the Gaussian distributions at the band edge and at the midgap, respectively. The degradations of Schottky junction diodes and SB-MOSFET were observed with the increase of interface trap states density. Especially, the Gaussian trap states at the midgap have considerable effects on the degradation of I-V curves. The simulations for metallic junction diodes and metallic S/D Schottky MOSFET are well coincide with the experimental results. A forming gas annealing after silicide formation is very effective for improving the Schottky junction diode and SB-MOSFET.

REFERENCES

[1] "Front end processes," in *International Technology Roadmap for Semiconductors 2003 Edition*. Austin, TX: Semiconductor Industry Assoc., 2003.

[2] E. Dubois and G. Larrieu, "Measurement of low Schottky barrier heights applied to S/D metal-oxide-semiconductor field effect transistors," J. *Appl. Phys.*, vol. 96, no. 1, pp. 729–737, Jul. 2004.

[3] J. Kedzierski, P. Xuan, E. H. Anderson, J. Bokor, T.-J. King, and C. Hu, "Complementary silicide S/D thin-body MOSFETs for the 20 nm gate length regime," *IEDM Tech. Dig.*, 2000, pp. 57–60.

[4] B.-Y. Tsui and C.-P. Lin, "A novel 25-nm modified Schottky-barrier FinFET with high performance," *IEEE Electron Device Lett.*, vol. 25, no. 6, pp. 430–432, Jun. 2004.

[5] S. Matsumoto, M. Nishisaka, and T. Asano, "CMOS application of Schottky S/D SOI MOSFET with shallow doped extension," Jpn. *J. Appl. Phys.*, vol. 43, no. 4B, pp. 2170–2175, 2004.

[6] R. T. Tung, "Electron transport at metal-semiconductor interfaces: general theory," *Phys. Rev. B, Condens. Matter,* vol. 45, pp. 13509-13523 (1992).

[7] R. B. Darling, "Current-voltage characteristics of Schottky barrier diodes with dynamic interfacial defect state occupancy," *IEEE Trans. Electron.*

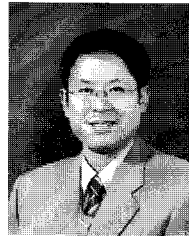
Devices, vol. 43, no. 7, pp. 1153-1160 (1996).

[8] A. M. Kemp, M. Meunier and C. G. Tannous, "Simulations of the amorphous silicon static induced transistor", *Solid-State Elect.*, Vol. 32, No. 2, pp.149-157 (1989).

[9] B. M. Hack and J. G. Shaw, "Numerical simulations of amorphous and polycrystalline silicon thin-film transistors", *Extended Abstracts 22nd International conference on Solid-State Device and Materials*, pp.999-1002 (1990).

[10] C. John G. Shaw and M. Hack, "An analytical model for calculating trapped charge in amorphous silicon", *Journal of Appl. Phys.*, 64 (9), pp.4562-4566 (1988).

[11] ATLAS User's Manual, *SILVACO*, Vol. 2, pp. 13.1-13.5 (2002).



Won-Ju Cho was born in Daegu, Daegu, Korea, 1967. He received the B.S. degree from Kyungpook National University, Daegu, Korea, in 1989, and the M.S. and Ph.D. degrees in electrical engineering from Keio University, Tokyo, Japan, in 1991 and 1994, respectively. During 1994-2000, he joined in the HYNIX Semiconductor Inc., Korea. During 1999-2000, he was with the AIST, Tsukuba, Japan, where he developed the ultra-low-loss power SiC devices. During 2000-2004, he joined in Electronics and Telecommunications Research Institute (ETRI), Daejon, Korea, for development of nanoscale silicon MOSFET devices and nano-bio sensors. Recently, he was appointed Professor of Department of Electronic Materials Engineering at the Kwangwoon University, Seoul, Korea. His current research interests include new electronic materials and devices, simulations, processing, and analysis of nanoscale silicon devices, memories, Bio-devices, micro- and nano-electromechanical systems (MEMS & NEMS).