

# A Sense Amplifier Scheme with Offset Cancellation for Giga-bit DRAM

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**Abstract**—To improve low sense margin at low voltage, we propose a negatively driven sensing (NDS) scheme and to solve the problem of WL-to-BL short leakage fail, a variable bitline reference scheme with free-level precharged bitline (FLPB) scheme is adopted. The influence of the threshold voltage offset of NMOS and PMOS transistors in a latch type sense amplifier is very important factor these days. From evaluating the sense amplifier offset voltage distribution of NMOS and PMOS, it is well known that PMOS has larger distribution in threshold voltage variation than that of NMOS. The negatively-driven sensing (NDS) scheme enhances the NMOS amplifying ability. The offset voltage distribution is overcome by NMOS activation with NDS scheme first and PMOS activation followed by time delay. The sense amplifier takes a negative voltage during the sensing and amplifying period. The negative voltage of NDS scheme is about  $-0.3V$  to  $-0.6V$ . The performance of the NDS scheme for DRAM at the gigabit level has been verified through its realization on 1-Gb DDR2 DRAM chip.

**Index Terms**—DRAM, charge-transferred presensing (CTPS), negatively-driven sensing(NDS), free-level precharged bitline(FLPB), sense amplifier offset voltage, threshold voltage distribution.

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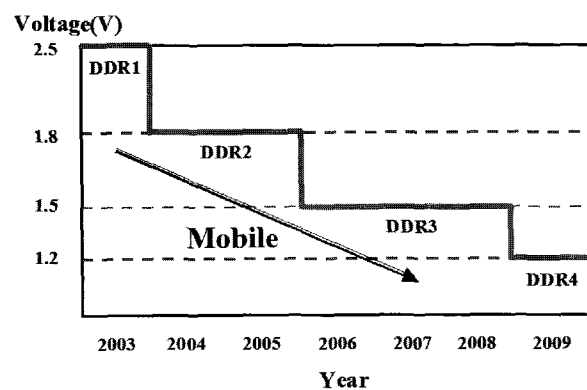
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## I. INTRODUCTION

It will be able to continue to shrink its chip technology through at least 2009 to about 20nm-30nm range. Recent breakthroughs in the improved manufacturing methods have sparked considerable excitement about the nanoscale memories. Memory circuits, such as dynamic random access memory (DRAM) arrays, have increased in complexity and density over time. To meet the technology trend, the memory circuits should adopt the low voltage and low power based scheme [1][2].

The trend for low voltage and low power is shown in Fig. 1. The PC based DRAMs such as DDR1, DDR2, DDR3, etc. go down to near to 1.0V and the mobile application based DRAMs go down to sub 1.0V with technology scaling.

In general for low voltage operation in MOS transistor based circuit, the threshold voltage ( $V_t$ ) of MOS device should be reduced to low threshold voltage value. But the low  $V_t$  value in MOS device induces a large sub threshold leakage current level, producing large stand-by



**Fig. 1.** The trend of operation voltage in PC and mobile based DRAM.

current and active dynamic current level. If a high  $V_t$ , the power consumption from sub threshold leakage current could be reduced, but a large speed delay induces performance degradation at the sensing circuit. One potential limitation regarding the use of a high  $V_t$  device in sense amplifier is that the speed of the sense amplifier may be reduced. The sense amplifier circuit typically has activation lines used to activate the data lines responsive to the values stored in the memory cells. To reduce standby currents, one of the activation lines may be grounded prior to a memory read cycle. The signal on the grounded activation line must then pass the entire range from ground to VDD to pull the data line to the desired state. The need for this full range swing reduces the response time of the sense amp circuitry. As operating voltages decrease, the sense amp circuit becomes slower, because of the lower NMOS gate-to-source voltage.

In DRAM a lot of the power consumption is likely from the charging and discharging current at bitlines (BLs) in a memory cell array. The voltage reduction at BLs directly related to power reduction by the power consuming relationship of  $P=CV^2f$ . And another issue in device scaling down is very likely that one or more shorts will occur between a WL and a BL [3]. A WL-to-BL short typically is a point defect that shorts together a particular row line to a perpendicular data line. The short faults increase the standby current and make difficulty in the negatively biasing word line (WL) scheme. As DRAM array sizes grow, however, row-to-column shorts become more prevalent. Redundancy rows and columns are created within the DRAM array in combination with address redirection circuitry to substitute functional spare rows and columns for those that are shorted. Even though this on-chip redundancy allows for the repair of a DRAM integrated circuit device, it is important to note that the shorted columns and rows are not disconnected from the array circuitry. The shorted columns and rows are merely no longer addressed by the array's address decode circuitry. Disconnection of the shorted rows and columns from the array circuitry is impractical with presently available technology due to the small pitch used to fabricate DRAM arrays. The repair of row to column shorts through redirected addressing does not eliminate the presence of shorts within the array, nor does it eliminate the potential for biased voltage pull

down with the attendant problems of excessive standby current, read and write operations resulting in invalid data and possible damage to cell capacitors within the array. For example, one serious problem is that of an increase in the quiescent standby current because of a defect in the circuit.

To solve the problem of WL-to-BL short, a variable bitline reference scheme with free-level precharged bitline (FLPB) scheme is adopted.

To overcome the sensing delay in the conventional sensing scheme, we propose a negatively driven sensing (NDS) scheme [4]. The NDS scheme achieves high performance properties of fast sensing speed and high data transfer rate at the sub-1.0V sensing voltage. NDS scheme automatically provides the dual operating voltage levels between BL voltage in cell array region and sense amplifier voltage in sense-amplifier area.

The sense amplifier circuit and the bit line architecture determine the signal limit for DRAM cell readout. Increasing memory sizes, smaller feature sizes and lower operating voltages make it more important to understand the cell signal sensing operation, the signal of memory cells and the limiting factors of process and circuit design. Measurements analysis of the sense amplifier offset distribution gives further insight into the sensing limitations. The process variations in the latch NMOS and PMOS transistors have been evaluated. The threshold voltage offset occurring in the latch type sense amplifier has been analyzed. From evaluating the sense amplifier offset voltage distribution of NMOS and PMOS, we learned that PMOS has more large distribution in threshold voltage variation than that of NMOS. The offset voltage distribution is overcome by NMOS activation first and PMOS activation followed by time delay in large voltage range. But there is limit for more improving in low voltage operation range. In this paper we use the NDS scheme for improving the sense amplifier offset voltage contribution using the conventional sense amplifier circuit and NDS control scheme.

## II. CHARGE-TRANSFERRED PRESENSING (CTPS) AND CONVENTIONAL SENSING SCHEME

To improve the sensing performance in low voltage,

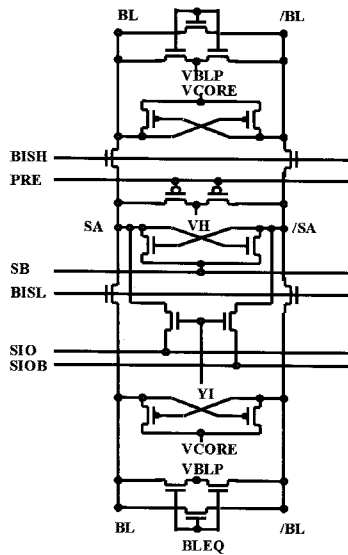


Fig. 2. The circuit details of charge-transferred presensing (CTPS) scheme.

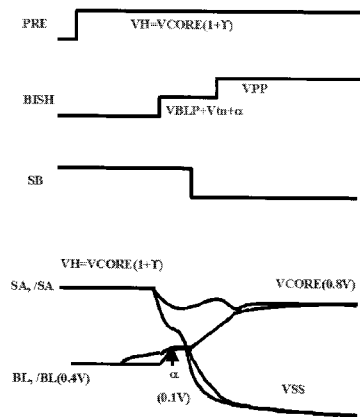


Fig. 3. The timing details of charge-transferred presensing (CTPS) scheme.

charge-transferred presensing (CTPS) scheme [1] has been proposed. The circuit and timing waveform of the conventional CTPS are shown in Fig. 2 and Fig. 3. But it requires additional transistors for transfer gates and very accurate reference level is required to have presensing effect.

The SA and BL are isolated by the transfer-gate of BISH. Here, the BISH is used for transferring the stored charge from BL to SA nodes. The BL is precharged to one-half of the power supply voltage for the array (VCORE), and the SA node is precharged at a higher level than VCORE. When the BISH level is a low level, WL is activated, and the data of memory cell is transferred to BL. Charge-transfer to BL from SA is complete when the original level of ( $V_{BISH}-V_{tn}$ ) is

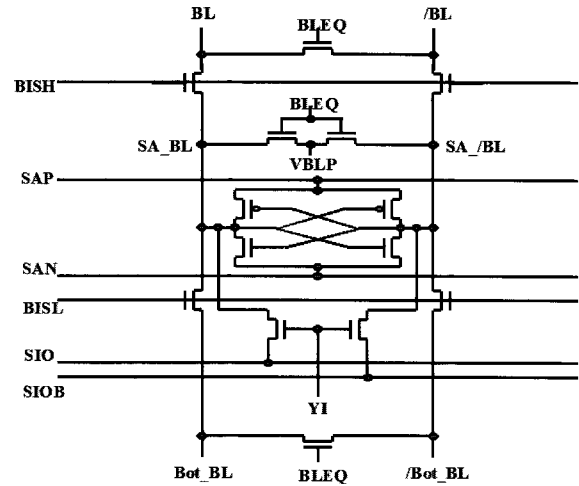


Fig. 4. The conventional sense amplifier circuit details.

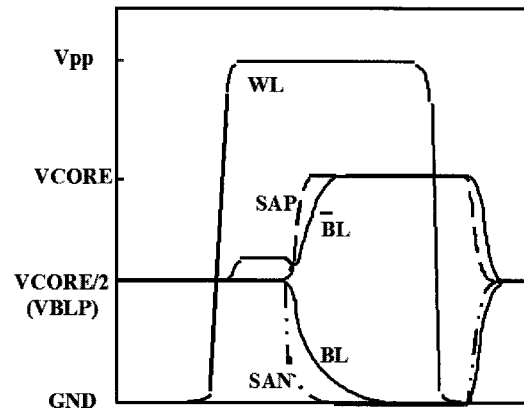


Fig. 5. The timing waveforms of the conventional sensing scheme.

reached on the BL and a large variation of readout voltage  $\alpha$  appears on the SA node pair.

The circuit of conventional or normal sensing scheme is shown in Fig. 4.

In general the low threshold voltage (low  $V_t$ ) transistors are adopted for the n and p-channel amplification. However, with even low  $V_t$  transistors the amplification margin at low VDD voltage of near 1.0V is reduced by the current degradation of n and p-channel devices. The major timing waveforms of the conventional scheme are shown in Fig. 5.

The operation voltage range of the CTPS and conventional sensing scheme is the ground voltage to VDD. The performance upgrade is limited by the way of low  $V_t$  policy in the aspect of process difficulties and sub-threshold leakage current damage. With the mismatches in the threshold voltage of YI gates and an

asymmetric resistance model, the CTPS and the conventional sensing scheme suffer from BL flipping when the sensing-to-YI delay is below about a few nano-seconds.

### III. NEGATIVELY DRIVEN SENSING (NDS) AND FREE-LEVEL PRECHARGED BITLINE (FLPB) SCHEME

To improve low sense margin at low voltage, we propose a negatively driven sensing (NDS) scheme. The circuit of the proposed NDS scheme is shown in Fig. 6. The BL of cell array and SA\_BL of sense-amplifier (S/A) are isolated by transfer-gate of BISH and BISL of PMOS transistors. The n-channel and p-channel amplifications are controlled by SAN and SAP, respectively. The data-transfer between S/A and data bus of SIO and SIOB is controlled by YI. There are BL equalizing devices controlled by BLEQ\_H and BLEQ\_L, and the second n-channel amplifier controlled by BLPD\_H and BLPD\_L.

The second n-channel amplifiers are optional circuits as shown in Fig. 7. If the WL voltage range is ground to VPP, the low voltage at one BL is ground and the high voltage at the other /BL is VCORE.

In the case of low BL voltage, the low voltage at BL should be ground voltage for refresh property. With below ground voltage at BL, the refresh property may be

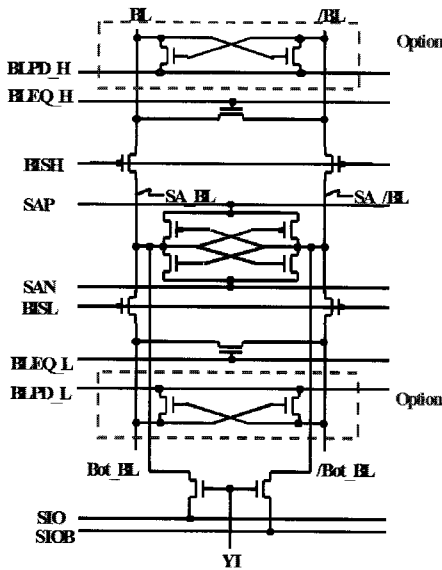


Fig. 6. The circuit details of the proposed NDS scheme with the second n-channel amplifiers.

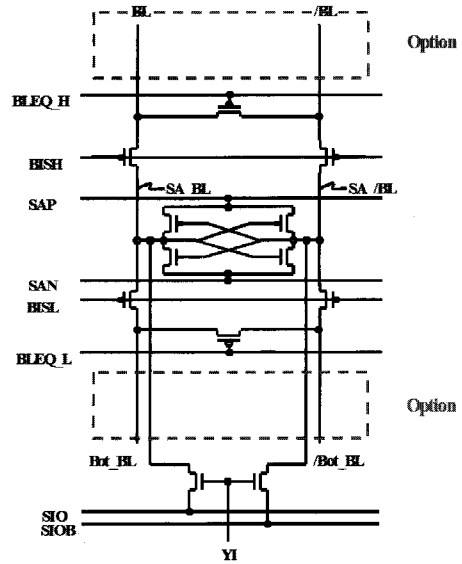


Fig. 7. The circuit details of the proposed NDS scheme without the second n-channel amplifiers.

degraded by the positive gate-to-source sub-threshold bias effect. But if the voltage control at BISH and BISH is adequately adjusted to accurate level for ground level at low BL, the optional circuits can be removed.

Without the second n-channel amplifiers, The circuit of the proposed NDS scheme is more simple than the conventional sense-amplifier.

In DRAM with low BL capacitance, these optional circuits can be removed without performance degradation if the voltage level of BISH or BISH of PMOS switches is well controlled and with negative wordline voltage scheme. The brief operational waveform comparison between the conventional and proposed sense-amplifiers is shown in Fig. 8.

In the circuit of NDS scheme with the optional circuit of the second n-channel amplifiers as shown in Fig. 6, during developing period by sharing cell data with BL, the level of BISH keeps more negative value from the BL precharged level than the threshold voltage of transfer-gate of BISH for sufficient BL sensing-data transfer to SA\_BL node. Before activating the sense-amplifier, the level of BISH turns back to the near threshold voltage of transfer-gate of BISH for the effective separation between the BL and SA\_BL node. Therefore, the sense-amplifier don't see the BL mismatched load at the initial state of sense-amplifier activation. Thus the minimum sensing margin is upgraded to the ideal BL load condition.

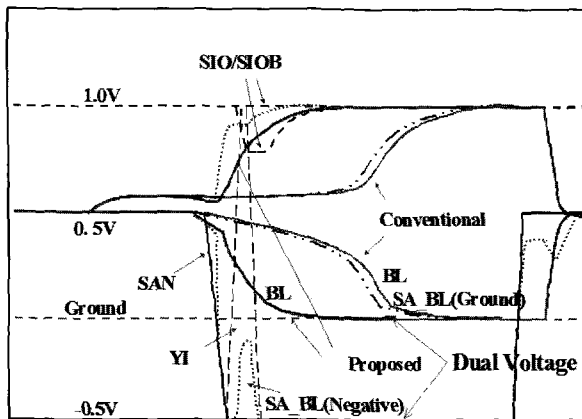


Fig. 8. The operation comparison between the conventional and proposed sense amplifiers.

On the condition of the cell array voltage of sub-1.0V, the speed of the conventional sensing operation is delayed by the amplification current degradation in the voltage range of near threshold voltage of both n-channel and p-channel transistors. On the contrary, there is no performance degradation of the NDS scheme at the S/A nodes of SA\_BL and SA\_/BL. The effective voltage at sense amplifier is still 1.5V with negatively driving voltage of -1.5V at the SAN. While the BL voltage range of cell array is still 0V and 1.0V. Therefore, the BL and sense-amplifier can independently take different dual voltages during the active period, but take same single voltage during the precharge period. The VDD voltage of sub-1.0V in NDS scheme is sufficient for marginal operation with normal thresholds of n and p-channels, which also guarantees the high performance data transfer rate through YI gates. The effective VDD voltage gain of NDS scheme is about 0.5V~0.6V at 1.0 ns pulse width on YI gate when compared with the conventional scheme. The negatively driven SAN node voltage range can be varied according to the properties and performance of n and p channels.

In standby mode, all the row word lines are actively held to ground or negative voltage, while the BLs are ideally held to an intermediate supply voltage known as half VDD in anticipation of a new access. The row-to-column short therefore acts to short half VDD to ground, giving a much higher standby current than is otherwise necessary or desired. Since such short defects cannot be eradicated entirely, large DRAM arrays have resorted to the use of new circuits, which act to limit the amount of supply current that actively holds a BL to half VDD. To

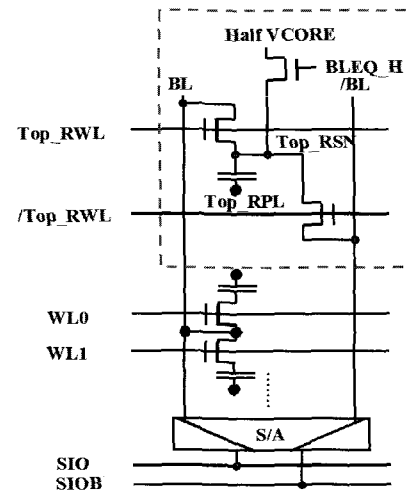


Fig. 9. Free-level precharged bitline (FLPB) scheme.

solve the problem of WL-to-BL short, a variable bitline reference scheme with free-level precharged bitline (FLPB) scheme is adopted as shown in Fig. 9.

In one edge of cell array there is a reference generation scheme with FLPB circuit that is composed of selection control switches. One of BL and /BL is connected to the reference generation circuit through the Top\_RWL or /TOP\_RWL gate control. The reference charge capacitor is the same to the main cell capacitor in size. The bias voltage between two capacitor nodes is zero at the precharge period with the node voltage of half V CORE. The reference charge of Top\_RSN node at half V CORE is shared with the selected one of BL or /BL. Top\_RPL voltage is the same as the main cell common plate voltage of half V CORE. Because there is no current-supply source, the float-state BL voltage levels are different from each column during BL precharge period. However, the developed sensing voltage difference between BL and /BL is always constant by the  $C_s * V_{CORE} / 2(C_s + C_b)$ . Here,  $C_s$  and  $C_b$  are main cell and BL capacitance, respectively. The switches of Top\_RWL and /Top\_RWL are turned off at the precharge period. There are no current sources to the BL and /BL so that the WL to BL short current is prevented at this reference scheme with FLPB circuit. The reference voltages of each column are generated by automatically adjusting to each BL voltage at the precharge period as shown in Fig. 10.

The sensing operation of the FLPB scheme at the precharge level of 0.1V and 0.4V is shown.

The amplified voltages at BLs are ground and

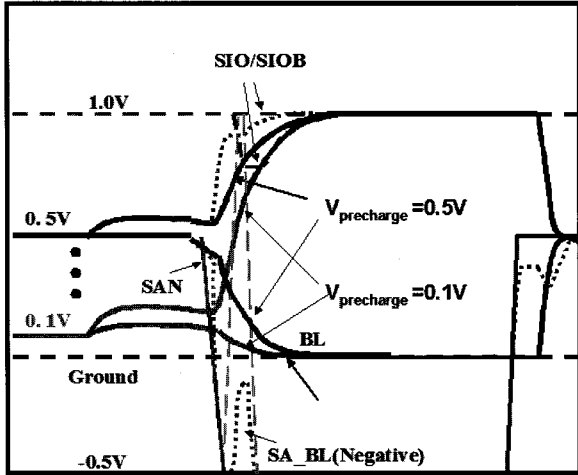


Fig. 10. The generated reference voltages at different BL voltages in free-level precharged bitline (FLPB) scheme.

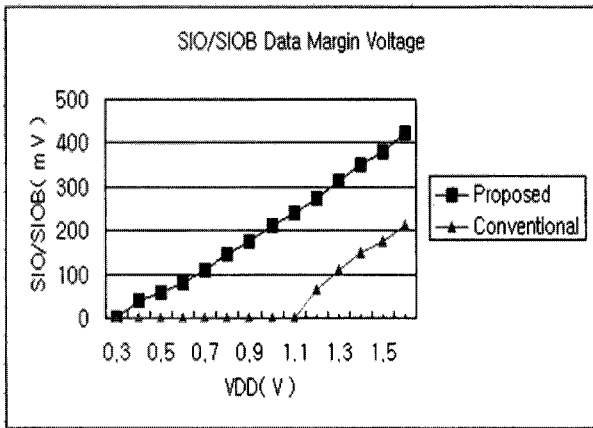


Fig. 11. Data transfer rate through YI gates.

VCORE, the amplified voltages at sense amplifiers are negative and V<sub>core</sub> in NDS scheme.

The data transfer from sense amplifier to data bus is through YI gate. YI gates are composed of NMOS transistor and data bus is precharged with high level. The data transfer type is pull-down current from data bus to sense amplifier. Thus the pull-down transition capability at YI switch is key property for data transfer rates at data bus. At low voltage of sub-1.0V there is little marginal voltage for operation in high NMOS threshold voltage that on-current of YI switch is small.

The BL and SA<sub>BL</sub> can independently take different dual voltages during the active period in NDS scheme. The NDS scheme enables the successful sensing operation at sub-1.0V with normal threshold NMOS of YI and it also guarantees the high data transfer rate through YI gates as shown in Fig. 11.

The effective voltage gain in NDS scheme is about 0.5V~0.6V at 1.0 ns pulse width on YI gate. The negatively driven voltage range can be varied according to the properties of n and p channels.

#### IV. A SENSE AMPLIFIER OFFSET CANCELLATION SCHEME AND MEASURED RESULTS

From the measurement results of the sense amplifier offset voltage distribution of NMOS and PMOS, we learned that the offset threshold voltage distribution of PMOS is around 400mV range, but the offset threshold voltage distribution of NMOS is less 100mV range as shown in Fig. 12 and Fig. 13 shows the simulation results of the PMOS offset voltage ( $V_{tp}$ ) influence in the passed and failed conditions.

Until 200mV range of  $V_{tp}$  offset voltage, the operation result of the sense amplifier is passed. But over 200mV range of  $V_{tp}$  offset voltage, the operation result of the sense amplifier is failed by flip mode. The sensing voltage margin of bitline voltage can not overcome the large  $V_{tp}$  offset voltage of sense amplifier. To overcome the large  $V_{tp}$  offset voltage, one conventional commonly used method is the delayed timing control in the sense amplifier activation, in which NMOS activation is firstly

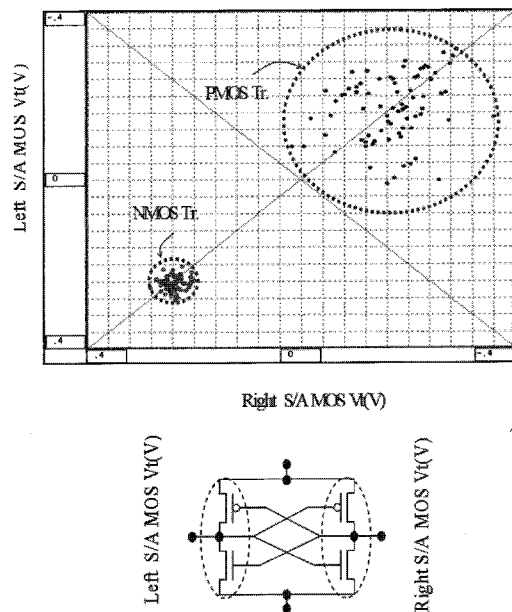


Fig. 12. Threshold voltage characteristics of sense amplifier of NMOS and PMOS.

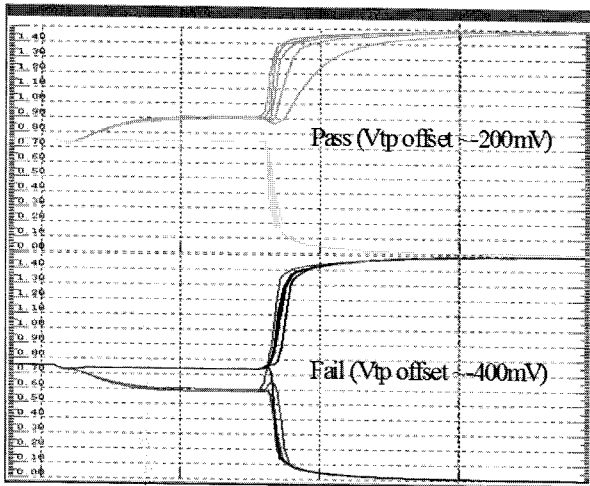


Fig. 13. Flip-failed operation condition of sense amplifier by PMOS threshold voltage offset.

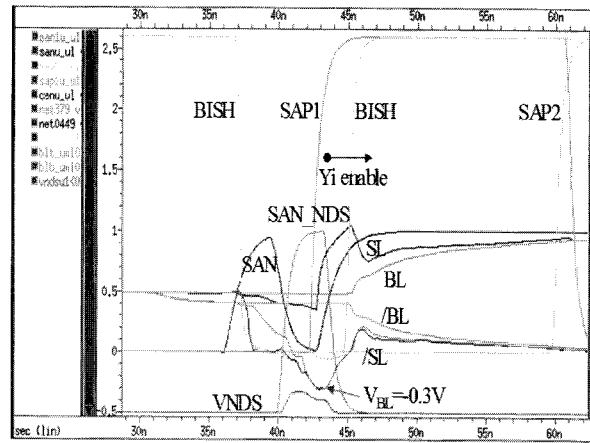


Fig. 16. Operation characteristics of NDS scheme.

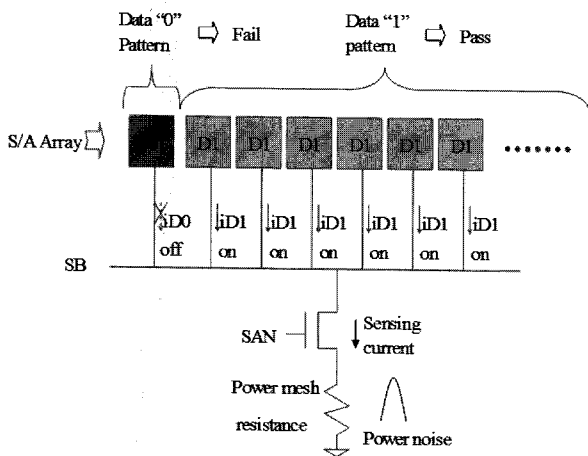


Fig. 14. Worst fail data pattern condition of sense amplifier operation.

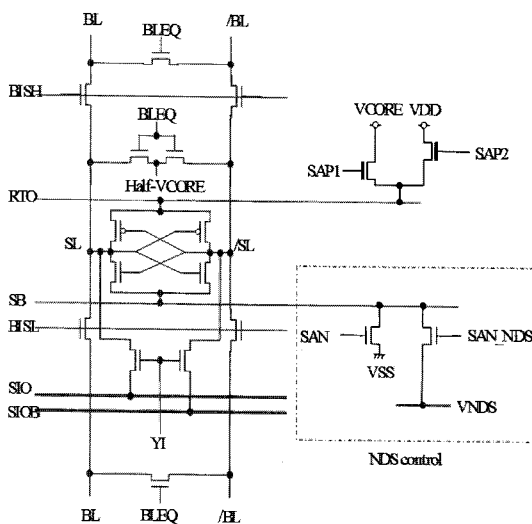


Fig. 15. NDS control scheme.

performed and secondly the PMOS activation is followed. The conventional method is very effective in high voltage operation range, but in low operation voltage the conventional method meets the limit by the ground voltage noise, which is caused by the switching current at activating sense amplifier by power mesh resistance as shown in Fig. 14.

Data "0" is easier to be failed than Data "1". The bitline sensing voltage level of Data "0" is lower than that of Data "1" so that Data "0" is easily affected by the ground voltage noise. NDS scheme is used for removing the affects of the ground voltage noise by using negative voltage source of VNDS and control signal of SAN\_NDS as shown in Fig. 15.

The NDS scheme uses the conventional sense amplifier circuit so that there is no layout change in the sense amplifier array. The only layout change area in core layout region is the sub hole region, in which VNDS power line and NMOS transistor of SAN\_NDS are added. The size of width of SAN\_NDS is about 10% of that of SAN. The detailed operation of NDS scheme is shown in Fig. 16.

The voltage of VNDS is around -0.5V. Vcore voltage is 1.0V and precharge voltage of bitline is 0.5V. SAN control signal changed from single enabled pulse to double enabled pulse. SAN\_NDS control signal is enabled during SAN control signal is disabled. BISH control signal is disabled during the first enable period of SAN and SAN\_NDS. The current consumption of VNDS power generator is mainly from the capacitance of sense amplifier output nodes of SL and /SL. The capacitance of SL and /SL is about 10% of that of BL and /BL. The estimated maximum condition current

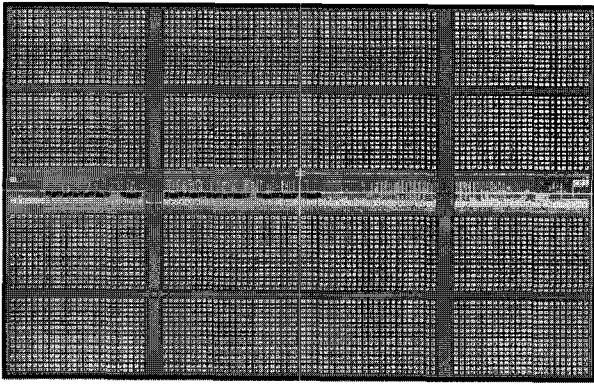


Fig. 17. Chip photo of 1-Gb DDR2 DRAM.

consumption of VNDS is less 5mA in 1-Gb DDR2 DRAM, which is small and acceptable for application. YI of column gate can be enabled after SAPI enabled, which improves the tRCD parameter. The chip photo of the 1-Gb DDR2 DRAM is shown in Fig. 17, which has been evaluated the NDS effects for improving the sensing margin in low voltage and large  $V_{tp}$  offset voltage condition.

## V. CONCLUSIONS

Three novel circuit schemes are proposed to achieve sub 1.0V chip operation, low power consumption, and high performance in DRAM.

Firstly, negatively-driven sensing (NDS) scheme enables sub-1.0V sensing operation without layout area penalty using negative voltage at SA region only.

Secondly, special reference circuit with free-level precharged bitline (FLPB) scheme can remove the standby leakage current of WL-to-BL shortage fail in cell array region.

Finally, the sense amplifier uses NDS offset cancellation control scheme. The performance of the NDS scheme has been verified through its realization on 1-Gb DDR2 DRAM chip.

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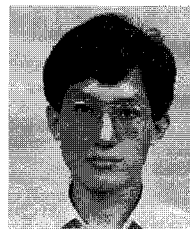
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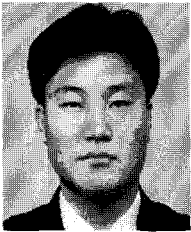
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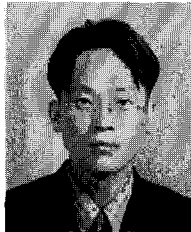
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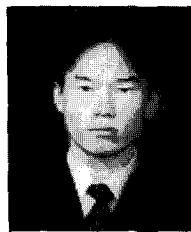




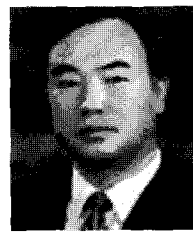
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