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A New PWM-Controlled Quasi-Resonant Converter for a High Efficiency PDP Sustaining Power Module

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ABSTRACT

A new PWM-controlled quasi-resonant converter for a high efficiency PDP sustaining power module is proposed in this paper. The load regulation of the proposed converter can be achieved by controlling the ripple of the resonant voltage across the resonant capacitor with a bi-directional auxiliary circuit, while the main switches are operating at a fixed duty ratio and fixed switching frequency. Hence, the waveforms of the currents can be expected to be optimized from the view-point of conduction loss. Furthermore, the proposed converter has good ZVS capability, simple control circuits, no high voltage ringing problem of rectifier diodes, no DC offset of the magnetizing current and low voltage stresses of power switches. In this paper, operational principles, features of the proposed converter, and analysis and design considerations are presented. Experimental results demonstrate that the output voltage can be controlled well by the auxiliary circuit using the PWM method.

Keywords: Pulse width modulation, Quasi-resonant converter, PDP

1. Introduction

Plasma display panels (PDPs) have been considered as the best candidate for flat panel displays because of their wide viewing angle, high contrast ratio, and long life span. Fig. 1 shows a simplified structure of a PDP with three electrodes. It consists of transparent X and Y sustain electrodes covered with a dielectric layer on the front panel and address electrodes perpendicular to the sustain electrodes on the back panel as shown in Fig. 1. Due to the existence of the dielectric layer, a PDP has a purely capacitive load with respect to circuit operation [1]. Since, it not only features pure capacitive load characteristics but is also driven by the address display separation (ADS) method, the load variation of the sustaining power module is very wide and abrupt in the case of a full-white screen as shown in Fig. 2. In the ADS method, the operation of a PDP can be divided into three periods known as the resetting, addressing, and sustaining periods. Also, the power dissipated by a PDP is the maximum in this case. However, in real PDP TVs, the load condition is strongly dependent on the average pixel level (APL), a concept that defines the total light output of a given TV image as a percentage of the total light output of a full-white image. Since TV signals typically have an APL of 20% or less [4], the sustaining power module is usually operating under light load conditions. Moreover, all PDPs have an automatic power control (APC) system that limits the power consumption to some maximum level by automatically reducing the luminance of the PDP. Thus,

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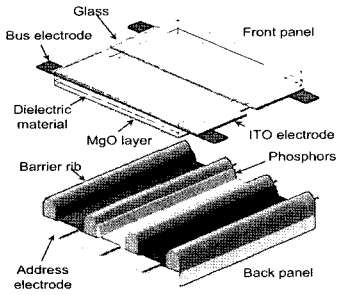

Fig. 1 Simplified structure of PDP with three electrodes

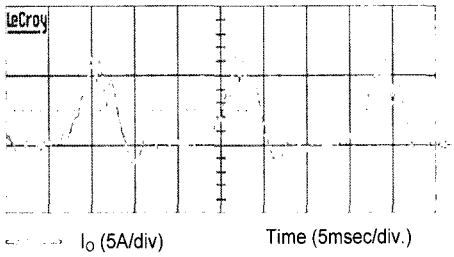

Fig. 2 Load current of sustaining power module

lower power is dissipated even under the full load condition which corresponds to the full-white screen [4]. Although the power dissipated during the sustaining period is less than the maximum power, it is still the highest power driving the PDP compared to that dissipated during the resetting and addressing periods. Therefore, the sustaining power module is mainly responsible for overall system efficiency [1-3]. In addition, when the PDP is operating on TV signals, high efficiency is needed primarily under light load conditions. Up to now, several DC/DC converters which can achieve high efficiency and low cost have been proposed for the sustaining power module of the PDP. Among them, resonant converters have been investigated to achieve the prominent characteristics of miniaturization, high efficiency, and low noise [7-8]. However, since a large variation in switching frequency is needed to control the output voltage, these converters have some difficulties from the view-points of size reduction and noise [9]. To overcome the above problems, recently a half bridge LLC resonant converter has been discussed because it has many unique characteristics and improvements over previous topologies [5-6]. Fig. 3 (a) shows a circuit diagram of a half bridge LLC resonant converter with a voltage doubler rectifier. As shown in this figure, it has a simple structure and low voltage stress on primary power switches. Moreover, since there is no secondary filter inductor, the voltage across the secondary rectifier can be effectively clamped to the output voltage. Employing rectifier diodes with a low voltage rating, the conduction loss can be greatly reduced. Also, its zero-voltage-switching (ZVS) capability is excellent from zero to full load condition [6]. These features make the half bridge LLC resonant converter very suitable for use as a PDP sustaining power module. However, this converter has a small magnetizing inductance in order to have a narrow variation in switching frequency. This results in not only considerably higher circulating energy on the primary side of the transformer, but also in more conduction loss especially in the below resonance mode as shown in Fig. 3 (b). In the case of light load conditions, high circulating energy can be a serious problem that reduces the system efficiency. In addition, a variable frequency control method makes the control circuits much more complicated than those using the pulse width modulation (PWM) control method. To resolve these problems effectively, we propose a new PWM-controlled quasi-resonant converter which has simpler control circuits and less conduction loss compared to a half bridge LLC resonant converter under light load conditions. As shown in Fig. 4, the proposed converter is similar to the half bridge LLC resonant converter except for the auxiliary circuit which is needed to control the output voltage. In the proposed converter, the output voltage can be regulated by controlling the voltage across the resonant capacitor while two main switches are operating at a fixed duty ratio and fixed switching frequency. Therefore, the waveforms of both primary and secondary currents can be expected to be optimized from the view-points of conduction loss and current stress. Simultaneously, since the auxiliary circuit controls some portion of the voltage ripple on the resonant capacitor, the output voltage can be regulated well under whole load conditions. Thus, while keeping the good characteristics of a half bridge LLC resonant converter, the proposed converter is expected to sufficiently overcome the above mentioned problems such as the higher current stress and high circulating energy, and can achive high power density, high performance, and high efficiency.

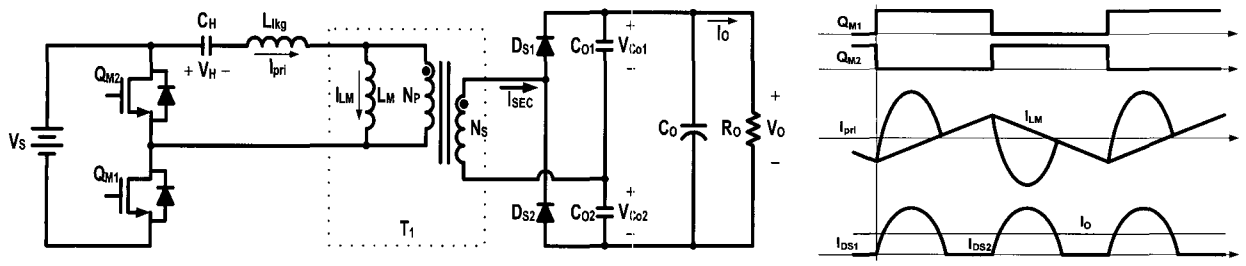

Fig. 3 Half bridge LLC resonant converter with voltage doubler rectifier, (a) Circuit diagram (b) Key waveforms

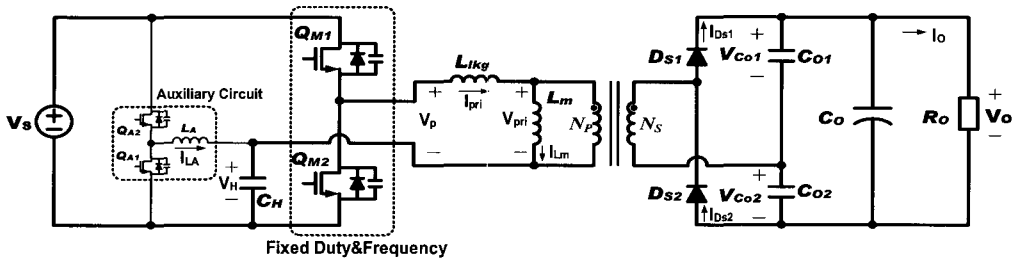

Fig. 4 Circuit diagram of proposed converter

2. Features of the Proposed Converter

Fig. 5 shows a variation of the voltage ripple across the resonant capacitor, C_H, according to load conditions in the half bridge LLC resonant converter which is a frequency controlled converter. As the load is changed from a full load to a light load, the variation of the resonant voltage ripple of C_H gets smaller. This is not only because the change of switching frequency causes the same effect to change the impedance of the resonant tank which is composed of the resonant capacitor and inductor, but also because the amount of the primary current which is reflected to the load current is getting smaller. Thus, in the proposed converter, the bi-directional auxiliary circuit is operating in order to change the resonant voltage ripple using the PWM method while two power switches Q_{M1} and Q_{M2} are operating with a constant duty ratio (D=0.5) and constant switching frequency. Since the load regulation can be achieved by the auxiliary circuit, the magnetizing inductance of the proposed converter is larger than that of the half bridge LLC resonant converter. Thereby, the circulating energy of the proposed converter is considerably reduced under light load conditions. Additionally, due to the operating of Q_{M1} and Q_{M2} with a fixed duty ratio and fixed frequency, the primary current can be optimized from the view-points of conduction loss. Fig. 6 (a) shows the comparison of current waveforms for the proposed converter and the half bridge LLC resonant converter. In each case, the load current is the same as the average value of I_{DS1} because of the capacitive output filter. Therefore, the peak value of I_{DS1} in the proposed converter must be smaller than that of I_{DS1} in the conventional converter under the same load condition. This can be similarly applied to the primary side of the transformer. Thus, to reduce the conduction loss, the waveforms of the current in the proposed converter are very reasonable. On the other hand, the proposed converter employs a voltage doubler type rectifier which has no output inductor. Due to the lack of an output inductor, there is no high voltage ringing across the rectifier diode. Also, by choosing the proper capacitance

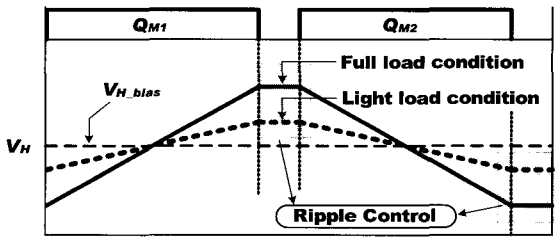

Fig. 5 Variation of voltage ripple across resonant capacitor, C_H according to load conditions

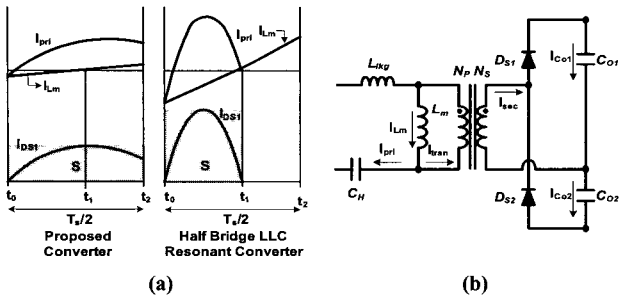

Fig. 6 Simplified waveforms and circuit (a) Comparison of current waveforms (b) Zero DC offset of magnetizing current

of C_{o1} and C_{o2}, the additional resonant voltage ripple of C_{o1} and C_{o2} helps the variation of the resonant voltage ripple of C_H, which is controlled by the auxiliary circuit. Moreover, no DC offsets of the magnetizing current and magnetic flux can be achieved. Considering the DC value of the current through the capacitor is 0A in steady state, the DC values of I_{pri}, I_{Co1}, and I_{Co2} ($<I_{pri}>$, $<I_{Co1}>$, and $<I_{Co2}>$, respectively) are all 0A, where $<\bullet>$ means the DC value of '•'. As shown in Fig. 6 (b), I_{sec} is equal to I_{Co1}-I_{Co2}, $<I_{sec}>=<I_{Co1}>-<I_{Co2}>=0A$. Thus, $<I_{Lm}>=<I_{pri}>+<I_{tran}>=0A$, because $<I_{tran}>=<I_{sec}/n>=0A$. This means that the DC offsets of the transformer magnetizing current and magnetic flux are completely blocked. Therefore, the transformer magnetic core is fully utilized, and its power density can be considerably increased while the heat generation of the transformer can be greatly reduced. Also, the control circuits which generate the gate signals for all power switches, can be easily implemented by using TL494.

3. Operational Principles

Fig. 7 shows the key waveforms of the proposed converter. The operation of the proposed converter can be divided into ten modes. One switching cycle of the proposed circuit is divided into two half cycles, t_0~t_5 and t_5~t_{10}. Since the operational principles of two half cycles are symmetric, only the first half cycle is explained. A half cycle can be divided into 5 modes and its equivalent circuits are shown in Fig. 8. The switches of Q_{M1} and Q_{M2} are turned on and off alternately with a constant duty ratio (D=0.5) and constant frequency. And the auxiliary switches such as Q_{A1} and Q_{A2} are turned on and off in duty cycle and controlled, where $D_E T_S$ is the operational conduction time of the auxiliary switches. To illustrate the steady state operation, several assumptions are made as follows:

- The power switches such as Q_{M1}, Q_{M2}, Q_{A1}, and Q_{A2} are ideal except for their internal diodes and output capacitors, C_{oss}.
- The rectifier diodes D_{S1} and D_{S2} are ideal except for their junction capacitors, C_j.
- The output voltage V_o is constant during a switching period.

Mode 1 (t_0~t_1): After the ZVS turned on, the Q_{M1} is achieved and the commutation between D_{S1} and D_{S2} is completed, Mode 1 begins. The primary current I_{pri}, which rises with resonance between the leakage inductor and resonant capacitor, is given by

$$I_{pri}(t)=\frac{1}{nZo}\left[\frac{V_S}{n}-\frac{V_H(t_0)}{n}-V_{Co1}(t_0)\right]\sin\omega_r(t-t_1)+I_{Lm}(t) \quad (1)$$

Concurrently, the magnetizing current, I_{Lm}, also rises with the resonance between the magnetizing inductor L_m, and rectifier capacitors $C_{o1}//C_{o2}$. On the other hand, since the resonant frequency, f_m, determined by L_m and $C_{o1}//C_{o2}$, is

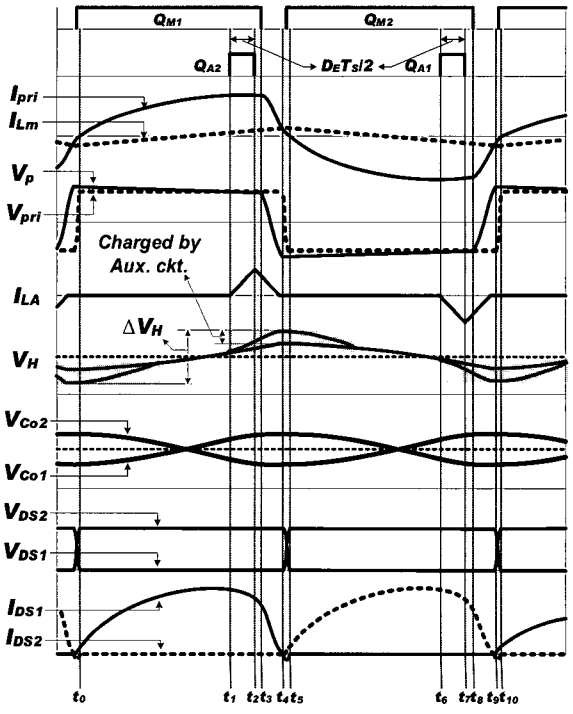

Fig. 7 Key waveforms of proposed converter

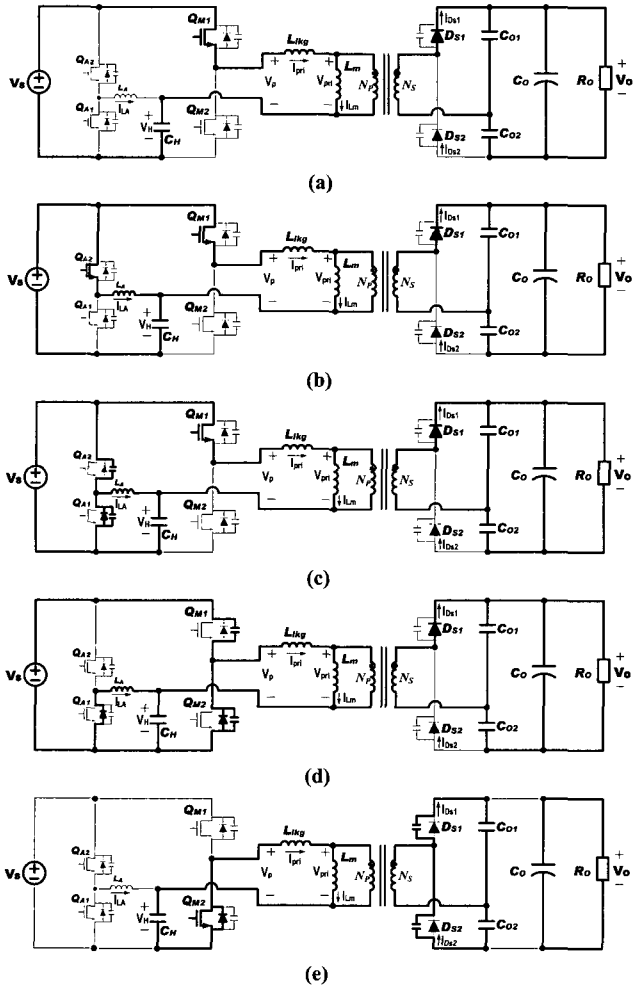

Fig. 8 Equivalent circuits of proposed converter, (a) Mode 1 (b) Mode 2 (c) Mode 3 (d) Mode 4 (e) Mode 5

much slower than the switching frequency, I_{Lm} can be linearly approximated as follows:

$$I_{Lm}(t) = I_{Lm}(t_1) + \frac{nV_{Co1}(t)}{L_m}(t - t_1). \quad (2)$$

$$where,\ \omega_r = \frac{1}{\sqrt{L_r C_r}},\ Z_o = \sqrt{\frac{L_r}{C_r}},\ L_r = \frac{L_{lkg}}{n^2},\ C_r = \frac{n^2 C_H \times C_{o1}//C_{o2}}{n^2 C_H + C_{o1}//C_{o2}},\ n = \frac{N_p}{N_s}.$$

The current of the rectifier diode D_{S1}, I_{DS1}, flows through C_{o1} and the equivalent load resistor, while the rectifier capacitor C_{o1} and C_{o2} is charged and discharged respectively.

Mode 2 (t_1~t_2): When Q_{A2} is turned on, mode 2 begins. During this mode, the resonant capacitor, C_H, is additionally charged from the input source, V_S, through the auxiliary inductor L_A operating in discontinuous conduction mode (DCM). It is assumed that L_A is large enough to approximate I_{LA} which is increased and decreased linearly. The slope of I_{LA} can be obtained as follows:

$$\frac{dI_{LA}(t)}{dt} = \frac{V_S - V_H(t)}{L_A}. \quad (3)$$

The primary and secondary side of the transformer operates similarly to Mode 1.

Mode 3 (t_2~t_3): After Q_{A2} is turned off, I_{LA} starts to charge and discharge the output capacitors, Q_{A2} and Q_{A1} , respectively. When the voltage across Q_{A1} becomes 0V, I_{LA} begins to flow through the internal diode of Q_{A1}. Since the voltage across the C_H, V_H is applied to L_A oppositely, I_{LA} is decreased. During this interval, C_H is still charged and both of the transformer sides operate similarly to mode 1.

Mode 4 (t_3~t_4): When Q_{M1} is turned off, mode 4 begins. Since I_{pri} starts to charge and discharge the output capacitors of Q_{M1} and Q_{M2} respectively, the voltage across the primary side of the transformer V_P, is decreased to $-V_S$. Since the rectifier diode D_{S1} is still conducting, the voltage across L_m, V_{pri} is maintained to be nV_{Co1}. Thus, the negative voltage which is the same as the difference between V_P and V_{pri}, is applied to the leakage inductor, L_{lkg}. Thereby, I_{pri} is decreased rapidly. Also, in this interval, C_H is continuously charged until I_{LA} becomes 0A. After the voltage across Q_{M2} becomes 0V, I_{pri} starts to flow through the internal diode of Q_{M2}. Thus, the ZVS condition of Q_{M2} is satisfied. Mode 4 is finished when $I_{pri}$is equal to I_{Lm}.

Mode 5 (t_4~t_5): When I_{pri} is smaller than I_{Lm}, the current of the secondary side of the transformer flows

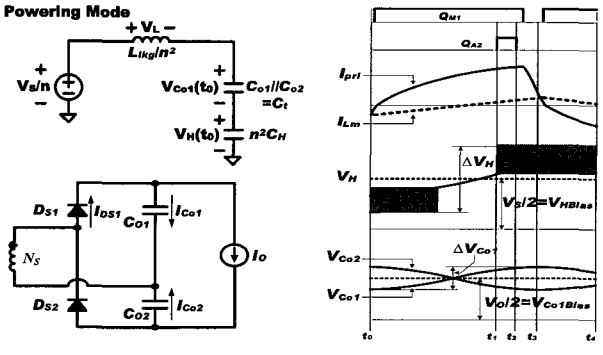

Fig. 9 Powering Mode, (a) Equivalent circuits (b) Key waveforms

oppositely through the junction capacitors, D_{S1} and D_{S2}. Since the voltage across each diode is increased and decreased respectively, the commutation between D_{S1} and D_{S2} is started. During this mode, the ZVS turned on for the Q_{M2} can be achieved. After D_{S2} is fully conducting, mode 5 is finished.

The circuit operation of t_5~t_{10} is similar to that of t_0~t_5. Subsequently, the operation from t_0 to t_{10} is repeated.

4. Analysis & Design Considerations

4.1 Variations of V_{Co1}, V_{Co2}, and V_H

Fig. 9 shows the equivalent circuit and its key waveforms for the analysis. Since both the time duration of t_2~t_3 and the dead time are much smaller than the switching period T_S, they can be discarded for simplicity of analysis. During the half switching period $T_S/2$, the charging current of C_{o1} is equal to the load current I_O. This is because C_{o1} must supply as much as I_O during the last half of the switching period. In addition, since the sum of V_{Co1} and V_{Co2} is always equal to the output voltage V_O, the bias voltage of V_{Co1} and V_{Co2} is $V_O/2$ as shown in Fig. 9 (b). Thus, by using the equation $I_C=C(dV_C/dt)$, $V_{Co1}(t_0)$ can be obtained as follows:

$$dV_{Co1}(t)=\frac{1}{C_{o1}}\int I_{Co1}(\tau)d\tau=\frac{TsIo}{2C_{o1}}, \tag{4}$$

$$where,\ \frac{2}{Ts}\int I_{Co1}(\tau)d\tau=Io.$$

$$V_{Co1}(t_0)=\frac{Vo}{2}-\frac{TsIo}{4C_{o1}}. \tag{5}$$

Similarly $V_{Co2}(t_0)$ can be obtained as follows:

$$V_{Co2}(t_0)=\frac{Vo}{2}+\frac{TsIo}{4C_{o2}}. \tag{6}$$

As mentioned previously, since both Q_{M1} and Q_{M2} are operating with the constant duty ratio (D=0.5), the bias voltage of V_H is the same as $V_S/2$. Thus, $V_H(t_0)$ can be represented as follows:

$$V_H(t_0)=\frac{V_S}{2}-\frac{\Delta V_H}{2}. \tag{7}$$

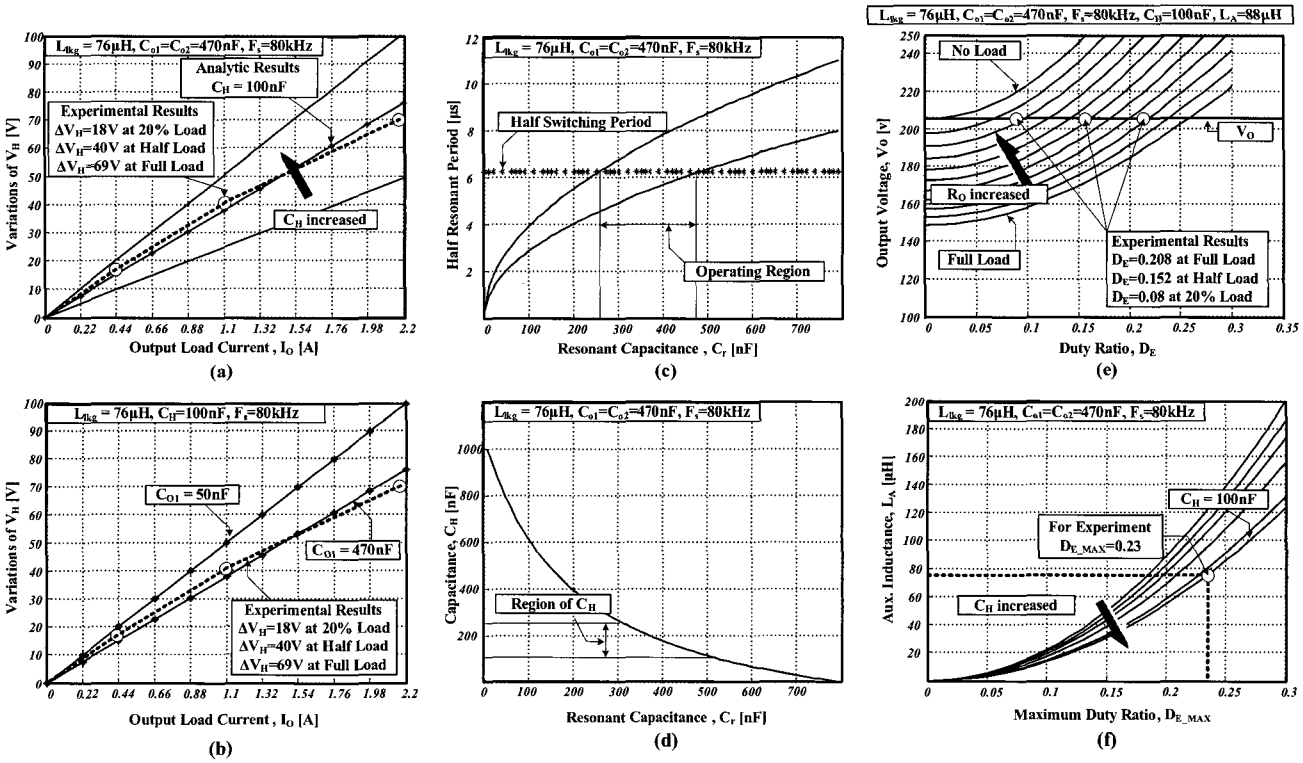

Fig. 10 Figures for analysis,

(a) V_H according to load with different C_H (b) V_H according to load with different C_{o1} and C_{o2}

(c) Desirable region of resonant frequency (d) Selection of C_H

(e) Output voltage according to duty ratio D_E with different load (f) Selection of L_A and maximum duty ratio D_{E_MAX}

4.2 Turns Ratio of the Transformer and Load Current

By using the equations (5) and (7), the current through D_{S1}, I_{DS1} can be easily obtained from the equivalent circuit as shown in Fig. 9 (a) as follows:

$$I_{DS1}(t)=\frac{1}{Zo}\left[\frac{Vs}{n}-\frac{1}{n}\left(\frac{Vs}{2}-\frac{\Delta V_H}{2}\right)-\left(\frac{Vo}{2}-\frac{TsIo}{4C_{o1}}\right)\right]\sin\omega_r t \quad (8)$$

The turn ratio of the transformer can be determined under no load in order to maintain V_O at the desired value without the operation of the auxiliary circuit. Thus, it can be obtained by using the equation (8) with the following conditions I_O=0A, I_{DS1}=0A, ΔV_H=0V, and $\sin\omega_r t \neq 0$.

$$n=\frac{Vs}{Vo}. \quad (9)$$

Since both the charging current of C_{o1} and the discharging current of C_{o2} flow through D_{S1}, the average value of I_{DS1} during $T_S/2$ is equal to two times I_O. From this fact, I_O can be represented as follows:

$$Io=\left[\frac{Vs}{n}-\frac{1}{n}\left(\frac{Vs}{2}-\frac{\Delta V_H}{2}\right)-\left(\frac{Vo}{2}-\frac{TsIo}{4C_{o1}}\right)\right]\times\frac{1}{ZoTs\omega_r}\left[1-\cos\left(\frac{Ts\omega_r}{2}\right)\right]. \quad (10)$$

From the equation (10), ΔV_H can be expressed as the following equation.

$$\Delta V_H=2n\frac{IoZoTs\omega_r}{1-\cos(Ts\omega_r/2)}-2n\left(\frac{Vs}{2n}-\frac{Vo}{2}+\frac{TsIo}{4C_{o1}}\right) \quad (11)$$

As shown in Fig. 10 (a) and (b), $\Delta V_H/2$ can be plotted by using the equation (11) according to I_O under different conditions. Fig. 10 (a) shows $\Delta V_H/2$ with a fixed value of C_{o1} and C_{o2} while C_H is varied. Similarly, Fig. 10 (b) shows it with a fixed value of C_H while C_{o1} and C_{o2} are varied. As can be seen in these figures, to regulate the output voltage according to load conditions, $\Delta V_H/2$ gets larger as the load approaches a full load.

4.3 Resonant Frequency vs. Switching Frequency

As mentioned above, the waveform of I_{pri} should be similar to that of the proposed converter as shown in Fig. 6 (a) so as to reduce the conduction loss. Therefore, the resonant frequency, which is decided by the resonant inductance and capacitance, should be selected according to the switching frequency. Fig. 10 (c) shows the desirable region of resonant frequency when the switching frequency is fixed as 80kHz. To be optimized about the conduction loss, the resonant frequency should be selected within the operating region. After the resonant frequency is selected, C_H can be decided with the resonant inductance 76μH, as shown in Fig. 10 (d). Also, the values of C_{o1} and C_{o2} can be obtained properly by using the equation (11) and Fig. 10 (a) and (b).

4.4 DC conversion ratio and Maximum duty ratio according to auxiliary inductor, L_A

ΔV_H, which is controlled by the auxiliary circuit, can be obtained in a similar way as mentioned in 4.1.

$$\Delta V_H=\frac{1}{C_H L_A}\left[\frac{Vs}{2}-\frac{TsIo}{2nC_H}\right](T_sD_E)^2. \quad (12)$$

From equations (10) and (12), the steady state voltage conversion ratio of the overall system can be derived as follows:

$$\frac{Vo}{Vs}=\frac{\frac{1}{2}+\frac{(T_sD_E)^2}{4C_HL_A}}{\frac{T_S}{Ro}\left[\frac{nZo\omega_r}{1-\cos(Ts\omega_r/2)}-\frac{n}{4C_{o1}}+\frac{(T_sD_E)^2}{2C_HL_A}\right]+\frac{n}{2}} \quad (13)$$

Using equation (13), the output voltage can be plotted as shown in Fig. 10 (e). In this figure, the output voltage can be obtained without the operation of the auxiliary circuit

Table 1 Parameters of prototype circuit

Item	Symbol	Value/Part
Input Voltage	V_{in}	390~410V
Output Voltage	V_O	205V
Max. Power Rating	P_{max}	451W
Switching Frequency	F_s	80kHz
Turn Ratio	n:1	1.96:1
Leakage inductance	L_{lkg}	76uH
Magnetizing inductance	L_m	1.2mH
Capacitance of half bridge	C_H	100nF
Capacitance of doubler cell	C_{o1},C_{o2}	470nF
Output Capacitance	C_o	680uF/250V
Main Power Switches	Q_{M1}, Q_{M2}	IRFPC60
Auxiliary Power Switches	Q_{A1}, Q_{A2}	FQP2N60
Auxiliary Inductor	L_A	88uH
Rectifier Diodes	D_{S1}, D_{S2}	15ETH03

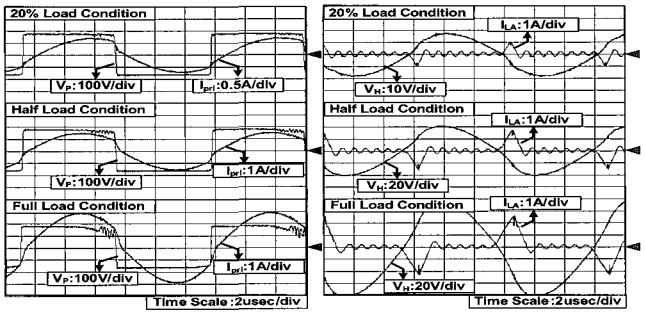

Fig. 11 Experimental waveforms at 20%, half, and full load, (a) V_P and I_{pri} (b) V_H and I_{LA}

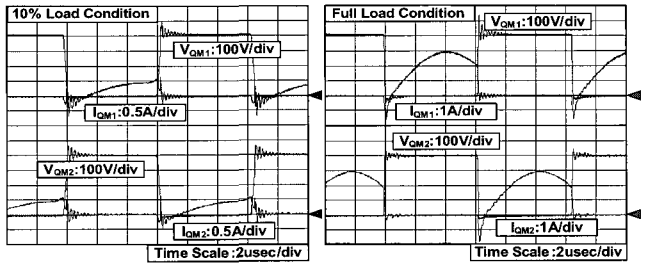

Fig. 12 ZVS of Q_{M1} and Q_{M2}, (a) At 10% load (b) At full load

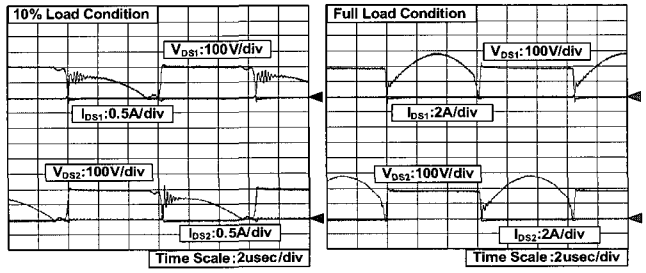

Fig. 13 ZCS of D_{S1} and D_{S2}, (a) At 10% load (b) At full load

under no load (D_E=0). As the load approaches a full load, D_E is increased to get the desired output voltage. From this figure, the output voltage can be regulated well under a full load condition by the auxiliary circuit. Fig. 10 (f) shows the proper auxiliary inductance needed to achieve the load regulation according to the maximum duty ratio $D_{E\text{-}MAX}$. As shown in this figure, when L_A is selected as the larger value to reduce the peak value of I_{LA}, the larger maximum duty ratio is needed.

5. Experimental Results

A 450W prototype of the proposed converter has been built for the experiment. The parameters of this prototype circuit are listed in Table 1. Fig. 11 shows the experimental waveforms at 20%, half, and full load. As can be seen in Fig. 11 (a), the waveform of I_{pri} is similar to that above resonance mode. This results in less conduction loss and lower peak values of I_{pri}, I_{DS1}, and I_{DS2}. Fig. 11 (b) shows V_H and I_{LA} at each load. As can be seen in this figure, C_H is additionally charged or discharged by I_{LA} to regulate the output voltage. The ZVS operation of Q_{M1} and Q_{M2} at 10% and full load is shown in Fig. 12. In order to have the waveforms of current in BRM, the leakage inductance is rather large compared with that of the half bridge LLC resonant converter. Due to the large leakage inductance, the ZVS operation of Q_{M1} and Q_{M2} is easily achieved even at 10% load as shown in Fig. 12. Fig. 13 shows the ZCS operation of D_{S1} and D_{S2}. Also, in this figure, the voltage across the D_{S1} and D_{S2} can be clamped to the output voltage without high voltage ringing.

6. Conclusions

A new PWM-controlled quasi-resonant converter for a high efficiency PDP sustaining power module is proposed in this paper. Since the load regulation of the proposed converter can be achieved by an auxiliary circuit, the waveforms of the current can be optimized from the view-points of the conduction loss especially under light load conditions. Moreover, by employing a voltage doubler type rectifier, additional resonant ripple of the voltage across the rectifier capacitors helps the operation of the auxiliary circuit. Besides, DC offsets of the magnetizing current and magnetic flux can be completely blocked. From the experimental results, good ZVS capability of the power switches Q_{M1} and Q_{M2} is also proven. A prototype was used in experiments to prove the validity of the proposed converter. Fig. 14 shows the measured efficiency. The measured efficiency within the 10%~40% load range is higher than that of the half bridge LLC resonant converter. As mentioned in the introduction, when the PDP is operating on TV signals, the sustaining power module is usually operating under light load conditions. Thus, the proposed converter is expected to be suitable for the sustaining power module of the PDP. On the other hand, the measured efficiency is decreased as the

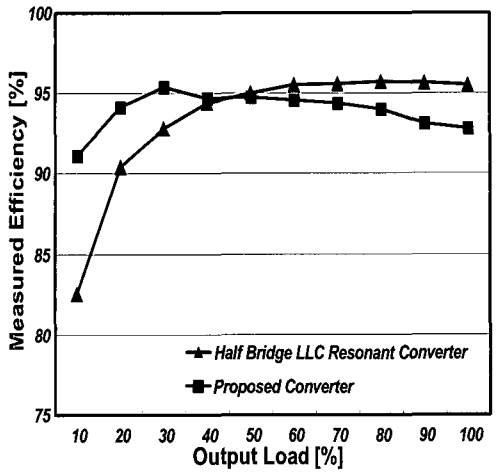

Fig. 14 Measured Efficiency

load approaches a full load. This is because the power dissipated by the auxiliary circuit is increased. However, the measured efficiency along wide load ranges shows as high as 94%. Therefore, the proposed converter demonstrates its suitability as a sustaining power module owing to its simple control circuits, low noise, and high efficiency.

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