High performance of ZnO thin film transistors using SiN$_x$ and organic PVP gate dielectrics

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Abstract The device performance of ZnO-thin film transistors (ZnO-TFTs) with gate dielectrics of SiO$_2$, SiN$_x$ and Poly-vinylphenol (PVP) having a bottom gate configuration were investigated. ZnO-TFTs can induce high device performance with low intrinsic carrier concentration of ZnO only by controlling gas flow rates without additional doping or annealing processes. The field effect mobility and on/off ratio of ZnO-TFTs with SiN$_x$ were 20.2 cm^{2}V^{-1}s^{-1} and 5×10^6, respectively, which is higher than those previously reported. The device adoptable values of the mobility of 1.37 cm^{2}V^{-1}s^{-1} and the on/off ratio of 6×10^3 were evaluated from the device with organic PVP dielectric.

Key words ZnO, ZnO-TFTs, Gate dielectrics, Field effect mobility, On/off ratio, Organic insulator

1. Introduction

ZnO thin film has attracted remarkable attention because of its optically transparent property with a wide band gap of 3.36 eV and polycrystalline growth at room temperature [1-4]. ZnO thin-film transistors (TFTs) are known as a strong candidate to substitute for α-Si : H transistors and organic thin-film transistors (OTFT) in transparent electronics, opto-electronics, and flexible electronics. Though grown at room temperature, poly-crystalline ZnO film can offer low processing cost and good compatibility with flexible plastic substrates [5, 6]. However, the ZnO-TFTs have not yet been applied to industry due to its lower field effect mobility, lower on/off ratio, and inadequate threshold voltage. These problems result from leaky dielectric, traps at the interface between ZnO gate dielectric, and Zn diffusion into the dielectric. As a solution for dielectric materials, high-k dielectric or double layer dielectrics have been suggested [7-11]. In spite of numerous endeavors, the ZnO-TFTs with sufficient device characteristics have not yet been reported. In addition, the non-leaky gate dielectric grown at a low temperature process is strongly needed for application to plastic substrates. Field-effect devices with organic channel on poly-4-vinylphenol (PVP), such as OTFT, appeared to have some potentials for exhibiting decent mobility but these are still inferior to devices

with inorganic semiconductor in many aspects of device performance [12, 13]. Low temperature processed ZnO-TFTs with polymer gate dielectric layer are meaningful for the application to flexible devices with plastic substrate.

In this study, we investigated the device characteristics of ZnO-TFTs with respective gate dielectrics of SiO$_2$, SiN$_x$, and PVP layer. To enhance device performance, the carrier concentration of ZnO active channel was varied only by controlling the Ar and O$_2$ gas flow rates. The device characteristics of un-doped and controlled ZnO-TFTs with adoptable inorganic and organic gate dielectrics will be discussed and compared with those previously reported [1, 6-8].

2. Experimental

The bottom gate and top contact-type ZnO-TFTs were fabricated on glass substrates. Gate dielectrics of SiO$_2$, SiN$_x$, and PVP were formed on ITO/corning 1737 glass, respectively. A 100 nm SiO$_2$ dielectric was deposited with SiH$_4$ and N$_2$O by inductively coupled plasma-chemical vapor deposition (ICP-CVD) system at 270°C. A 150 nm SiN$_x$ film was deposited with SiH$_4$, NH$_3$, and N$_2$ gases by plasma enhanced chemical vapor deposition (PECVD) system at 320°C. A 480 nm PVP dielectric was spin-coated on the isopropanol-cleaned ITO substrate at room temperature and cross-linked at 175°C for 1 hour in vacuum. Here, the PVP solution consisted of commercial PVP solution and cross-linking agent of

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polymelamine-co-formaldehyde in propylene glycol mono-methyl ether acetate.

Next, ZnO films with a thickness of 100 nm as an active channel layer were deposited at an optimized condition by RF magnetron sputtering at room temperature. For the optimized ZnO film, $O_2/Ar + O_2$ ratio varied from 0 to 1. Finally, the source and drain of a 100nm ITO grown by RF magnetron sputter at room temperature were patterned by a lift-off method for SiO_2 and SiN_x dielectrics and with a shadow mask for the PVP dielectric.

ZnO films grown at optimized deposition conditions were characterized by field emission scanning electron microscopy (FE-SEM), X-ray diffraction (XRD), and Hall measurement. Fabricated ZnO-TFTs were electrically characterized by Agilent 4155 semiconductor parameter analyzer at room temperature.

3. Results and Discussion

Figure 1 shows an XRD pattern from the ZnO film grown on glass substrate. A strong peak corresponding to (002) plane of the hexagonal ZnO structure was observed at 34.16°, indicating that the ZnO film grows with the c-axis orientation. The crystallinity of the film was evaluated from XRD θ-rocking curve of (002) plane and its full width at half maximum (FWHM) for ZnO (002) was about 0.49. This result suggests that this film contains hardly any impurities or the least amount of point defects. The poly-crystalline ZnO film has a distribution of grain size ranging from 20 to 50 nm, as shown from the top view SEM image in the inset. The
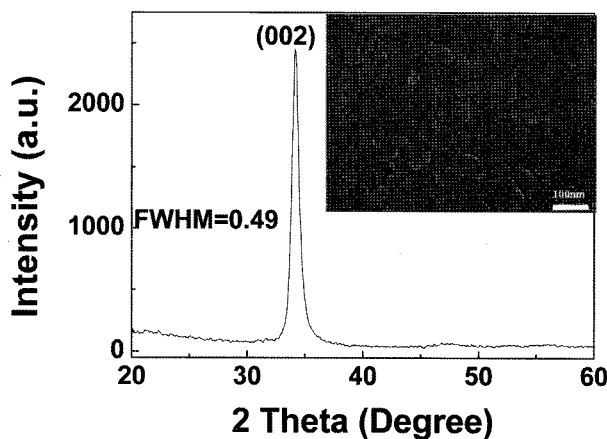

Fig. 1. X-ray diffraction pattern of the ZnO thin film as a channel layer for the ZnO TFTs and SEM image of the as-deposited ZnO thin film.

surface was very smooth with a root mean square (RMS) of 4.14 nm in the contacting mode over a scale of $2 \times 2 \ \mu m^2$. In order to choose the appropriate ZnO as an active channel layer, the background electron concentration must be reduced to increase the carrier mobility [14]. Thus, for the ZnO film with low carrier con- centration and high resistivity, the deposition was controlled with gas flow rates of Ar and O_2 during the film growth process. It was found that only the pure argon supplement was effective for high device performance as an optimized sputtering environment. This agrees with the results that oxygen is most likely connected with charged particles upon substrate impaction during the sputtering [14]. These optimized ZnO films had a carrier concentration of $10^{12}\sim10^{14} \ cm^{-3}$ and showed n-type behaviors. The corresponding ranges of resistivity and carrier mobility of this ZnO film were $10^4\sim10^6 \ \Omega cm$ and $10^{-1}\sim10^{-3} \ cm^2V^{-1}s^{-1}$, respectively.

Linear region transfer characteristics (I_{ds}-V_{gs}) of the fabricated ZnO-TFTs with SiO_2, SiN_x, and PVP gate dielectrics were investigated. The drain current of fabricated ZnO-TFTs were measured as a function of the gate voltage (I_{ds}-V_{ds}). It was observed that all of the ZnO-TFTs were n-channel enhancement-mode characteristics, which is preferable to depletion mode for low power displays. The field effect mobility, μ_{FE}, in the linear region was calculated from the equation $g_m = \partial I_{ds}/\partial V_{gs} = m_{FE}C_{ox}(W/L)V_{ds}$, where g_m is the transconductance, C_{ox} is the capacitance per area of the gate insulator, I_{ds} is drain current, V_{gs} is the applied gate to source voltage, V_{ds} is the applied drain to source voltage, and W and L are the channel width and length, respectively. The relative dielectric constants evaluated from the capacitance-voltage curve of SiO_2, SiN_x, and PVP were 3.9, 6.0, and 4.2, respectively.

Figure 2(a) represents the transfer curve of I_{ds} vs. V_{gs} at V_{ds} of 3 V fabricated using SiO_2 dielectrics. The values of μ_{FE} and I_{on}/I_{off} were 1.8 $cm^2V^{-1}s^{-1}$ and 8×10^4. The threshold voltage (V_{th}) was calculated by fitting a straight line to the plot of the square root of I_{ds} vs. V_{gs}, and then evaluated at 7.5 V. Figure 2(b) shows a high source to drain current of above 4×10^{-6} A at an applied gate bias of 15 V and a low drain current of 2×10^{-9} A. Though deposited at room temperature, the ZnO film showed higher performance than previous reports because of the lower carrier concentration of ZnO film [6]. The transfer characteristics of fabricated ZnO-TFTs with SiN_x gate dielectric at $V_{ds} = 4$ V are shown in Fig. 2(c). To measure a source to drain current as a function of the gate voltage, the gate bias was applied at a range between
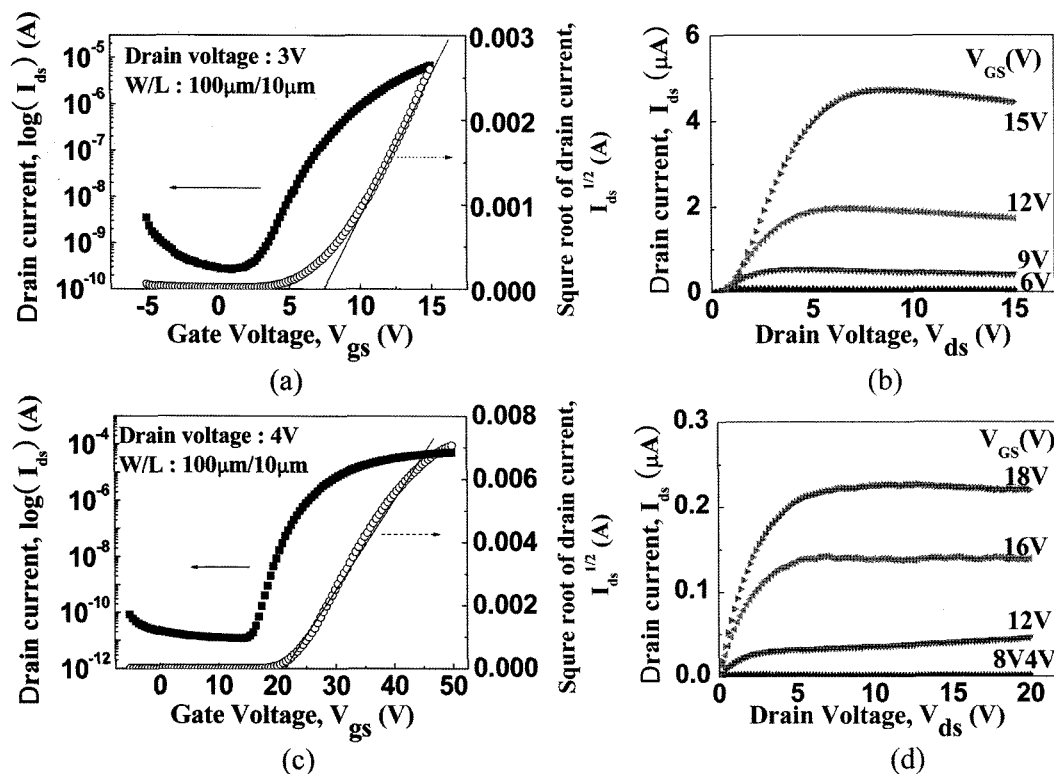
Fig. 2. Device characteristics of ZnO TFTs with inorganic gate insulators. (a) Transfer characteristics (I_{ds}-V_{gs}) of various ZnO-TFTs with the SiO$_2$ gate insulator layer at V_{ds} = 3V. (b) The drain current with a variation of gate voltages from ZnO-TFTs with the SiO$_2$ gate insulator. (c) Transfer characteristics (I_{ds}-V_{gs}) of various ZnO-TFTs with the SiN$_x$ gate insulator layer at V_{ds} = 4. (d) The drain current with a variation of gate voltages from ZnO-TFTs with the SiN$_x$ gate insulator.

−5 V and 50 V. The values of μ_{FE} and V_{th} in the linear region (V_{ds} = 4 V) were calculated to be 20.2 cm^{2}V^{-1}s^{-1} and 22 V, respectively. It was also observed that the ZnO-TFT has n-channel, since electrons are generated by the positive voltage (V_{gs}). In Fig. 2(d), we obtained a high source to drain current of above 2 × 10^{-7} A at an applied gate bias of 18 V and a low drain current of about 2 × 10^{-11} A. In ZnO-TFTs with SiN$_x$ layer, the on/ off ratio and the field effect mobility dramatically increased, as compared with that of the ZnO-TFTs on the SiO$_2$ layer. The off-state current of the SiN$_x$ layer was 2 orders of magnitude lower than that of the SiO$_2$. The high μ_{FE} of ZnO-TFT with SiN$_x$ gate dielectric can be resulted from not only the high quality of gate dielectric, but also the good dielectric-channel interface. Depositing ZnO on a SiO$_2$ layer caused diffusion of Zn into the SiO$_2$ layer, thus degrading the insulating properties of the SiO$_2$ layer [7]. The value of μ_{FE} in un-doped ZnO TFTs with SiN$_x$ dielectric is 20.2 cm^{2}V^{-1}s^{-1}, which is higher than the other previous results of 0.2~7 cm^{2}V^{-1}s^{-1} [1, 8]. The usual carrier concentration of un-doped ZnO is above 10^{16} cm^{-3} [6, 7]. However, the lower intrinsic carrier concentration of 10^{12}~10^{14} cm^{-3} in this study may lead to the higher mobility of ZnO-TFTs with SiO$_2$ and

SiN$_x$ dielectrics.

On the other hand, the performance improvement of ZnO-TFTs with SiNx is related to the gate insulator-ZnO semiconductor interface, the high quality crystallinity, low oxygen vacancies and/or Zn interstitials working as donors [15]. The issue of Zn penetration through the gate dielectric in ZnO-TFTs, which alters the device properties in an unwanted way, is a significant concern for device integration. In solution of these problems, SiN$_x$ layer is effective to prevent Zn diffusion into the insulating layer [7].

Figure 3(a) represents the transfer curve of I_{ds} vs. V_{gs} at V_{ds} of 40 V fabricated using PVP organic gate dielectric. Because the source-drain was formed by shadow mask process, W/L ratio of the transistor is smaller than previously discussed ZnO-TFTs with inorganic gate dielectric in this study. The electrical characteristics of μ_{FE}, V_{th}, and the I_{on}/I_{off} ratio were obtained 1.37 cm^{2}V^{-1}s^{-1}, 17.5 V, and 6 × 10^3, respectively. Figure 3(b) shows the source to drain current of about 9 × 10^{-7} A at applied gate bias of 40 V. ZnO-TFTs with PVP organic gate dielectric revealed much poor device performance such as lower I_{on}/I_{off} ratio and μ_{FE}, high operating voltage, compared with those with inorganic gate dielectrics. In
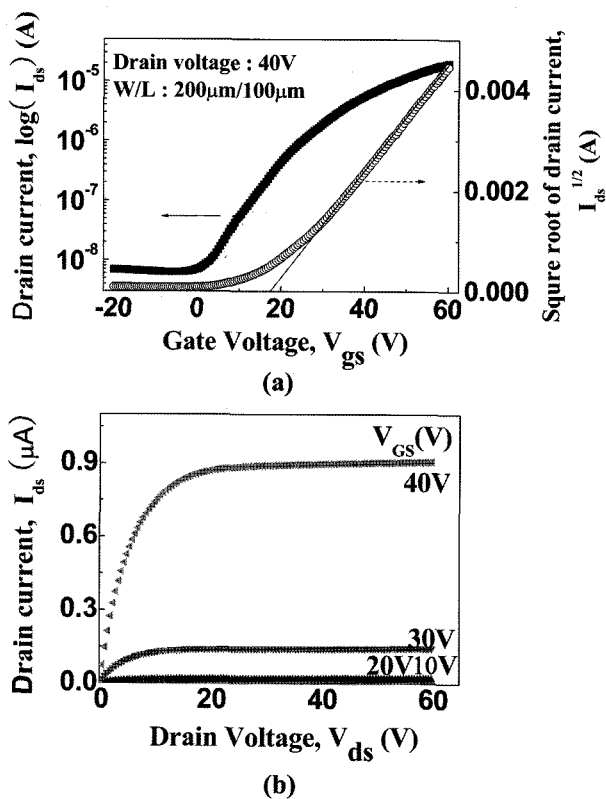
Fig. 3. Device characteristics of ZnO TFTs with the organic gate insulator. (a) Transfer characteristics (I_{ds}-V_{gs}) of various ZnO-TFTs with the PVP organic gate insulator layer at V_{ds} = 40. (b) The drain current with a variation of gate voltages from ZnO-TFTs with the organic gate insulator.

Table 1
Summary of the electrical characteristics of ZnO-TFTs with inorganic/organic gate insulators.

Gate dielectric		On/off ratio	Threshold voltage (V)	Field effect mobility ($cm^2V^{-1}s^{-1}$)
Inorganic	SiO_2	8×10^4	7.5	1.81
	SiN_x	5×10^6	20	20.2
Organic	PVP	6×10^3	17.5	1.37

to the lower carrier concentration and the higher crystallinity of ZnO channel. The lower carrier concentration of un-doped ZnO channel was obtained only by controlling process conditions during film deposition without external doping or post-annealing process. Besides, the field effect mobility of $20.2\ cm^2V^{-1}s^{-1}$ and on/off ratio of 5×10^6 was obtained for the ZnO-TFTs with SiNx dielectric which is much higher than those with SiO_2. It is due to the superior barrier property of SiNx against the Zn diffusion into dielectric. Furthermore, high field effect mobility ($1.37\ cm^2V^{-1}s^{-1}$) and on/off ratio (6×10^3) were obtained using an organic PVP gate dielectric. These results are compatible to those of OTFT processed at low temperatures with inorganic dielectrics. We suggest that ZnO-TFTs with inorganic SiN_x or organic PVP as a gate dielectric would be promising for various displays as OLED and LCD that require low temperature processes and high performance.

the poor interface of ZnO and organic gate insulation, we supposed that PVP was formed by the spin coating process, caused by lattice mismatch between large molecular organic and inorganic semiconductors. The value of μ_{FE} of ZnO-TFTs with PVP dielectric was 1.37 $cm^2V^{-1}s^{-1}$, which is higher than those of OTFT devices with the same PVP dielectric but organic channel (< 1 $cm^2V^{-1}s^{-1}$) [12]. It indicates that ZnO-TFTs with the new organic gate dielectric can replace the well-known pentacene OTFT for the various displays.

4. Conclusions

In conclusion, we investigated the device performance of ZnO-TFTs with inorganic and organic gate dielectrics of SiO_2, SiN_x, and PVP. Table 1 summarizes the principal electrical properties, including field effect mobility and on/off ratio of these ZnO-TFTs. These values are excellent compared with those of ZnO-TFTs having same dielectric materials previously reported Improvements of these devices performance are related

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References

[1] E.M.C. Fortunato, P.M.C. Barquinha, A.C.M.B.G. Pimentel, A.M.F. Goncalves, A.J.S. Marques, L.M.N. Pereira and R.F.P. Marins, "Fully transparent ZnO thin-film transistor produced at room temperature", Adv. Mater. 17 (2005) 590.

[2] B. Liu, Z. Fu and Y. Zia, "Green luminescent center in undoped zinc oxide films deposited on silicon substrates", Appl. Phys. Lett. 79 (2001) 943.

[3] H.Y. Choi, S.H. Kim and J. Jang, "Self-organized organic thin-film transistors on plastic", Adv. Mater. 16 (2004) 732.

[4] M.H. Lim, K.T. Kang, H.G. Kim, I.D. Kim, Y.W. Choi

and H.L. Tuller, "Low leakage current - stacked MgO/ $Bi_{1.5}Zn_{1.0}Nb_{1.5}O_7$ gate insulator - for low voltage ZnO thin film transistors", Appl. Phys. Lett. 89 (2006) 202908.

[5] H. Yabuta, M. Sano, K. Abe, T. Aiba, T. Den, H. Kumomi, K. Nomura, T. Kamiya and H. Hosono, "High-mobility thin-film transistor with amorphous $InGaZnO_4$ channel fabricated by room temperature rf-magnetron sputtering", Appl. Phys. Lett. 89 (2006) 112123.

[6] P.F. Carcia, R.S. McLean, M.H. Reilly and G. Nunes, "Transparent ZnO thin-film transistor fabricated by rf magnetron sputtering", Appl. Phys. Lett. 82 (2003) 1117.

[7] S. Masuda, K. Kitamura, Y. Okumura, S. Miyatake, H. Tabata and T. Kawai, "Transparent thin film transistors using ZnO as an active channel layer and their electrical properties", J. Appl. Phys. 93 (2003) 1624.

[8] J. Nishii, F. M. Hossain, S. Takagi, T. Aita, K. Saikusa, Y. Ohmaki, I. Ohkubo, S. Kishimoto, A. Ohtomo, T. Fukumura, F. Matsukura, Y. Ohno, H. Koinuma, H. Ohno and M. Kawasaki, "High mobility thin film transistors with transparent ZnO channels", Jpn. J. Appl. Phys. 42 (2003) L347.

[9] R.L. Hoffman, "ZnO-channel thin-film transistors: Channel mobility", J. Appl. Phys. 95 (2004) 5813.

[10] H.S. Bae, M.H. Yoon, J.H. Kim and S. Im, "Photodetecting properties of ZnO-based thin-film transistors", Appl. Phys. Lett. 83 (2003) 5313.

[11] P.F. Carcia, R.S. McLean and M.H. Reilly, "High-performance ZnO thin-film transistors on gate dielectrics grown by atomic layer deposition", Appl. Phys. Lett. 88 (2006) 123509.

[12] J. Lee, D.K. Hwang, J.M. Choi, K. Lee. J.H. Kim and S. Im, "Flexible semitransparent pentacene thin-film transistors with polymer dielectric layers and NiO_x electrodes", Appl. Phys. Lett. 87 (2005) 023504.

[13] K. Lee, J.H. Kim and S. Im, "Probing the work function of a gate metal with a top-gate ZnO-thin-film transistor with a polymer dielectric", Appl. Phys. Lett. 88 (2006) 023504.

[14] E.M.C. Fortunato, P.M.C. Barquinha, A.C.M.B.G. Pimentel, R.F.P. Martins and L.M.N. Pereira, "Wide-bandgap high-mobility ZnO thin-film transistors produced at room temperature", Appl. Phys. Lett. 85 (2004) 2541.

[15] E. Fortunato, A. Pimentel, L. Pereira, A. Goncalves, G. Lavareda, H. Aguas, I. Ferreira, C.N. Carvalho and R. Martins, "High field-effect mobility zinc oxide thin film transistors produced at room temperature", J. Non-Cryst. Sol. 338-340 (2004) 806.