A Simple Efficient Stopping Criterion for Turbo Decoder

Young-Sup Kim and Sung-Woong Ra

ABSTRACT—The performance of a turbo decoder depends strongly on the number of iterations in its decoding process. It is necessary to stop the decoding process at an appropriate moment to alleviate the serious burden, in terms of both the computational speed and latency, part of which is associated with too many iterations. In this letter, we introduce a criterion for finding the opportune moment to stop the decoding process, called a hard decision aided criterion based on bit interleaved parity, which is known to have much simpler hardware logic, compared with other schemes, and does not lead to any significant performance degradation.

Keywords—Turbo decoding, iterative decoding, HDA.

I. Introduction

In digital communication systems, channel coding has been used to correct the bit errors caused by communication channels. Turbo coding was introduced in 1993 [1] as a forward error correction technique that has a decoding performance close to the Shannon limit. It has been chosen by international standard bodies such as ITU and 3GPP as a channel coding for third-generation wireless high-speed data services [2]. A turbo code, called a parallel concatenated convolutional code (PCCC), consists of recursive systematic convolutional (RSC) encoders and interleavers. Due to an interleaver in an encoder, it is impossible to apply maximum likelihood sequence decoding. Therefore, the decoding of a turbo code can be done in an iterative way using a maximum *a posteriori* algorithm or soft output Viterbi algorithm. An output from the decoder in a turbo decoder is fed to the following stage decoder as an input. This feedback information is called extrinsic information. Since extrinsic information is used for decoding in the following iteration, turbo code has better performance as the number of iterations increases. But too many decoding iterations lead to more additional power consumption and decoding delay. As a result, it is important to find an efficient criterion to stop the iteration process and prevent unnecessary computation and decoding delay.

Some stopping criteria have been suggested based on the cross entropy (CE) between the distributions of estimated outputs of the decoders at each iteration [3]-[5]. It provides an effective stopping criterion of the iteration process, which has very little performance degradation. Another suggested stopping criterion is based on the signature code of estimated outputs [6]. Two successive decoding messages are compared bit-by-bit according to the CE-based stopping criteria. If the differences between the comparison messages are under an arbitrary threshold, the decoder stops its decoding process. Thus, the CE-based stopping criterion requires the same size of memories as that of messages to store previous decoding results. However, the signature-based stopping criterion needs memories with the size of the signature code because the decoding process can be terminated when two signature codes become equal. It is highly desirable to use a signature-based stopping criterion method in the design of a turbo decoder with insufficient memory space.

In this letter, we propose a new signature code, called *bit interleaved parity* (BIP) and apply it to the signature-based stopping criterion. Compared with the conventional CE-based criterion method, the proposed method can be implemented using little memory and simple hardware logics.

This letter is organized as follows. Turbo decoding and related works are introduced in section II. Section III describes the proposed stopping criterion using a BIP-based method and shows some simulation results. Finally, section IV provides our concluding remarks.

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II. Related Works

In this section, we review some conventional stopping criteria. The decoder block diagram of a rate-1/3 turbo decoder is shown in Fig. 1. The iterative decoder computes the reliability of the frame and stops the iteration when the reliability is less than the predetermined threshold.

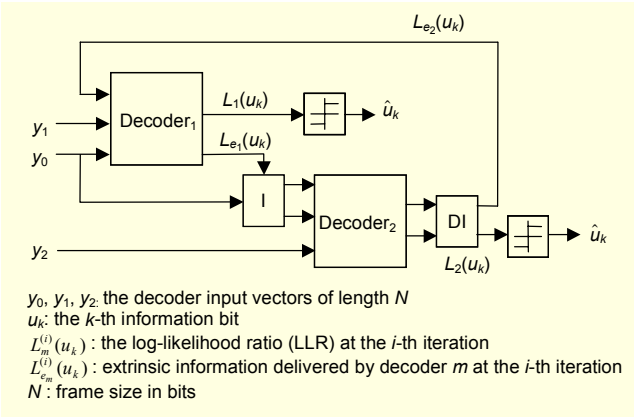

Fig. 1. Turbo decoder, code rate = 1/3.

The cross entropy (CE) technique [3] computes the approximate cross entropy $T_{CE}^{(i)}$ given by

$$T_{CE}^{(i)} = \sum_{k=1}^{N} \frac{\left| L_{e_2}^{(i)}(u_k) - L_{e_2}^{(i-1)}(u_k) \right|^2}{\exp\left(\left| L_1^{(i)}(u_k) \right| \right)} \qquad (1)$$

and stops the iteration if $T_{CE}^{(i)} < (10^{-2} \sim 10^{-4}) T_{CE}^{(1)}$.

In sign change ratio (SCR) and hard decision aided (HDA) criteria [4], the decoder counts the number of sign changes between $L_{e_m}^{(i-1)}(u_k)$ and $L_{e_m}^{(i)}(u_k)$ and stops the iteration if the ratio of sign changes to the frame size N is less than the threshold ε_{SCR} ($0.005 \le \varepsilon_{SCR} \le 0.03$).

In the sign difference ratio (SDR) [5] and improved HDA criteria [6], the decoder counts the number of sign changes between $L_m^{(i)}(u_k)$ and $L_{e_m}^{(i)}(u_k)$, where $L_m^{(i)}(u_k)$, is *a priori* information for u_k at decoder m, and stops the iteration if the ratio of sign changes to the frame size N is less than the threshold ε_{SDR} ($0.001 \le \varepsilon_{SDR} \le 0.01$). An advantage of SDR is that it does not require the memory to store the information obtained in the previous iteration.

The HDA criterion requires memory for storing previous hard decision output bits and N binary additions of each bit and a counter. To reduce the resources, an HDA criterion based on cyclic redundancy check (CHDA) [7] was proposed. The CHDA compares two consecutive CRCs calculated on the hard decision output bits of iterations i and i–1 and stops the iteration process if the two CRC values are equal.

III. A New Stopping Criterion and Comparisons

The CE technique is too complex to implement using hardware logics because it requires too many arithmetic logic units. The SCR and HDA techniques require large storage for saving previous decoding results. The SDR and improved HDA methods have no memory but require a comparator and a counter. The CHDA method needs CRC generation logic and some memories to store the previous CRC value. In this study, we introduce a new stopping criterion based on BIP of the half iteration decoding output, which is called BHDA. The BIP algorithm is widely used to detect the differences between two binary streams like the CRC calculations. For example, it is used to estimate the bit error rate (BER) of wire line communication link, or to check the integrity of data in storage media. The BIP values are calculated as

$$\begin{aligned} BIP_m^{(i)}(j) &= 0, \quad j < 0, \\ BIP_m^{(i)}(j) &= BIP_m^{(i)}(j-1) + \hat{u}_k, \quad k = 0, 1, 2, \cdots, N-1, \end{aligned} \qquad (2)$$

where $m = k \bmod n$, $j = \lceil k/n \rceil$, n is the code length of BIP, N is the message length, and (i) is the iteration number of the iterative decoding. If $BIP^{(i)} = BIP^{(i-1)}$ for $i \ge 2$, then the iterative decoding process is stopped. We can implement the BIP generation logic using only one adder and n shift registers by shift operations. Therefore, the BHDA algorithm requires one modulo-2 adder, n registers, n memories to save the previous BIP, and an n-bit comparator. The hardware logic of the BHDA algorithm is simpler than that of the CHDA because the CRC generation logic requires more adders than BIP. The complexity comparison is shown in Table 1.

We simulated the performance of each algorithm applied to the 3GPP turbo code. Figure 2 shows the performance of each algorithm under AWGN channel and Rayleigh fading channel with message length $N = 640$ bits. The 'GENIE' case, where the message bits are known at the decoder and the iteration stops immediately after the frame is correctly decoded, is shown as the limit of all possible schemes. All algorithms have

Table 1. Complexity comparison of stopping criteria.

	Memory	Arithmetic logic	Register
CE	$2N$	1 adder, multiplier, exponential function	-
SCR	N	Counter	-
SDR	N	Counter	-
CHDA	n	m adders (m>1)	n
BHDA	n	1 adder	n

N: message length, n: code length of CRC or BIP, m: according to the generating polynomial of CRC.

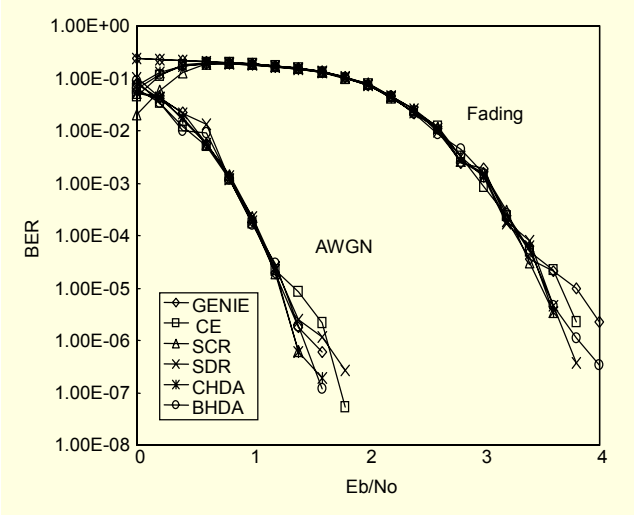

Fig. 2. Performance of stopping criteria (N = 640 bits).

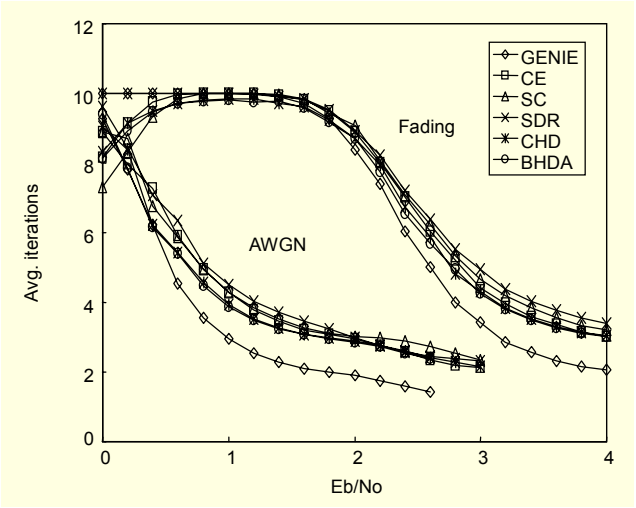

Fig. 3. Average number of iterations (N = 640 bits).

Table 2. Comparison performance of stopping criteria.

	AWGN (1 dB)		Fading (3 dB)	
	BER	Average iteration	BER	Average iteration
GENIE	1.84E-04	2.94	1.88E-03	3.43
CE	1.17E-04	4.29	8.54E-04	3.97
SCR	2.24E-04	4.29	1.56E-03	4.20
SDR	2.29E-04	4.52	1.46E-03	4.39
CHDA	1.86E-04	3.95	1.32E-03	3.83
BHDA	1.59E-04	3.87	1.48E-03	3.82

almost the same performance in view of BER. Figure 3 shows the average number of iterations of each algorithm. Some numerical results of the simulation are listed in Table 2. According to Fig. 3 and Table 2, the average iteration number of the BHDA and CHDA algorithms is nearly 10% lower than others under the AWGN channel and Rayleigh channel. But, the performance of each algorithm is almost the same. Therefore, BHDA and CHDA save about 10% power consumption by eliminating unnecessary operations.

IV. Conclusions

The performance of a turbo decoder is determined by the number of iterations in its decoding process. Because too many iterations cause a critical computation and latency burden, it is necessary to alleviate this problem by stopping the decoding process at the opportune moment. In this letter, we introduced a new stopping criterion in the decoding process, called HDA based on BIP (BHDA), which has simpler hardware logic than other schemes and does not lead to any performance degradation.

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