Novel Low-Power High-dB Range CMOS Pseudo-Exponential Cells

Carlos A. De La Cruz Blas and Antonio López-Martín

In this paper, novel CMOS pseudo-exponential circuits operating in a class-AB mode are presented. The pseudo-exponential approximation employed is based on second order equations. Such terms are derived in a straightforward way from the inherent nonlinear currents of class-AB transconductors. The cells are appropriate to be integrated in portable equipment due to their compactness and very low power consumption. Measurement results from a fabricated prototype in a 0.5 µm technology reveal a range of 45 dB with errors lower than ±0.5 dB, a power consumption of 100 µW, and an area of 0.01 mm^2.

Keywords: VGA, pseudo-exponential circuits, low-voltage.

I. Introduction

Pseudo-exponential circuits can be found in numerous applications such as communication systems and audio/video analog signal processing. Often these circuits are employed as part of a variable gain amplifier or automatic gain control [1]-[3]. The first realizations were implemented by means of bipolar junction transistors with their inherent exponential characteristic [4], [5]. In CMOS technology MOS transistors working in the weak inversion region or the available parasitic lateral bipolar transistors have been employed [6], [7]. However, the poor matching, limited bandwidth, and modest dynamic range of these devices have forced the employment of the quasi-quadratic law of MOS transistors in strong inversion and saturation [1]. In this latter operation mode, several strategies have been proposed in order to approximate the exponential law by quadratic and/or linear terms. Thus, truncated Taylor series [8]-[13] or pseudo-exponential approximations [3], [14]-[20] have been employed to this end. Nevertheless, most of the former proposed pseudo-exponential circuits are operating in a class-A mode, thus consuming substantial quiescent power.

In this paper, a novel implementation of class-AB pseudo-exponential cells is proposed to avoid this drawback. The exponential approximation is based on an alternative equation that leads to decibel ranges up to 50 dB [16]. In this regard, the authors of [19], [20] have proposed pseudo-exponential circuits following this approach. However, here such a technique is generalized, expanded, and applied to implement a new circuit. The new circuit features an output range larger (5 dB) than the circuits proposed in [19], [20]. Moreover, a comparison with former pseudo-exponential cells is presented to highlight the large output decibel range and low power consumption of the

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proposed cells. The circuits perform a voltage-to-voltage conversion allowing compatibility with voltage-mode circuits. Moreover, such cells feature simplicity, easy tuning, and an elegant way to implement the equations that form the approximation.

The paper is organized as follows. In section II, a review of the pseudo-exponential approximations is given. The proposed circuits and second-order effects are presented in section III and section IV, respectively. Measurement results from a fabricated prototype and a comparison with former implementations are introduced in section V in order to validate the employed approach and the proposed circuits. Finally, conclusions are drawn in section VI.

II. Exponential Approximations

The exponential function e^{ax} can be defined in a variety of equivalents ways, namely, limit, infinite series, and integral or differential form [21]. However, the more suitable form to approximate it using CMOS transistors is the infinite series definition given by

$$e^{ax} = 1 + \frac{a}{1!}x + \frac{a^2}{2!}x^2 + \cdots + \frac{a^n}{n!}x^n + \cdots, \quad (1)$$

where a and x are a coefficient and the independent variable, respectively. Now, if it is considered that $|ax| \ll 1$, the exponential function can be approximated by the first three terms of (1) as

$$e^{ax} \approx 1 + \frac{a}{1!}x + \frac{a^2}{2!}x^2 = \frac{1}{2}(1 + (1+ax)^2). \quad (2)$$

In [16], the approximation

$$e^{ax} = \frac{e^{ax/2}}{e^{-ax/2}} \approx \frac{k + (1+ax/2)^2}{k + (1-ax/2)^2} \quad (3)$$

is proposed, with $k \leq 1$ a constant. In (3), if $k = 1$, the approximation is called pseudo-exponential [1]. In this case, the numerator and denominator are the truncated second-order Taylor series described by (2). For $k < 1$, the approximation range is enlarged considerably [16]. Figure 1 shows a comparison on a dB-scale ($y = 20\ log_{10}(e^{ax}) = 20a log_{10}(e) \cdot x$) of different approximations.

In Fig 1, the approximations by (2) and (3) are plotted with $a = 0.15$. The truncated second-order Taylor series (dashed line) and pseudo-exponential $k = 1$ (dashed-dotted line) provide 12 dB and 20 dB ranges with nonlinearity errors less than ±0.5 dB, respectively. For $k < 1$ in (3), the dB-linear range is extended, thus for instance with $k = 0.2$ the range is enlarged from 20 dB to 50 dB as represented by the solid line in Fig. 1.

In [16], a current-mode circuit implementation of (3) is proposed. The design is based on two stacked translinear loops [22] to derive the second order terms in (3) and several transistors to allow division. In this paper, a novel voltage-mode implementation of (3) based on a class-AB transconductor is presented obtaining a significant reduction of transistor count and power consumption as demonstrated in section III.

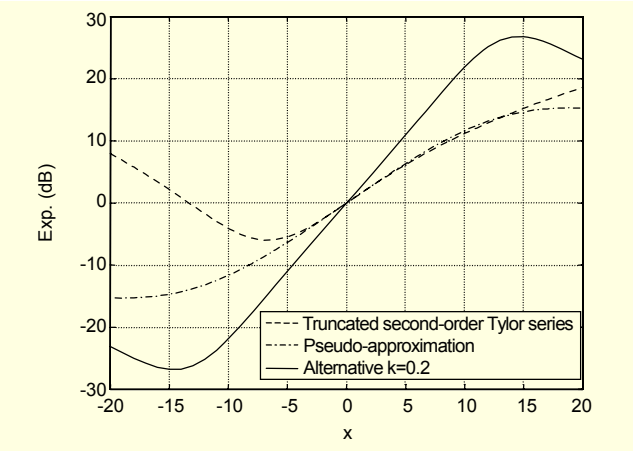

Fig. 1. Comparison of different pseudo-exponential approximations.

III. Circuit Implementation

In Fig. 2, the proposed circuits to implement (3) are shown. Both circuits are based on a class-AB transconductor, namely, M_1 to M_4, two scaled currents kI_B, a resistor and transistor M_5 operating in the triode region. In Fig. 2, the class-AB transconductors are known as a voltage-biased differential pair and a cross-coupled quad respectively. They have been used in adaptively biased linearized transconductors, multipliers, and an extended family of computational circuits [23], [24]. In both circuits, transistors M_1 to M_3 are matched and they work in strong inversion and saturation with

$$I_d = \frac{\beta}{2}(V_{GS} - V_T)^2, \quad (4)$$

where β and V_T are the tranconductance parameter and the threshold voltage. On the other hand, transistor M_5 is operating in the ohmic region as a voltage controlled resistor, that is,

$$I_{d5} = \beta(V_{GS5} - V_T)V_{DS5} + \frac{V_{DS5}^2}{2}. \quad (5)$$

Factor k of the scaled currents can be easily implemented by the transistor aspect ratios of a current mirror. In both circuits of Fig. 2, the input voltages $v_1 = V_{CM} - V_{in}/2$ and $v_2 = V_{CM} + V_{in}/2$

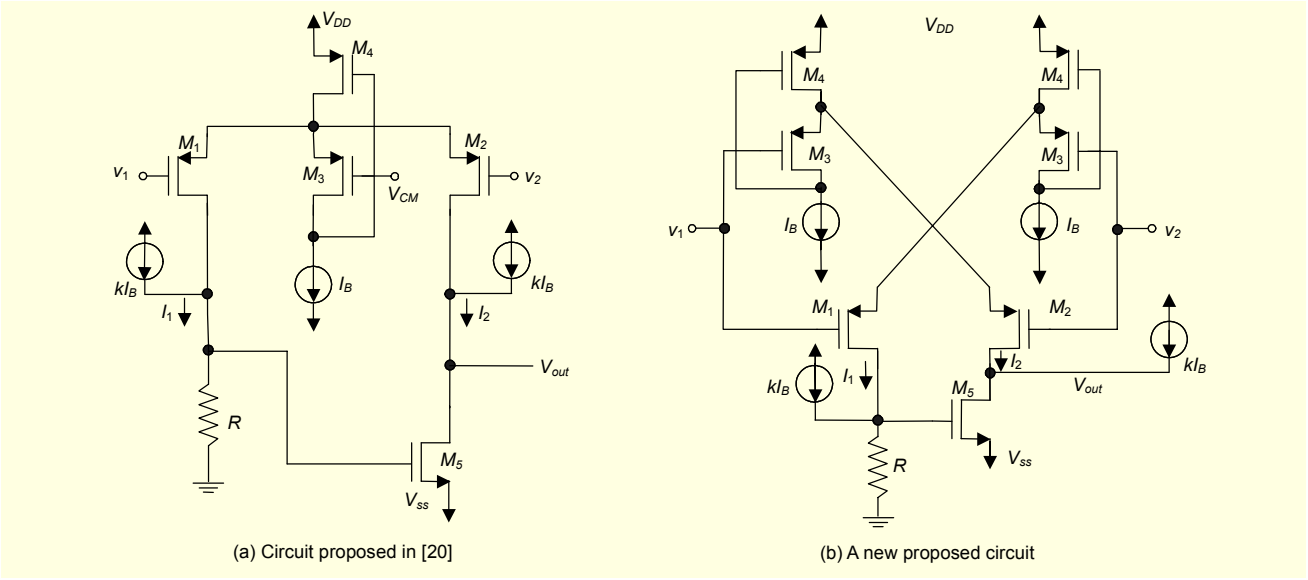

Fig. 2. Proposed circuits to implement a pseudo-exponential approximation.

are applied to the gates of M_1 and M_2, respectively. Then these voltages are converted to drain currents I_1 and I_2. Such currents, together with scaled current sources kI_B, form the numerator and denominator of (3). The division and conversion to voltage in (3) are implemented by resistor R and transistor M_5.

1. First Approach

This approach is based on [19] and [20]. In Fig. 2(a), transistors M_1 to M_4 implement a pseudo-differential pair [24], [25]. The configuration of transistors M_3 and M_4 set a very low impedance node at the drain of M_4 with a voltage value of [26]

$$V_{CM} + \sqrt{\frac{2I_B}{\beta}} + |V_T|,$$

hence the currents I_1 and I_2 are given by

$$I_1 = \begin{cases} 0 & \text{if } v_{in} > a/2 \\ I_B(1 - av_{in}/2)^2 & \text{if } v_{in} < a/2 \end{cases} \tag{6}$$

$$I_2 = \begin{cases} 0 & \text{if } v_{in} < -a/2 \\ I_B(1 + av_{in}/2)^2 & \text{if } v_{in} > -a/2 \end{cases} \tag{7}$$

with $a = \sqrt{\beta / 2I_B}$. Equations (6) and (7) are the typical V-I characteristic of a class-AB transconductor [23]. Thus, for v_{in} =0V, the quiescent current of the cell is given by I_B, and for v_{in}≠0V, the current I_1 and I_2 can be higher than I_B following a square V-I characteristic. Following with the implementation of (3), the numerator and denominator are easily achieved adding the scaled currents kI_B at the drains of M_1 and M_2, that is, $kI_B + I_B$ $(1 - av_{in}/2)^2$ and $kI_B + I_B(1 + av_{in}/2)^2$, respectively. Note that these latter terms can be implemented by second-order truncated Taylor series of the exponential function (2). If the decibel range in our application is flexible (< 12 dB) these approximations can fulfill the requirements. In this paper, the resistor R and transistor M_5 are employed to allow division and implementation of (3), obtaining a decibel range up to 45 dB with errors less than ±0.5 dB.

If the voltage at the drain of M_5 is considered small, transistor M_5 operates as a voltage-controlled resistor R_{DM5} with

$$R_{DM5} = \frac{1}{\beta(V_{GS5} - V_T)} \tag{8}$$

and

$$V_{GM5} = (I_1 + kI_B)R, \quad v_{out} = (I_2 + kI_B)R_{DM5}, \tag{9}$$

thus

$$v_{out} \approx \begin{cases} \dfrac{k}{\beta R\left(k + \left(1 - \dfrac{av_{in}}{2}\right)^2 - \dfrac{V_{ss} + V_T}{RI_B}\right)}, & v_{in} < \dfrac{-2}{a} \\ \dfrac{k + \left(1 + \dfrac{av_{in}}{2}\right)^2}{\beta R\left(k + \left(1 - \dfrac{av_{in}}{2}\right)^2 - \dfrac{V_{ss} + V_T}{RI_B}\right)}, & \dfrac{-2}{a} \le v_{in} \le \dfrac{2}{a} \\ \dfrac{k + \left(1 + \dfrac{av_{in}}{2}\right)^2}{\beta R\left(k - \dfrac{V_{ss} + V_T}{RI_B}\right)}, & v_{in} > \dfrac{2}{a} \end{cases} \tag{10}$$

If the term $(V_{ss}+V_T)/RI_B$ is considered negligible (see section IV for more details), then an implementation of (3) is achieved with $-2/a \leq v_{in} \leq 2/a$ as input voltage range. Note that outside this range the circuit implements an approximation of $e^{ax/2}$.

2. Second Approach

The operation of the circuit in Fig. 2(b) is similar to that of the circuit in Fig. 2(a) but in this case, the circuit implementation is new. The difference relies on the implementation of currents I_1 and I_2. In Fig. 2(b), the class-AB transconductor is formed by transistor M_1-M_4. Due to the negative shunt feedback of M_4, its drain voltage is accurately set by the gate voltage of M_3. Moreover such a node is a low impedance one able to drive a large current as required by the design. Thus M_3 and M_4 act as floating voltage sources [24]-[27]. Therefore, the sum of gate-to-source voltages of transistor M_1 and M_2 is forced to be constant. The currents I_1 and I_2 are given by (6) and (7), but now parameter a is $a = \sqrt{2\beta / I_B}$, that is, two times the circuit shown in Fig. 2(a). The remaining elements operate as the circuit of Fig. 2(a) and they follow the expression (10). An advantage of this approach is that the input voltage does not need to be balanced, but more area and power consumption are required.

IV. Second Order Effects

In this section, second order effects on the proposed cells are analyzed. The main considered effect is mismatch in the currents I_B. It leads to different k values in the numerator and denominator of (3). Thus, the impact of such difference in the approximation has to be analyzed. This effect is illustrated in Fig. 3.

In Fig. 3, the parameter k in approximation (3) is modified. The solid line, dashed line, dashed-dotted line, and dotted line represent the ideal approximation with $a = 0.15$ and $k = 0.2$, the parameter $k = 0.5$ ($k = 0.2$) in the numerator (denominator), the parameter $k = 0.5$ ($k = 0.2$) in the denominator (numerator), and the parameter $k = 10$ ($k = 0.2$) in the denominator (numerator), respectively. Note that the mismatch of k affects the behavior in the approximation (3). For a larger k in the numerator than in the denominator (dashed line) the range is decreased by the lower values. On the other hand, for a larger k in the denominator than in the numerator (dashed-dotted line) the range is again decreased, but in this case for the higher values. The high differences between values of k in Fig. 3 are only to show the effects on approximation. For more realistic deviations, it is considered that k can present a variation of ±5%. Under these conditions, the output range is reduced by 0.8 dB. Therefore the impact on current mismatch is minimal. In order

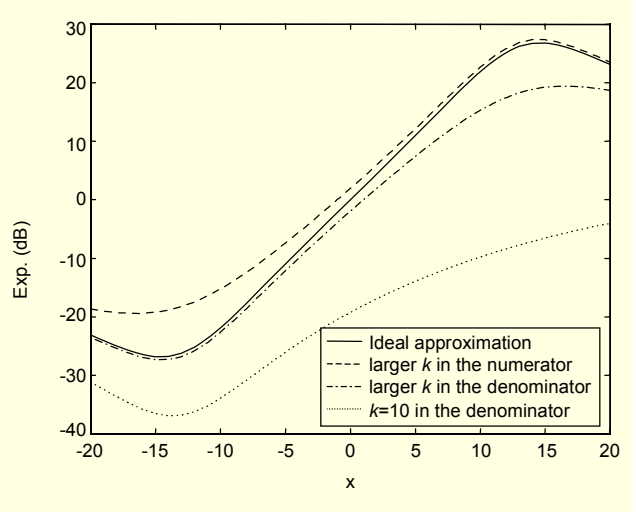

Fig. 3. Second order effects: mismatch of current I_B.

to more accurately predict the deviation of parameter k, the implementation of the current mirror, the area, the current magnitude, and parameters depending on the CMOS technology have to be considered [28], [29].

An in-depth look at (10) reveals that in the denominator there is a constant term namely $(V_{ss} + V_T)/RI_B$ which can strongly affect the pseudo-exponential approximation. For instance, if it is considered that V_{ss} = -1.5 V, V_T = 0.65 V, R = *10* kΩ, and I_B = 10 μA, then $(V_{ss} + V_T)/RI_B$ = -8.5. This value adds a constant in the denominator to the parameter k of (10) reducing the decibel range drastically. As an example, in Fig. 3, the dotted line represents the exponential approximation (3) with $k = 0.2$ in the numerator and $k = 10$ in the denominator. Note that more than 50% of the range is lost. To avoid this fact, higher current levels of I_B and/or higher values of resistance can be employed.

The body effect does not influence the operation of the circuits in Fig. 2, since all the MOS transistors with source not connected to the supply rail are PMOS ones embodied in independent wells.

V. Measurement Results

The circuits of Fig. 2 were fabricated in a 0.5 μm CMOS process. The measurement results were obtained using a dual supply voltage of ±1.5 V, I_B = 5 μA, and the factor $k = 0.2$. The power consumption under these conditions was less than 100 μW for the circuit in Fig. 2(a) and less than 125 μW for the one in Fig. 2(b). The transistor aspect ratios (W/L) were M_1-to-M_3 (75/1.2), M_4 (50/0.6), and M_5 (7/1.2). Resistor R was 20 kΩ. Figure 4 shows the measured dc transfer curves from the fabricated prototype. The deviations that were observed between the measurement results and simulation results using the BSIM3.3 model for MOS transistors were less than 1%.

Figure 4(a) shows the output voltage v_{out} of the circuit in Fig. 2(a) as a dashed line and Fig. 2(b) uses a solid line with a linear scale in the Y axis for an input range of -1.5 V to 1.5 V. Note that the correct operation of the cells achieves output ranges up to 1.0 V for the circuit in Fig. 2(a) and 2 V for the circuit in Fig. 2(b). Outside these ranges, transistor M_2 is driven to the triode region precluding exponential behavior. The factor of 2 in parameter a in the circuit implementations can also be noted; thus, the parameter of the circuit of Fig. 2(b) is twice as large as that of the circuit in Fig. 2(a), but its input range is reduced by the same factor (see (10)). The small signal frequency response of the cells strongly depends on the output capacitance at the drain of M_2. Considering that the pseudo-exponential circuits are operating with an output capacitance of 1.0 pF and the bias conditions mentioned above, the bandwidth is around 50 MHz. For higher capacitances the bandwidth is reduced. Thus in the practical realization, the output capacitance was around 50 pF due to bonding pad, board, and test probe parasitics and the measured bandwidth was 2 MHz approximately.

Figure 4(b) shows the measured results from Fig. 4(a) using a decibel scale on the Y axis. Moreover, the prediction of (10) is in agreement with the experimental results. Note the high decibel range up to 42 dB and 52 dB with errors less than ±1.5 dB for the circuit of Fig. 2(a) and Fig. 2(b), respectively. Such errors can be improved by increasing the I_B current, but the decibel range will be reduced. Thus, employing a current I_B = 10 μA the ranges are 39 dB and 45 dB with errors less than ±1.0 dB, respectively. Table 1 shows a performance comparison of the cells in Fig. 2 with former implementations. The terms *Trans*., *Tech.*, and *Res.* in Table 1 stand for transistor count, employed CMOS technology, and presentation of results (simulation or measurement results), respectively. Reference [19] presents a version of the circuit illustrated in Fig. 2(a) using floating gate transistors and a novel biasing scheme to control the common mode voltage at the gate of M_3. In [20], a circuit is presented having the same topology as that illustrated in Fig. 2(a) and simulation results are given. The cell descriptions of Fig. 2 are in the last two rows of Table 1. The power consumption was calculated considering I_B = 20 μA to obtain output voltage errors less than ±0.5 dB. Note the simplicity and large decibel range that can be obtained with the proposed cells thanks to class-AB operation and the internal characteristics of their currents.

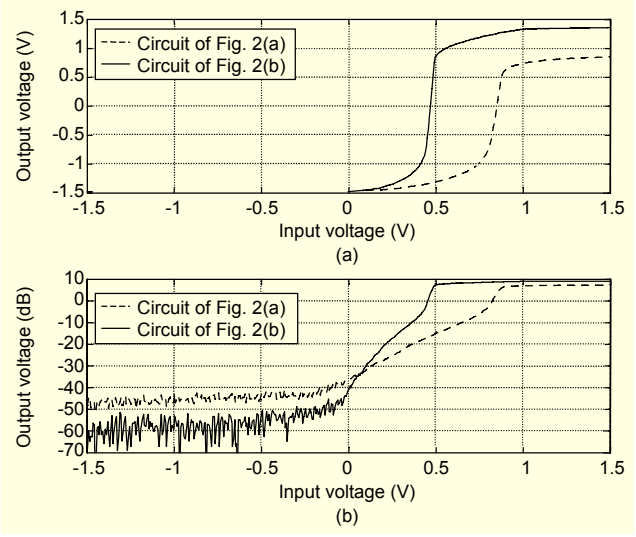

Fig. 4. Measurement results of the pseudo-exponential circuits proposed in Fig. 2, (a) with a linear Y axis and (b) using a dB Y axis.

Table 1. Comparison of former implementation with this work.

Ref.	Trans.	dB range	Error	Power	V_{dd}	Tech.	Res.
[8]	12	12 dB	±0.5 dB	1.74 mW	3 V	0.8 μm	Sim.
[9]	18	22 dB	±0.5 dB	2.1 mW	3 V	CI4007	Sim.
[10]	9	15 dB	±0.5 dB	0.8 mW	±1.5 V	0.35 μm	Sim.
[11]	14	30 dB	-	-	-	0.8 μm	Sim.
[12]	5	18 dB	±0.5 dB	0.5 mW	±1 V	0.25 μm	Sim.
[13]	11	38 dB	±1 dB	0.18 mW	1.2 V	0.18 μm	Fab.
[14]	9	30 dB	-	-	3 V	2 μm	Fab.
[15]	8	15 dB	±0.5 dB	0.4 mW	±1.5 V	0.5 μm	Fab.
[16]	25	46 dB	-	0.8 mW	1.5 V	0.25 μm	Sim.
[17]	15	31 dB	±0.5 dB	0.2 mW	1.25 V	0.25 μm	Sim
[19]	5	47 dB	±1 dB	0.08 mW	±0.75 V	0.5 μm	Fab.
2(a)	5	37 dB	±0.5 dB	0.2 mW	±1.5 V	0.5 μm	Fab.
2(b)	7	42 dB	±0.5 dB	0.26 mW	±1.5 V	0.5 μm	Fab.

VI. Conclusion

In this paper, the inherent nonlinear currents of class-AB transconductors are proposed to implement pseudo-exponential approximations. Such nonlinear currents can form second-order truncated Taylor series easily providing flexibility in design. In this study, a transistor in the triode region was employed to allow a division between such nonlinear currents to increase the range up to 45 dB with errors less than ±0.5 dB. Two cells have been proposed and tested on silicon from a fabricated prototype to validate the approach and design. Second order effects on the mismatch of currents and considerations for the realization of approximations have been treated to provide more insight in the design. The cells realize a voltage-to-voltage conversion featuring compactness, simplicity, and very low power consumption with a high decibel range.

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