A New Approach for Built-in Self-Test of 4.5 to 5.5 GHz Low-Noise Amplifiers

Jee-Youl Ryu and Seok-Ho Noh

This paper presents a low-cost RF parameter estimation technique using a new RF built-in self-test (BIST) circuit and efficient DC measurement for 4.5 to 5.5 GHz low noise amplifiers (LNAs). The BIST circuit measures gain, noise figure, input impedance, and input return loss for an LNA. The BIST circuit is designed using 0.18 μm SiGe technology. The test technique utilizes input impedance matching and output DC voltage measurements. The technique is simple and inexpensive.

Keywords: BIST circuit, defect detection, input matching.

Manuscript received Aug. 31, 2004; revised Nov. 14, 2005.

Jee-Youl Ryu (phone: + 82 55 380 2208, email: Jeeyoul.ryu@samsung.com) was with Department of Electronic Engineering, Arizona State University, Tempe, USA, and is currently with Department of LCD Development Engineering, Samsung SDI, Suwon, Gyeonggi-do, Korea.

Seok-Ho Noh (phone: +82 54 820 5569, email: shnoh@andong.ac.kr) is with Department of Electronic & Information Engineering, Andong National University, Andong, Gyeongbuk, Korea.

I. Introduction

A recent proliferation of RF integrated circuit (IC) chips has been overwhelming in the wireless communication market. The integration density and complexity of these devices are increasing with consumer demands in functionality. With testing cost being a large portion of the total production cost, there should be a cheaper way to test RF IC chips. In spite of the considerable research underway to reduce the testing overhead in RF IC chips [1]-[3], the difficulties in testing still remain as the major bottleneck of product manufacturing. The problems come from a limited access to major components of the internal RF structures, and the non-linear effects in RF faults that may occur on a circuit under testing [4]-[5]. To solve these problems, the BIST technique in the RF and mixed signal domain is applied as a suitable on-chip test structure [6]-[10].

To design an effective RF BIST structure, proper identification of catastrophic faults and parametric variations in the RF system play an integral part of the design. Analog systems have only a few inputs and outputs, and their internal states exhibit low time constants compared to digital circuits. A test resulting in a high coverage for catastrophic faults is possible using the standard approach based on current test stimulus and frequency domain measurements. However, according to Pleskacz and others, the standard approach based on current test stimulus covers only linear circuits [4]. This approach is difficult when used to detect and diagnose spot defects that severely result in non-linear RF circuits implemented as CMOS or BiCMOS ICs [7]. To test point-to-point radios, a loopback technique with a BIST using a spectral signature analysis is generally used with lower effort and very small test overhead [2]-[4]. However, this test technique has disadvantages such as a lower test coverage due to the fact that

the complete transceiver is tested as a whole, and the need of an additional digital signal processor hardware because of the higher complexity of the test signature generation [6]-[7]. R. Voorakaranam and others demonstrated the testing of gain, noise figure, and third-order input intercept point (IIP3) of a 900 MHz LNA using signature analysis. This technique also requires an additional off-chip signature response evaluator such as the FASTest RF runtime system [3].

In this paper, we discuss an RF parameter estimation method of noise figure, voltage gain, input impedance, and input return loss for a 4.5 to 5.5 GHz LNA using a novel BIST circuit and a very efficient DC measurement. This measurement and parameter estimation method can be highly correlated with bench equipment to improve its accuracy in production IC tests. The BIST scheme is based on an input impedance measurement and peak detection of the output transient voltage. The LNA and BIST circuits are integrated on a single chip using 0.18 μm SiGe technology. Our BIST technique requires only the use of a DC meter and RF voltage source generator.

II. Test Set-up and Approach

The traditional way of testing an LNA involves measurements of S-parameter, noise figures, signal-to-noise ratio, and IIP3 using a variety of different RF testing equipment. It is highly labor intensive and requires expensive measurement equipment. Our proposed technique utilizes an on-chip BIST circuit to measure and extract important LNA specifications without major external testing equipment.

Figure 1 shows the proposed testing set-up and characterizes gain, noise figure, input impedance, and input return loss for the LNA. The on-chip RF BIST consists of a test amplifier (TA) and two RF peak detectors, PD1 and PD2. The RF peak detectors are used to convert an RF signal to DC voltage [11]. The measurement set-up contains low-loss RF relays with 50 ohm matching impedances, and input transmission matching to the LNA and TA. The complete LNA test structure consists of an RF voltage source generator (v_{in}), LNA chip with RF BIST, DC meter, 50 ohm load impedance (Z_L), and three external switches, *S1, S2*, and *S3*.

In our testing approach, we assumed a unilateral LNA where the reverse isolation (S_{12}) is zero. The fabricated LNA has a maximum error of less than ± 0.005 dB at 4.5 to 5.5 GHz as discussed in [12], so we considered the fabricated LNA as a unilateral LNA.

The key result of this work provides a highly efficient low-cost accurate determination of input impedance, gain, noise figure, and input return loss, irrespective of considering second-order effects such as S_{12} and so on. The extracted input impedance, gain, noise figure, and input return loss are very close to the measured values, and they can be used for parametric and catastrophic fault testing of RF amplifiers. Their accuracies can be improved through industry standard look-up table calibration procedures. The following sections describe test details of these parameters.

A. Input Impedance

Figure 2 shows the equivalent circuit for the inputs of the LNA and test amplifier. Impedances Z_1 and Z_2 represent the input impedances of the LNA and test amplifier, respectively. These impedances have real and imaginary parts.

The input impedance measurement is performed with switches *S2* and *S3* in closed positions and switch *S1* in an open position. The overall testing technique is to find any deviations between source impedance R_s and input impedances Z_1 and Z_2. For example, the TA of Fig. 1 looks for changes in the input impedance of the LNA for any mismatch with the source resistance. In the case of a mismatch due to a defect or process variation, the transient DC voltage of PD2 is presented at the test output in the DC measurement. For simplicity we abbreviate 'test frequency range between 5 and 5.25GHz' as TFR and 'whole test frequency range between 4.5 and 5.5 GHz' as WTFR. We consider three cases below.

Case I. Fault-Free LNA at TFR

We consider a fault-free LNA with good input matching condition. Equation (1.1) represents the theoretical values for the voltage across the input impedances of the LNA and TA.

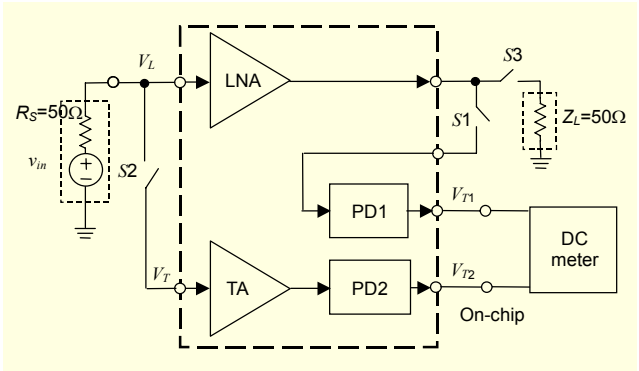

Fig. 1. Set-up of the proposed test structure.

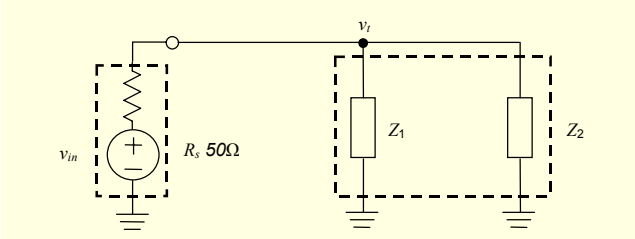

Fig. 2. Equivalent circuit for the inputs of an LNA and test amplifier.

The TA is designed with input and output matching impedances of 50 Ω, and a flat gain of $G_2 \approx 3$ to increase the test output voltage to the level of the original input voltage $|v_{in}|$ as indicated in (1.2). The BIST circuit monitors transient DC voltage V_{T2} as shown in Fig. 1. Equations (1.1) and (1.2) represent important expressions that were developed to derive the input impedance of the LNA.

$$|v_t| = \left|\frac{Z_1 // Z_2}{[R_s + (Z_1 // Z_2)]}\right| |v_{in}| = \left|\frac{Z_1}{2Z_1 + R_s}\right| |v_{in}|, \tag{1.1}$$

$$\begin{aligned} V_{T2} &= |v_{TAout}| + V_{02} = |v_t| \times (G_2) + V_{02} \\ &= \left|\frac{Z_1}{2Z_1 + R_s} v_{in}\right| \times (G_2) + V_{02}, \end{aligned} \tag{1.2}$$

where $|Z_1|$ and $|Z_2|$ are magnitudes of the input impedances of the LNA and TA, respectively, G_2 is the voltage gain of the TA and designed to be 3, and V_{02} is the DC output voltage of the peak detector, PD2. Since the complex impedances of the LNA and the test amplifier can be said to have Re(Z_1)>>Im(Z_1), and Re(Z_2)>>Im(Z_2), their magnitudes $|Z_1|$ and $|Z_2|$ are respectively expressed by

$$|Z_1| = \sqrt{[\mathrm{Re}(Z_1)]^2 + [\mathrm{Im}(Z_1)]^2} \approx \mathrm{Re}(Z_1), \tag{1.3}$$

$$|Z_2| = \sqrt{[\mathrm{Re}(Z_2)]^2 + [\mathrm{Im}(Z_2)]^2} \approx \mathrm{Re}(Z_2). \tag{1.4}$$

From (1.1) to (1.4), we can express the new magnitude of the input impedance of the LNA as

$$|Z_{1B}| = R_s \frac{K_1}{1 - 2K_1} [\Omega], \tag{2.1}$$

where $K_1 = G_{02}/G_2$ and G_{02} is the voltage gain obtained by the input matching test.

$$G_{02} = \frac{V_{T2} - V_{02}}{|v_{in}|}. \tag{2.2}$$

Case II. Faulty LNA at TFR

The LNA can have catastrophic faults such as a resistive short or open faults due to the spot defects, and parametric faults such as unusual parameter variations or unusual process variations [4], [8], and [9]. In this case, there is a certain variation in magnitude of the input impedance of the LNA because of the change in its input matching condition. If the transient output voltage has $\overline{V_{T2}} > V_{T2}$, (2.1) can be expressed as (3). Transient DC voltage $\overline{V_{T2}}$ replaces V_{T2} under a faulty case.

$$|\overline{Z_{1B}}| \le R_s \frac{K_1}{1 - 2K_1} [\Omega], \tag{3}$$

where $|\overline{Z_{1B}}|$ represents $|Z_{1B}|$ under a faulty case.

If $\overline{V_{T2}} \le V_{T2}$, (2.1) can be expressed as (4).

$$|\overline{Z_{1B}}| \le K_1 \left(2|Z_{1B}| + R_s\right) [\Omega]. \tag{4}$$

Case III. Fault-Free LNA at WTFR

Consider the input impedance of the LNA obtained by the BIST at the WTFR. In this case, there are certain variations in the input impedance magnitudes of both the LNA and test amplifier because of changes in their input matching condition. The test amplifier was designed with less than ±10% magnitude variation of input impedance at the WTFR, as compared to the magnitude of input impedance at the TFR. When this approximation is applied, $|Z_2| \approx \mathrm{Re}(Z_2)$ for Re(Z_2)>>Im(Z_2). Thus, we derive (5) at the WTFR.

$$|Z_1| = \frac{R_s \dfrac{G_{02}}{G_2 \pm \Delta G_2}}{\left(1 - \left[1 + \dfrac{R_s}{|Z_2| \pm \Delta |Z_2|}\right]\left[\dfrac{G_{02}}{G_2 \pm \Delta G_2}\right]\right)} [\Omega], \tag{5}$$

where ΔG_2 is the voltage gain variation obtained by the input matching test, and $\Delta|Z_2|$ is the magnitude variation of the input impedance of the test amplifier.

B. Voltage Gain

Case I. Fault-Free LNA at TFR

As Fig. 1 shows, the voltage gain measurement is performed with switch *S1* in a closed position, and switches *S2* and *S3* in an open position. The voltage gain measurement is based on monitoring the transient DC voltage of the first peak detector, PD1. The BIST monitors transient DC voltage V_{T1} as shown in Fig. 1.

$$V_{T1} = G_{1B} |v_L| + V_{01}, \tag{6}$$

where V_{01} is the DC output voltage of PD1.

From Fig. 1, we obtain (7).

$$|v_L| = \frac{|Z_{1B}|}{R_s + |Z_{1B}|} |v_{in}|. \tag{7}$$

Therefore, from (6) and (7), we get the voltage gain of the LNA using the BIST.

$$G_{1B} = \frac{V_{T1} - V_{01}}{|v_L|} = \frac{R_s + |Z_{1B}|}{|Z_{1B}|} G_{01}, \quad (8.1)$$

where G_{01} is the voltage gain measured by a gain test.

$$G_{01} = \frac{V_{T1} - V_{01}}{|v_{in}|}. \quad (8.2)$$

Case II. Faulty LNA at TFR

Under a faulty case, if $\overline{V_{T2}} > V_{T2}$, (8.1) can be expressed as (9.1), and if $\overline{V_{T2}} \le V_{T2}$, it can be expressed as (9.2).

$$\overline{G_{1B}} \le \frac{|\overline{Z_{1B}}|_{\min} + R_s}{|\overline{Z_{1B}}|_{\min}} G_{01}, \quad (9.1)$$

$$\overline{G_{1B}} \le \frac{|Z_{1B}| + R_s}{|\overline{Z_{1B}}|_{\max}} G_{01}. \quad (9.2)$$

Case III. Fault-Free LNA at WTFR

In this case, putting (5) into (8.1), we obtain the voltage gain for a fault-free LNA at *WTFR*.

C. Noise Figure

The conventional formula for the noise figure [4] is

$$NF = 1 + \frac{N_2}{GN_1}, \quad (10)$$

where G is the amplifier power gain, N_1 is the LNA source resistance noise power, and N_2 is the inherent output noise.

Case I. Fault-Free LNA at TFR

If there is no defect or acceptable process variation from input impedance and voltage gain measurements, the noise figure obtained by the BIST can be expressed using the noise figure required by the LNA specifications. An approximate expression for a fault-free noise figure based on the proposed RF BIST structure is developed as

$$NF_B = 1 + \frac{G_0}{{G_{1B}}^2}(NF_0 - 1) = 1 + \left\{\frac{|Z_{1B}|}{[R_s + |Z_{1B}|]}\right\}^2 \cdot \frac{G_0}{{G_{01}}^2}(NF_0 - 1), \quad (11)$$

where G_0 and NF_0 are the power gain and noise figure required by the specifications, respectively.

Case II. Faulty LNA at TFR

Under a faulty case, if $\overline{V_{T2}} > V_{T2}$, (11) can be expressed as

$$\overline{NF_B} \ge 1 + \frac{{|\overline{Z_{1B}}|_{\min}}^2 G_0}{\left(|\overline{Z_{1B}}|_{\min} + R_s\right)^2 {G_{01}}^2}(NF_0 - 1). \quad (12)$$

If $\overline{V_{T2}} \le V_{T2}$, (11) can be expressed as

$$\overline{NF_B} < 1 + \frac{{|\overline{Z_{1B}}|_{\min}}^2 G_0}{\left(|\overline{Z_{1B}}|_{\min} + R_s\right)^2 {G_{01}}^2}(NF_0 - 1). \quad (13)$$

Case III. Fault-Free LNA at WTFR

In this case, if we put (5) and (8.1) into (11), we can obtain the noise figure for a fault-free LNA at the WTFR.

D. Input Return Loss

The input return loss (RL_{in}) is also an important parameter in the LNA. Using unilateral assumption [12], we obtained the input return loss of the LNA from new measured input impedances using the BIST. We used the conventional formula discussed in [12].

III. Fault Models

Both catastrophic faults and parametric faults are considered for bipolar junction transistors (BJTs) and passive components [1]. Spot defects that can severely degrade the performance or result in chip malfunction are considered [7]. We used a 0.18 μm BiCMOS technology; however, only defects in BJTs are considered since the LNA is designed using the devices. The resistor and inductor with open faults are selected to have approximately ten times the given values, and the resistor and inductor with short faults are selected to have approximately 0.1 times the given values. For a capacitor, open faults have approximately 0.1 times the given value, and short faults have approximately 10 times the given value [1]. We considered ±10% to ±50% variations in resistors, capacitors, and inductors, and ± 25% and ± 50% for the number of emitters, emitter width, and length variations in BJTs for parametric faults. A total of 173 different fault models were considered. Amongst them are a fault-free model, 28 different catastrophic fault models, and 144 different parametric fault models.

In addition to inserting catastrophic faults into the simulations, we also performed Monte Carlo simulations and a sensitivity analysis. A Monte Carlo analysis is performed to ensure that no parametric faults can mask catastrophic faults. If the range of response of a catastrophic faulty circuit is indiscernible from a fault-free case, then the parametric fault will mask the catastrophic fault. We have considered variable process parameters such as surface mobility, junction depth,

substrate doping, cut-off voltage, transistor emitter lengths, and transistor emitter widths for Monte Carlo analysis. Each of the device model parameters listed above was randomly perturbed with a Gaussian distribution from one simulation to the next. The distribution of the Gaussian random variables was selected at 10% of nominal at 3σ.

IV. LNA and BIST Circuit Analysis

The two-stage LNA is designed using 0.18μm BiCMOS SiGe technology and its schematic is shown in Figure 3. It was designed for 5 GHz 802.11a wireless LAN application, and is powered by a 1 V supply. The bias stage utilizes a band-gap reference circuit for a low supply voltage and low power dissipation. It controls the base currents for the first and second stages. The base resistance of HBT Q_1 and bias resistor R_{b1} are selected to make good resistive input impedances for 5 to 5.25 GHz. The complete design consists of four HBT transistors, five inductors, five capacitors, and six resistors, all on a single chip.

The proposed BIST circuit is shown in Fig. 4. It consists of TA and peak detector, PD2, circuit stages. The other peak detector circuit, PD1, is also a part of the BIST circuit and has the same topology as the PD2 circuit as shown in Fig. 4. The bias stage utilizes the band-gap reference circuit for a low supply voltage and low power dissipation. The inductor, L_{c01}, is used for input and output impedances matching. The RF peak

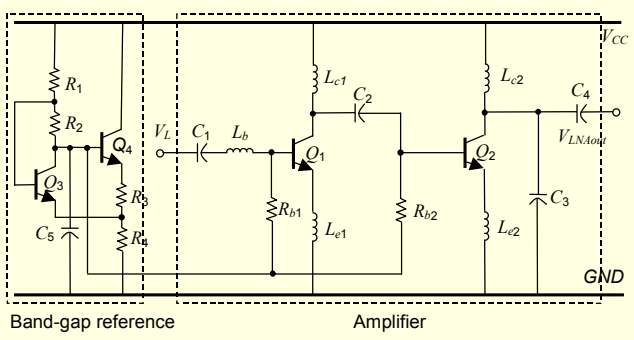

Fig. 3. Schematic diagram of a 5 GHz LNA.

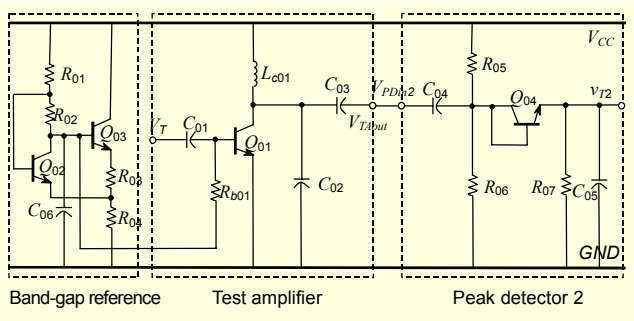

Fig. 4. Schematic diagram of a BIST.

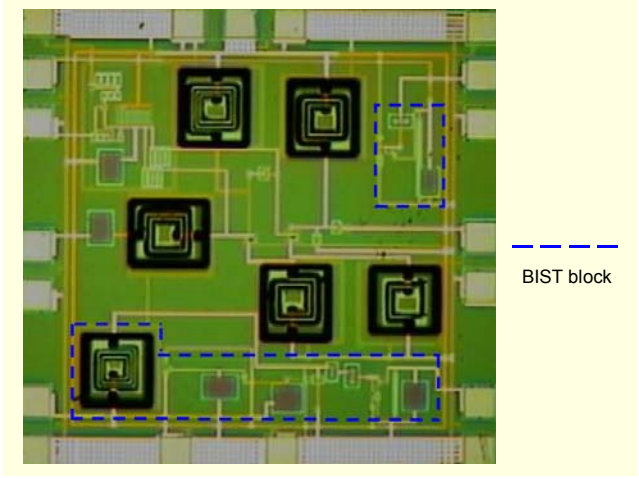

Fig. 5. Chip micrograph of the LNA and BIST circuit.

detectors are used to convert an RF signal to DC voltage [11]. The bias resistors, R_{05} and R_{06}, shown in Fig. 4 are used to keep transistor Q_{04} in the active region so that the transistor acts as a rectifier. The diode connections have the advantage of keeping the base-collector junction at zero bias. The smallest amount of minority charge storage during a forward biased condition will be highly beneficial to the rectification of RF signals [13]. To reduce the output ripple voltage, R_{07} and C_{05} are chosen with large values.

We processed a total of 173 defective cases, which resulted in 173 chip layouts for the post processing of defects. We used Cadence to perform the layouts and post processing. Figure 5 illustrates a chip micrograph of the LNA and BIST circuit. As an example, a defective inductor can be put into the circuit schematic of Fig. 3, and Cadence will automatically do a layout of the inductor. This process has been performed for all 173 cases, and a post processing has been done for each to verify the true values of the parasitics. We used the values that were extracted from the layout to perform a circuit simulation. We observed that the physical size of each circuit element on the chip layout varied with respect to the values given in the schematic. However, we fabricated seven cases for a fault-free LNA and six faulty LNAs. The physical chip area is approximately 1.45 mm × 1.45 mm using the 0.18 μm BiCMOS SiGe process. The BIST circuit is indicated in dotted lines. The chip area of the LNA and test circuit was not optimized to be compacted as small as possible, but for the experimental chip the BIST hardware occupies approximately 10% of the total area. It seems expensive in terms of area overhead. However, the proposed BIST technique represents a first step toward the development of a low-cost system-on-chip (SoC) transceiver environment and a first estimation method of an RF parameter using an efficient DC measurement without major and expensive external testing equipment.

V. Results

The proposed test technique utilizes output DC voltage measurements, V_{T1} and V_{T2}, and these measured values are translated into the LNA specifications such as input impedance and gain using the developed mathematical equations. In this work, we fabricated fault-free LNA, LNAs with Q_1 base open, Q_1 base-emitter and Q_1 emitter-collector short faults, and LNAs with process variations such as L_b+30%, L_b+40% and L_b+50%. Most of the data in section V are based on real measurements. Several measured data are compared with simulations.

1. Results for Cases I and II

Figures 6(a) and 6(b) show the scatter plots of transient DC voltages for various faults including open and short, as well as parametric variations in a low-noise amplifier. The results include simulated and measured data. The fault-free LNA provided real measured voltages of 180 mV and 445 mV for V_{T2} and V_{T1}, respectively. As can be seen from Fig. 6(a), most of the catastrophic faults are in the lower end of V_{T1} with a varying V_{T2}. For the resistor and transistor faults shown in Fig. 6(a), the observed output voltages V_{T1} remain in the far-left side as compared to a fault-free value. This result reveals that lower voltages of V_{T1} indicate faults in the resistors and transistors. These results show that the proposed BIST structure is suitable to detect a variety of faults. Figure 6(b) shows the scatter plot for parametric variations. It shows that the parametric faults are concentrated near the fault-free case. These transient voltages, V_{T1} and V_{T2} are measured after a settling time of 40 nanoseconds for the peak detectors, PD1 and PD2, to ensure a steady-state DC value. The output RC time constant of the peak detector contributed to the settling time constant. We used an RF input source of 100 to 180 mV at 4.5 to 5.5 GHz. The DC voltages V_{T1} and V_{T2} were measured using a conventional DC meter.

Table 1 shows a partial list of the actual measured V_{T1} and V_{T2} values of several faults for the results shown in Fig. 6. These results are measured at 5.25 GHz. In this table, we considered faults in transistor Q_1 and inductor L_b. These results are used to obtain voltage gains, noise figures, and magnitudes of input impedances of the LNA. As shown in Table 1, the fault-free value was significantly different from faulty values.

Using the values shown in Table 1, Table 2 lists real measured partial values of input impedances, gains, noise figures, and input return losses.

For good input matching, the LNA must have an input impedance of $Re(Z_1)\approx 50\Omega$ and $Im(Z_1)\approx 0$; however, the designed LNA showed an acceptable tolerance of $Re(Z_1)\approx 45\pm 10\Omega$ from the process variation. As shown in Table 2, for the fault-free case, the proposed BIST showed a very small error of 4% in input impedance, gain, noise figure, and

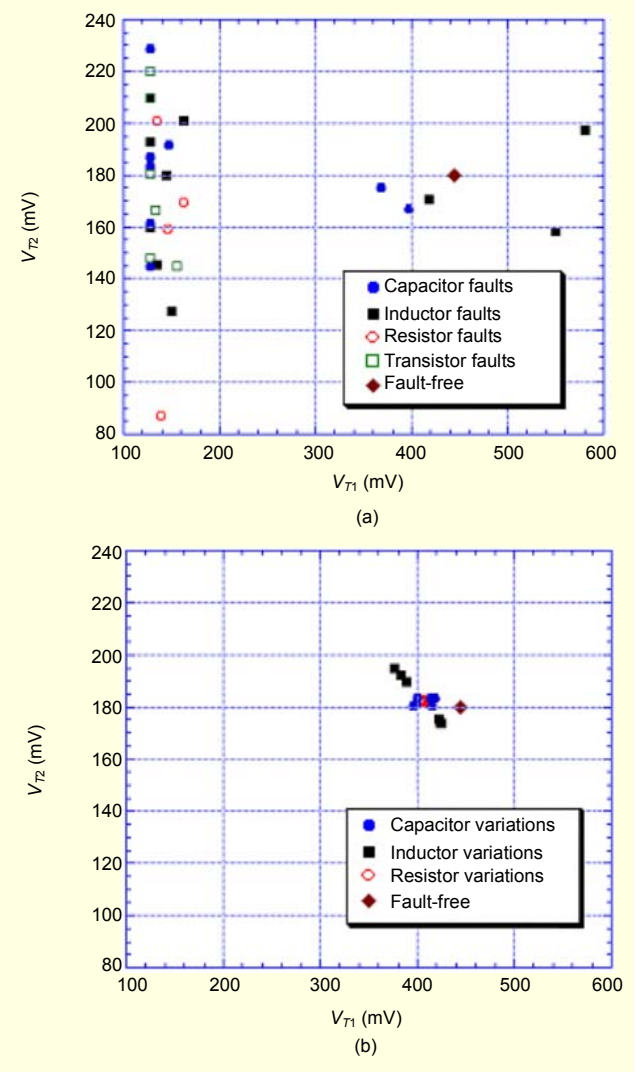

Fig. 6. Scatter plots of transient DC voltages for (a) catastrophic faults and (b) parametric variations.

Table 1. Real measured V_{T1} and V_{T2} by BIST.

Test voltage / Faults	V_{T1} (mV)	V_{T2} (mV)
Fault-free	445.0	180.0
Q_1 base open	127.3	209.6
Q_1 B-E short	127.3	220.0
Q_1 E-C short	155.2	144.6
L_b + 30%	389.3	194.8
L_b + 40%	383.5	192.0
L_b +50%	375.8	189.8

Table 2. Compared measurement results for LNA specifications.

Test / Faults	External equipment test				Proposed on-chip BIST			
	$\|Z_1\|$ (Ω)	G_1 (dB)	NF (dB)	RL_{in} (dB)	$\|Z_{1B}\|$ (Ω)	G_{1B} (dB)	NF_B (dB)	RL_{inB} (dB)
Fault-free	40.26	17.15	2.773	-19.4	41.76	16.89	2.904	-20.9
Q_1 base open	92.87	-75.84	88.06	-10.5	70.88	-44.44	61.11	-12.9
Q_1 B-E short	137.0	-28.83	26.28	-6.65	87.50	-44.60	61.27	-7.77
Q_1 E-C short	24.49	2.28	7.496	-9.31	33.28	-2.190	18.91	-14.8
L_b + 30%	53.38	16.18	2.956	-29.7	49.01	14.95	3.960	-26.7
L_b + 40%	57.35	16.05	3.035	-23.3	51.70	14.67	4.130	-34.6
L_b + 50%	61.69	15.90	3.120	-19.6	54.23	14.34	4.330	-39.2

input return loss compared to the results of the external equipment test, which included using expensive RF testing equipment.

These results reveal that our proposed on-chip BIST scheme is suitable for functional testing of an LNA. Using the RF Spectre suite of tools in Cadence, we were able to simulate conventional testing. We noticed that conventional testing provided significant differences between a fault-free and faulty LNA. On the other hand, the proposed BIST provided similar differences between the two. Therefore, the proposed BIST structure provides the same fault coverage with significantly less cost. The fault detection of an LNA can be made by looking at the gain, noise figure, impedance, or input return loss variations. The decreased inductance values did not vary much from the fault-free value. Therefore, we did not list them in Table 2.

The proposed on-chip BIST scheme showed fault coverage of 100% for catastrophic faults and 89% for process variations. There was very small deviation between the conventional and proposed on-chip BIST scheme for the fault-free case as indicated in Table 2.

2. Results for Case III

We also considered process variations of ±10% to ±25% of all the passives on the BIST circuit using a sensitivity analysis to verify its accuracy. The process variations on the inductor L_{c01} shown in Fig. 4 was the most sensitive to the gain variation of the LNA. The maximum change in the gain of the LNA due to the ±25% process variation of the BIST circuit was less than 0.02dB for the LNA. Therefore, the value can be neglected for the measurement error. Table 3 lists the measured gain and input impedance of the test amplifier. These results are used to obtain magnitudes of input impedances of the LNA as shown in (5). Because the test amplifier is designed with $\mathrm{Re}(Z_2)>>\mathrm{Im}(Z_2)$ at a frequency between 4.5 and 5.5 GHz, the input impedance phase shift of the test amplifier at this frequency range can be neglected.

Table 3. Measured gains and input impedances of the test amplifier.

Frequency (GHz)	S-parameter results	
	$G_2 \pm \Delta G_2$	$\|Z_2\| \pm \Delta\|Z_2\|$ (Ω)
4.50	2.80	54.57
4.75	2.92	52.45
5.00	3.10	50.28
5.25	3.06	47.95
5.50	2.98	45.31

Table 4. V_{T1} and V_{T2} measured by BIST circuit.

Frequency (GHz)	V_{T1} (mV)	V_{T2} (mV)
4.50	400	166.2
4.75	421	160.3
5.00	448	171.4
5.25	445	180.0
5.50	432	189.0

Table 4 lists V_{T1} and V_{T2} measured by the BIST circuit as a function of frequency. These results are also used to obtain voltage gains and magnitudes of input impedances of the LNA as shown in (2.1) and (8.1). As we can expect from these results, V_{T1} has higher values at the TFR than at other frequency ranges, and when the frequency is increased, V_{T2} is also increased.

The compared measurement results of an external equipment test, and the proposed on-chip BIST for a good LNA as a function of frequency, are listed in Table 5. Our proposed BIST results also showed good approximation results compared to the external equipment test.

Table 5. Compared measurement results of an external equipment test and proposed on-chip BIST.

Frequency (GHz)	External equipment test				Proposed on-chip BIST			
	G_l (dB)	Z_l (Ω)	NF (dB)	RL_{in} (dB)	G_{1B} (dB)	Z_{1B} (Ω)	NF_B (dB)	RL_{inB} (dB)
4.50	16.40	38.45	2.493	-17.68	16.00	38.16	2.674	-17.44
4.75	17.76	33.08	2.559	-13.82	17.44	34.64	2.707	-13.56
5.00	17.95	32.57	2.652	-13.51	17.96	34.18	2.648	-14.87
5.25	17.16	40.27	2.773	-19.35	16.89	41.76	2.904	-20.94
5.50	15.96	55.24	2.922	-26.06	15.40	55.98	3.206	-24.97

VI. Conclusions

This paper proposed a new low-cost BIST technique for measuring gain, noise figure, input impedance, and input return loss of a 4.5 to 5.5 GHz LNA. Our BIST scheme utilized input impedance and efficient DC voltage measurements to extract important RF parameters without major external testing equipment. The LNA and BIST circuits were designed using a 0.18 μm BiCMOS SiGe technology. The BIST circuit consisted of a test amplifier and two RF peak detectors. This technique requires only the use of a common DC meter and RF voltage source generator. We believe that proposed BIST technique is simple and inexpensive. This measurement and parameter estimation method will be highly correlated with bench equipment to improve its accuracy in production IC tests.

In the future we plan to present a more practical testing technique using an off-chip circuitry designed on a test board. Our technique will use the same circuitry to test millions of DUTs and fully characterize the on-board test circuitry at the debugging stage of product testing. Our technique will have a calibration step that periodically calibrates the on-board test circuitry.

References

[1] J.-Y. Ryu, B. C. Kim, S.-T. Kim, and V. Varadarajan "Novel Defect Testing of RF Front End Using Input Matching Measurement," *9th IEEE International Mixed-Signal Testing Workshop*, vol. 9, June 2003, pp. 31-34.

[2] M. Soma, "Challenges and Approaches in Mixed Signal RF Testing," *IEEE Proc.*, 1997, pp. 33-37.

[3] R. Voorakaranam, S. Cherubal and A. Chatterjee, "A Signature Test Framework for Rapid Production Testing of RF Circuits," *Proc. of the 2002 Design, Automation and Test in Europe Conference and Exhibition*, Mar. 2003, pp. 186-191.

[4] W. A. Pleskacz, D. Kasprowicz, T. Oleszczak and W. Kuzmicz, "CMOS Standard Cells Characterization for Defect Based Testing," *IEEE International Symposium on DFT in VLSI Systems*, Oct. 2001, pp. 384-392.

[5] A. J. Bishop and A. Ivanov, "On the Testability of CMOS Feedback Amplifiers," *IEEE Proc.*, 1994, pp. 65-73.

[6] D. Lupea, U. Pursche and H.-J. Jentschel, "RF-BIST: Loopback Spectral Signature Analysis," *IEEE Proc. of the 2003 Design, Automation and Test in Europe Conference and Exhibition*, Mar. 2003, pp. 478-483.

[7] J. Dabrowski, "BiST Model for IC RF-Transceiver Front-End," *2003 Proc. of the 18th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, Nov. 2003, pp. 295-302.

[8] B. R. Veillette and G. W. Roberts, "A Built-in Self-Test Strategy for Wireless Communication Systems," *Proc. of the 1995 International Test Conf.*, Oct. 1995, pp. 930-939.

[9] J.-Y. Ryu, B. C. Kim, and I. Sylla, "A New BIST Scheme for 5GHz Low Noise Amplifiers," *9th IEEE European Test Symposium*, vol. 9, May 2004, pp. 228-233.

[10] J.-Y. Ryu and B. C. Kim, "A New RF BIST for 4.5-5.5GHz Low Noise Amplifiers," *10th IEEE International Mixed-Signal Testing Workshop*, vol. 10, June 2004.

[11] R. G. Meyer, "Low-Power Monolithic RF Peak Detector Analysis," *IEEE J. of Solid-State Circuits*, vol. 30, no. 1, Jan. 1995, pp. 65–67.

[12] G. Gonzalez, *Microwave Transistor Amplifiers: Analysis and Design,* 2nd Ed., Prentice Hall, New Jersey, 1997, pp. 212-293.

[13] B. Razavi, *RF Microelectronics,* Prentice Hall, New Jersey, 1998, pp. 11-53.

Jee-Youl Ryu received the BS and MS degrees in electronics engineering from Pukyong National University, Busan, Korea in 1993 and 1997, and the PhD degree in electrical engineering from Arizona State University, Tempe, in December 2004. He is currently the Group Manager of LCD Development Engineering at Samsung SDI Co., Ltd., Korea. His current research interests include the design and testing of RF integrated circuits and the modeling of integrated passives.

Seok-Ho Noh was born in Seoul on August 1, 1959. He received the B. Eng. Degree in electronic engineering from Hanyang University, Seoul, Korea in 1982, the M. Eng. Degree in information engineering from Tokyo Institute of Technology, Tokyo, Japan in 1990, and the PhD degree in information engineering from Saitama National University, Saitama, Japan in 1993. In 1993, he joined the Satellite Communication Division of ETRI as a member of the research staff. Since 1998, he has been an Associate Professor at Andong National University, Andong, Korea. In 2003, he was a Visiting Researcher at the Dept. of Electrical Engineering of Arizona State University. His research interests include signal processing, digital DBS system, and RF IC design and testing.