Characteristic Variation of 3-D Solenoid Embedded Inductors for Wireless Communication Systems

Dongwook Shin, Changhoon Oh, Kilhan Kim, and Ilgu Yun

The characteristic variation of 3-dimensional (3-D) solenoid-type embedded inductors is investigated. Four different structures of a 3-D inductor are fabricated by using a low-temperature co-fired ceramic (LTCC) process, and their s-parameters are measured between 50 MHz and 5 GHz. The circuit model parameters of each building block are optimized and extracted using the partial element equivalent circuit method and an HSPICE circuit simulator. Based on the model parameters, the characteristics of the test structures such as self-resonant frequency, inductance, and quality (Q) factor are analyzed, and predictive modeling is applied to the structures composed of a combination of the modeled building blocks. In addition, characteristic variations of the 3-D inductors with different structures using extracted building blocks are also investigated. This approach can provide a characteristic estimation of 3-D solenoid embedded inductors for structural variations.

Keywords: Embedded inductor, low-temperature co-fired ceramic (LTCC), variation, partial element equivalent circuit (PEEC), modeling.

I. Introduction

Most modern wireless systems rely on radio frequency or microwave signals. The growth of commercial wireless communication systems has raised the demand for reduced size, high performance, low power, and low production cost [1]. In order to accomplish these demands with advances in technology, many off-chip passive components are being transferred to an on-chip system as integrated passives. The low-temperature co-fired ceramic (LTCC) process is considered a good choice for RF-integrated modules both in mobile phones and in base stations [2]. LTCC technology can support well over 30 layers of metal, each on a thin ceramic tape substrate, with interconnectivity between layers achieved by the use of vias [3].

Among the many passive elements, inductors are very important in many wireless applications. The inductor has an influence on the quality of a sub-circuit, such as a filter circuit, low-noise amplifier (LNA), and voltage-controlled oscillators (VCO) [4]-[6]. For mobile and microwave applications, inductors with high Q-factor and inductance are required. Previously, there have been numerous researches on the design, fabrication, and performance of planar spiral inductors. Li investigated the inductance calculation of micro-strip line spiral inductors using a closed form formula [7]. Zhang and others worked on the optimization of the characteristics of spiral inductors [6], and Lutz and others investigated the modeling of spiral inductors concerned with lossy substrates [8]. In addition, Melendy and others studied a new compact modeling for spiral inductors in RF-integrated circuits [9].

In this paper, we discuss a characteristic variation of 3-D solenoid embedded inductors. The inductor test structures are fabricated and their s-parameters are measured. The circuit model parameters of the inductor test structures, which are

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defined using partial element equivalent circuits or building blocks, are extracted and optimized using an HSPICE circuit simulator. After extracting the model parameters, the characteristic prediction of different test structures is performed to verify the circuit model. Then, the model verification, self-resonant frequency (SRF), inductance (L), and quality (Q) factor are estimated, as are the characteristic variations of inductors composed of different building blocks.

II. Test Structure Description

Test structures were fabricated in a twelve-layer LTCC process. All test structures were designed to have an upper and a lower conductor on different layers. Both conductors were separated by six layers of ceramic tape to reduce coupling capacitance between the conductors, and were connected by a stacked via such that a solenoid pattern of current flow through the structure was realized. The bottom conductor had a layout with an angle to facilitate connections between via stacks connecting the layers. A schematic diagram of the test structures is shown in Fig. 1. For all the test structures, the metal conductor was designed to be 10 mils wide.

The test structures are categorized by the spacing between adjacent coil patterns and the shape. For the four loose test structures (L), that is, 1-L, 2-L, 3-L, and 4-L, shown in Fig. 1, the spacing between adjacent coil patterns were designed to be 30 mils, whereas the spacing for the four dense test structures (D), that is, 1-D, 2-D, 3-D, and 4-D, also shown in Fig. 1, were designed to be 10 mils. In addition, for both loose and dense test structures, test structure 1 was constructed as a 3-D straight-line-shape inductor, while the rest of the test structures were constructed as 3-D serpentine-shape inductors with a different number of links. In this paper, test structures 1 and 2 were used for inductor modeling, and test structures 3 and 4 were used to predict the characteristics, which can verify the circuit model of inductors.

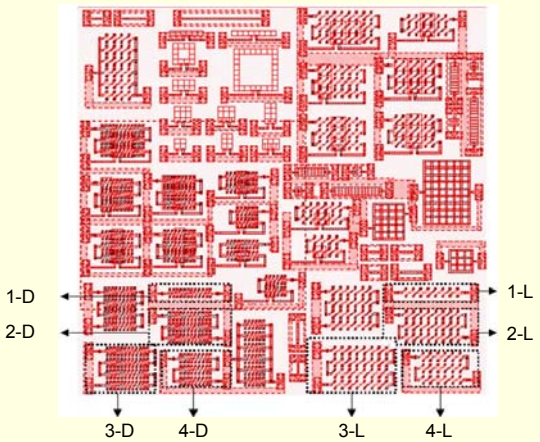

Fig. 1. Schematic diagram of test structures.

III. Processing and Measurement

The LTCC structure was physically designed using integrated circuit design tools within the Cadence Virtuoso design environment. The design was fabricated at the National Semiconductor Corporation's LTCC fabrication facility. The size of the completed coupon was approximately 2.25 in x 2.25 in. Twelve-layer test structures were fabricated. The design utilized twelve layers of ceramic tape with a dielectric constant of 7.8. Each layer of tape was 3.6 mils thick. Metal lines were drawn 10 mils wide, and the via had a diameter of 5.6 mils. Interconnectivity between layers was achieved using a stacked via. The embedded structures were accessed using ground-signal-ground probe pads on the exposed top layer, with signals reaching the embedded layers through the via. A complete test structure coupon is shown in Fig. 2.

The test structures were measured using standard network analysis techniques. Since very low-loss metal was used in the manufacturing process, dc resistance measurements were unreliable and not used. For high-frequency measurements, an HP 8510C network analyzer was used in conjunction with a Cascade Microtech probe station and ground-signal-ground configuration probes. Calibration was accomplished using a standard substrate and utilization of the line-reflect-match calibration method. The s-parameters were collected for each of the test structures at over 201 frequency points between 50 MHz and 5 GHz.

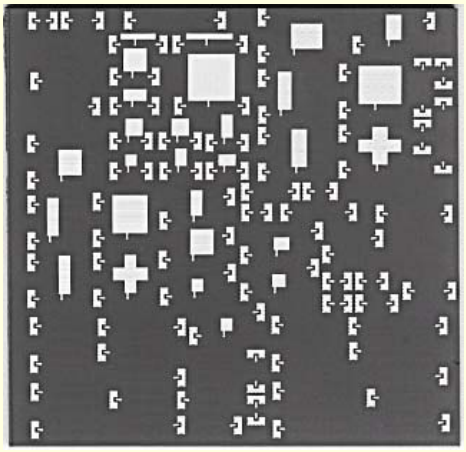

Fig. 2. A complete test structure coupon (only top layer is visible).

IV. Modeling Scheme

A novel method of full 3-D solenoid inductor modeling and simulation has been utilized. This method is based on the

generation of passive circuit element models [10]. This approach first determines a set of fundamental circuit building blocks for the inductors, and test structures are then designed and fabricated, and their s-parameters measured up to a desired frequency. Afterwards, the electrical contribution to the overall inductor response by individual building blocks is determined. Partial equivalent circuit models of each building block are then extracted using a hierarchical extraction procedure. These building-block equivalent circuits are then used to construct a 3-D solenoid inductor circuit that is geometrically comprised of the blocks. Simulation of the constructed circuit using an HSPICE circuit simulator provides an accurate prediction of the behavior of the test structure in a fraction of the time and using far fewer resources than the traditional EM/RF solution methodology. The model of the test structure is then verified experimentally by comparing the predicted response with that measured directly from the manufactured structure.

The first step involved in the modeling procedure was a determination of what types of structures and geometries were to be modeled. As mentioned above, four test structures with different dimensions were considered. Modeling of 3-D solenoid inductors is very important to ensure that they function as intended at high frequencies. Solenoid inductor modeling using the hierarchical technique required only three building blocks: a probe pad, 3-D sequential inductor coil, and 3-D linked inductor coil block. A standard partial element equivalent circuit is illustrated in Fig. 3. In addition, the mutual inductance and capacitance between two sequential building blocks can be considered for test structures 2, 3 and 4. As a

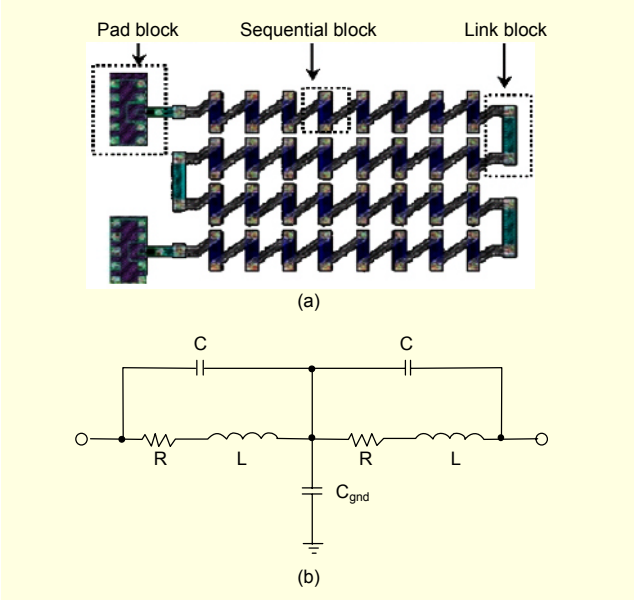

Fig. 3. Basic building block definition and its partial element equivalent circuit: (a) schematic diagram of basic building blocks and (b) partial element equivalent circuit.

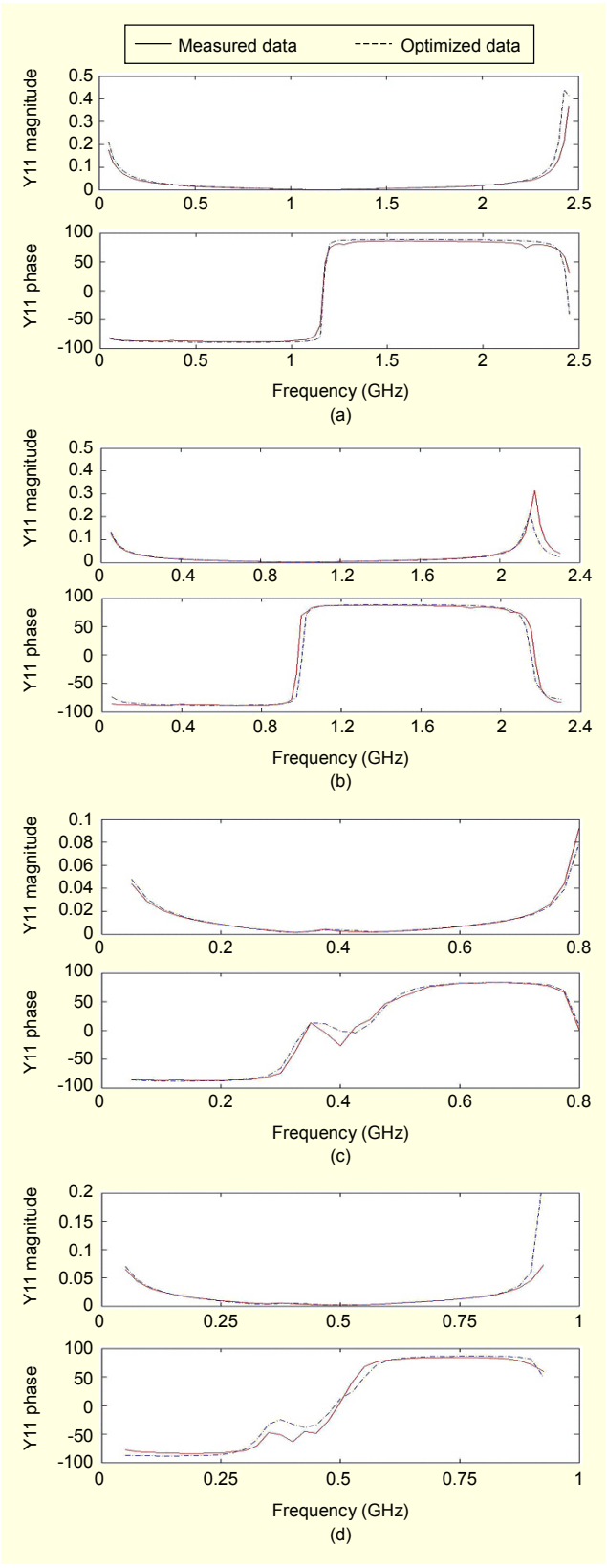

Fig. 4. Test structure optimization results of Y11 (magnitude) and Y11 (phase) for (a) test structure 1-L, (b) test structure 1-D, (c) test structure 2-L, and (d) test structure 2-D.

Table 1. Summary of extracted circuit model parameters and statistics.

	Test structure 1-L	Test structure 1-D	Test structure 2-L	Test structure 2-D	Mean value	Standard deviation
R_{pad} (Ω)	1.48E-01	6.25E-01	3.20E-01	1.00E-01	2.61E-01	2.14E-01
L_{pad} (H)	3.79E-10	1.34E-09	4.01E-10	2.75E-09	9.10E-10	8.25E-10
C_{pad} (F)	1.50E-11	1.89E-12	4.42E-10	5.69E-12	1.38E-10	2.52E-10
R_{esq} (Ω)	1.00E-03	1.00E-03	1.41E-02	1.38E-01	1.86E-09	4.37E-09
L_{seq} (H)	9.00E-10	7.84E-10	6.79E-09	5.22E-09	3.06E-09	2.93E-09
C_{seq} (F)	3.94E-13	4.82E-13	1.99E-12	5.20E-12	1.52E-12	1.49E-12
R_{lin} (Ω)			6.10E+01	6.10E+01	6.10E+01	0.00E+00
L_{lin} (H)			8.90E-08	8.90E-08	8.90E-08	0.00E+00
C_{lin} (F)			1.16E-12	1.16E-12	1.16E-12	0.00E+00
L_{mut} (H)			1.13E-08	2.22E-08	1.40E-08	7.38E-09
C_{mut} (F)			3.94E-13	1.10E-13	3.23E-13	2.74E-13

result, a mutual inductor (L_{mut}) and mutual capacitor (C_{mut}) are added between the sequential building blocks.

The equivalent circuits of building blocks are symmetry structures, and the equivalent circuits of all basic building blocks have the same structure. Parameter extraction and optimization of all test structures composed of each building block are achieved in the first resonance frequency bandwidth because an inductor behaves as an inductor in the frequency range below the first resonant frequency, and parasitic effects can be minimized at a higher frequency.

The extraction of the circuit model parameters was achieved and compared with measured s-parameters and the modeled s-parameters by the HSPICE circuit simulator on a Sun Ultra-Sparc workstation. Four test structures each of test structures 1 and 2 were optimized with respect to measured s-parameters, and their individual building block equivalent circuit model parameters were extracted. However, for inductors, Y-parameters are more informative than S-parameters. Therefore, Y-parameters for all test structures were calculated using S to Y conversion equations [11]. After the circuit models of embedded inductors are obtained, the model verification process is performed using predictive modeling for test structures 3 and 4.

Afterward, the characteristics of embedded inductors are investigated using the inductor circuit models. Here, the variation of the self-resonant frequency, inductance (L), and quality factor (Q) are examined as the main factors. The inductance and Q-factor were calculated using the following equations [12],

$$\text{Inductance (L)} = \frac{2\pi f}{\text{Im}[Z_{in}]},$$

$$\text{Quality Factor (Q)} = \frac{\text{Im}[Z_{in}]}{\text{Re}[Z_{in}]}.$$

V. Results and Discussion

Figure 4 shows the measured versus optimized results of input admittance for test structures 1 and 2 for both loose and dense structures. As seen in the plots, very good agreement has been obtained for both magnitude and phase of Y11 for the test structures. The extracted circuit model parameters and statistics are summarized in Table 1. Note that abrupt jumps in the phase graph in Figs. 4(c) and 4(d) were observed, which may come from the parasitic effect of the link block.

We observed that the inductance values of the test structures are well-matched in all cases. However, some errors are contained for the Q-factors for all cases since measurement noise and the tolerance of parasitic effects can be involved.

After the partial-element equivalent-circuit models of embedded inductors were constructed, the characteristic prediction of embedded inductors was then performed as a means of model verification. The circuit model parameters in Table 1 were then applied to test structures 3 and 4 to verify the circuit model of the inductors. The results of predictive modeling of test structures 3 and 4 are shown in Fig. 7.

As can be seen in Fig. 7, the prediction results are well-matched with the measured data, indicating that the inductor circuit models represent the inductor characteristics very well.

After the model verification, the effects of different test structures on the characteristics of the inductors were investigated. Since the geometry of embedded passives are restricted by the dimension of the chip in the IC design phase, the variations of the number of link and sequential blocks are thus considered as the main factors of the variation used in the HSPICE circuit simulation. For the loose and dense test structures, the circuit model parameters were used for each test structure previously extracted. A test structure without link

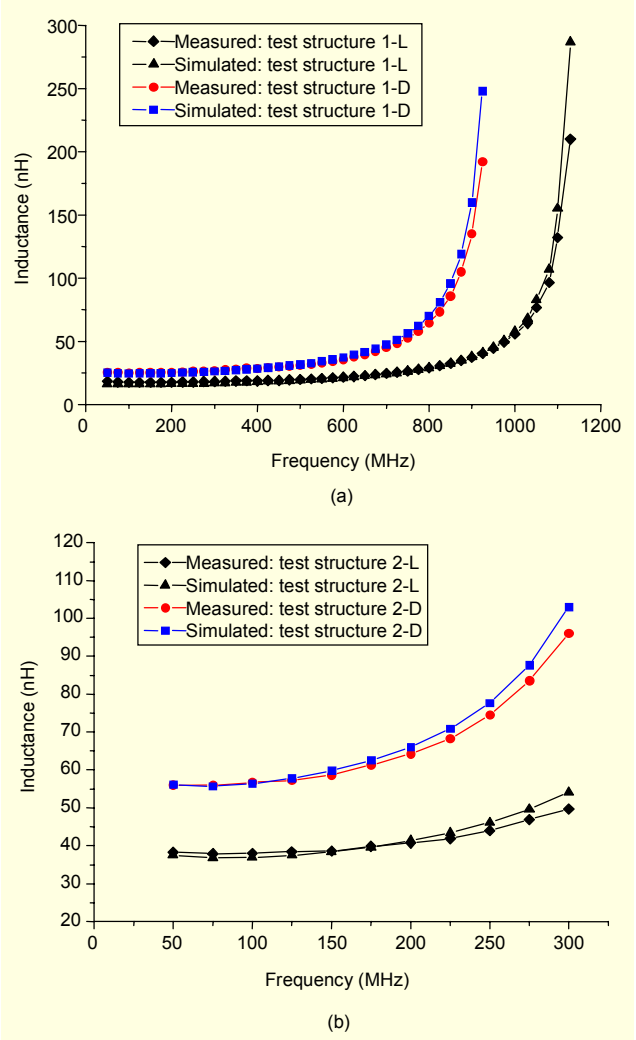

Fig. 5. Inductance comparison of the measured versus simulated data for (a) test structure 1 and (b) test structure 2.

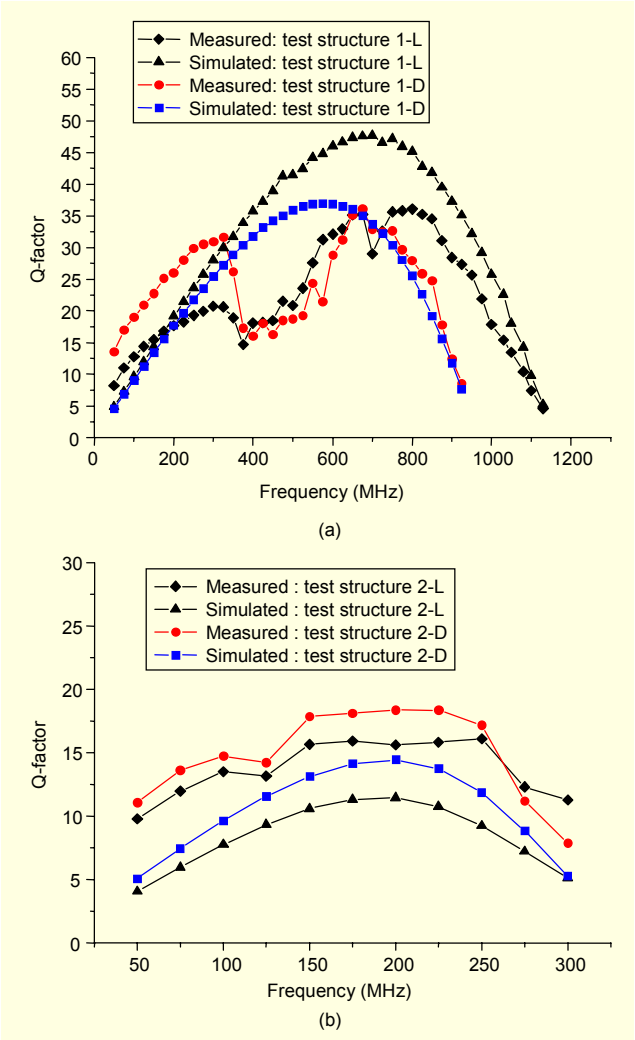

Fig. 6. Q-factor comparison of the measured versus simulated data for (a) test structure 1 and (b) test structure 2.

block was constructed as a 3-D straight-line-shape inductor. A test structure with k link blocks was constructed as a 3-D serpentine-shape inductor consisting of series-connected k sequential blocks.

The estimation results of inductor characteristics with different numbers of link and sequential blocks are presented in Figs. 8 through 10.

Figure 8 shows the effects of the number of link and sequential blocks on the SRF.

We observed that the SRF decreases as the number of sequential blocks or the number of link blocks is increased.

Figure 9 shows the effects of the number of link and sequential blocks on the inductance. We observed that the inductance generally increased as the total number of sequential blocks is increased. However, the number of link blocks crucially impacts on the inductance. In addition, the self-resonant frequency of the inductor with 2 link blocks is below 1 GHz, so this type of inductor can only be used for baseband circuit applications. For wireless local area network applications, the link block should be carefully designed to improve the self-resonant frequency of the inductors.

The inductance can be categorized by two components, self inductance and mutual inductance. The mutual inductance is positive or negative depending on the current flows in parallel microstrip lines. If the current flows of two adjacent microstrip lines are in a meander shape, and the current flows are in the opposite direction, a negative mutual inductance is obtained [13]. The test structure containing no link block has only self inductance. In this case, the inductance increases as the number of sequential blocks is increased. In the case of the test structure with one link block, it has self inductance along with a negative mutual inductance. As the number of sequential blocks is increased, the inductance is almost constant since the increment of the self inductance is almost comparable with the increment

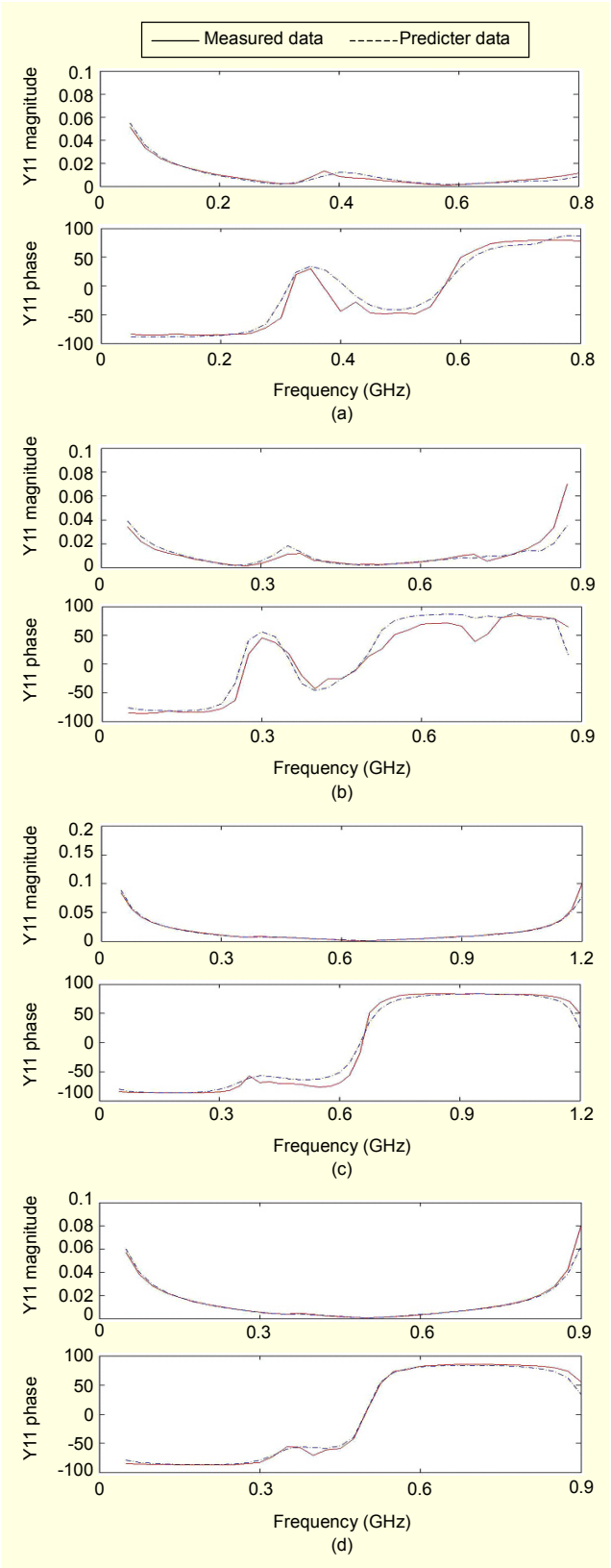

Fig. 7. Predictive modeling results of Y11 (magnitude) and Y11 (phase) for (a) test structure 3-L, (b) test structure 3-D, (c) test structure 4-L, and (d) test structure 4-D.

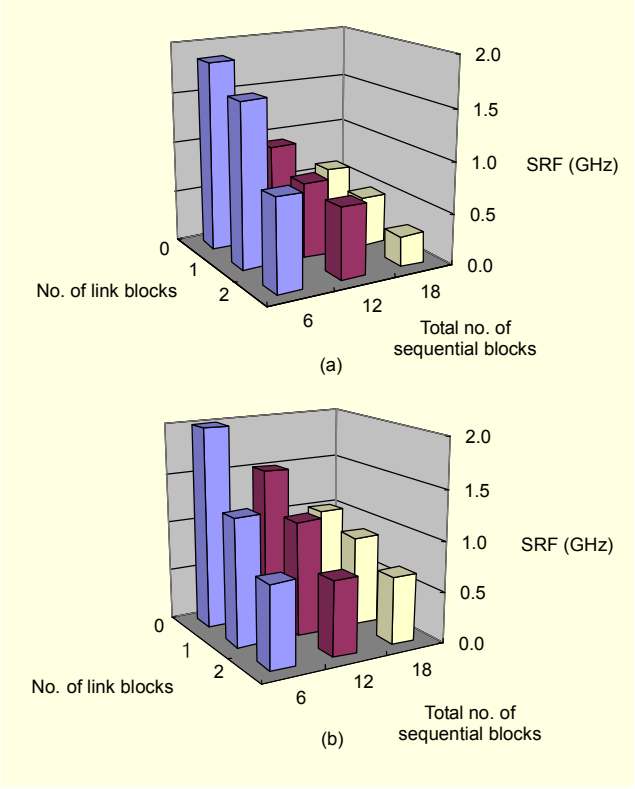

Fig. 8. Performance prediction results of self-resonant frequency for (a) loose and (b) dense structures.

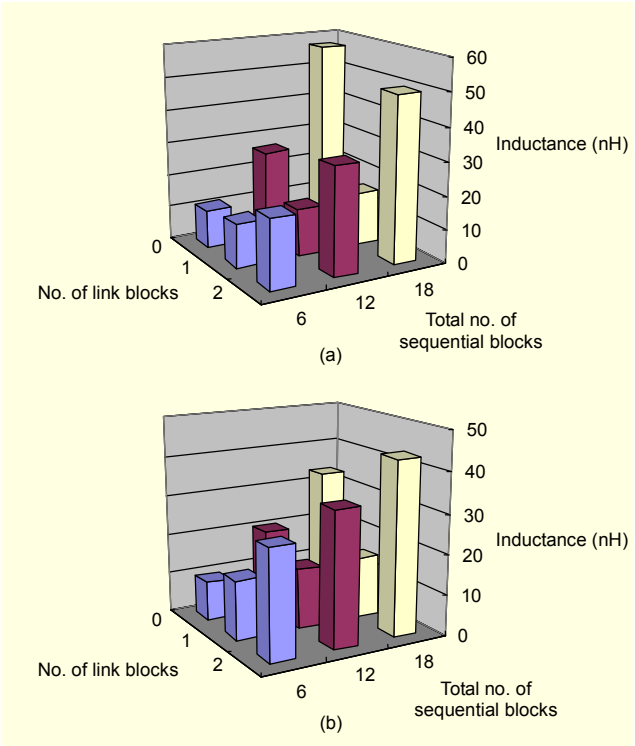

Fig. 9. Performance prediction results of inductance for (a) loose and (b) dense structures.

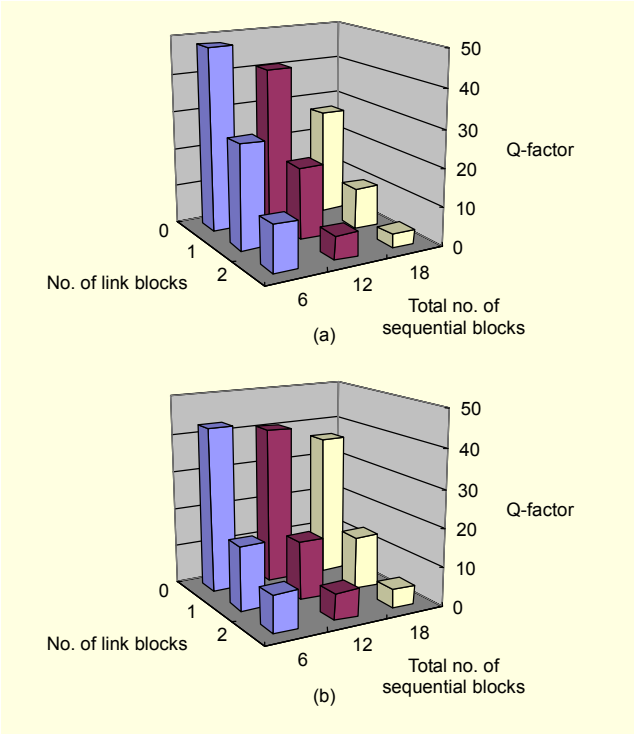

Fig. 10. Performance prediction results of Q-factor for (a) loose and (b) dense structures.

of the negative mutual inductance.

However, for the test structure with two link blocks, the negative mutual inductance is alleviated by the other parallel sets of sequential blocks with the same current flows so that the self inductance is dominant compared with the mutual inductance. In addition, note that the inductance of the link block (L_{lin}) is larger than the inductance of the sequential block (L_{seq}) or the mutual inductance (L_{mut}) in Table 1. As a result, the inductance of the test structure with two link blocks exhibits the largest inductance among the test structures.

Figure 10 shows the effects of the number of link and sequential blocks on the Q-factor. We observed that the Q-factor decreases as the number of sequential blocks or the number of link blocks is increased. Also note that the Q-factor is mainly impacted by the number of link blocks, and the effect of the sequential blocks is negligible.

VI. Conclusion

In this paper, modeling and characteristic prediction of 3-D embedded solenoid inductors has been investigated using a partial-element equivalent-circuit method. The extraction of the circuit model parameters was achieved in an HSPICE circuit simulator. Both loose and dense test structures were used for the circuit modeling of embedded inductors, and the two different structures were used to verify the circuit model. After the model verification, the characteristic variation of embedded inductors, such as the self-resonant frequency, inductance, and Q-factor were investigated with different structures. This approach could potentially be extended to allow device designers to predict the performance and parametric yield of a given device. Furthermore, even a small number of test structures provide the relevant circuit model to allow characteristic prediction.

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