Circuit Modeling of Interdigitated Capacitors Fabricated by High-K LTCC Sheets

Kilhan Kim, Min Su Ahn, Jung Han Kang, and Ilgu Yun

The circuit modeling of interdigitated capacitors fabricated by high-k low-temperature co-fired ceramic (LTCC) sheets was investigated. The s-parameters of each test structure were measured from 50 MHz to 10 GHz, and the modeling was performed using these measured s-parameters up to the first resonant frequency. Each test structure was divided into appropriate building blocks.

The equivalent circuit of each building block was composed based on the partial element equivalent circuit (PEEC) method. Modeling was executed to optimize the parameters in the equivalent circuit of each building block. The validity of the extracted parameters was verified by the predictive modeling for the test structures with different geometry. After that, Monte Carlo analysis and sensitivity analysis were performed based on the extracted parameters. The modeling methodology can allow a device designer to improve the yield and to save time and cost for the design and manufacturing of devices.

Keywords: LTCC, embedded passives, PEEC, circuit model.

I. Introduction

As the wireless communication system continues to progress, higher levels of integration, smaller size, lower weight, lower power consumption, higher performance, and lower product costs are required. The development of the future communication system is leading the rapid growth of radio frequency integrated circuits (RFICs). Embedded passives are attractive for RFICs due to the compactness and integration of the system [1]-[4]. Passive devices are not only very important in many electronic systems and circuits, but they also take up larger portions than the active devices in the aspects of size and numbers. The ratio of these passive devices is around 80% in the chip area, and even as close as 95% in the chip area for some cases [5]. Integrated or embedded passives have many advantages such as a reduction of size, performance improvement, the removal of defects like solder joint failure, and the realization of high reliability [6].

Suitable processes for embedding passive devices are low temperature co-fired ceramic (LTCC) processes. LTCC technology has the advantages of a high packaging ratio, the use of highly conductive metals, and high reliability. LTCC technology offers multilayer packaging that enables one to embed passive devices in a multilayer manner for size reduction. Therefore, LTCC technology can be a powerful candidate for integrating passive devices [7]. The successful design of passive structures in LTCC systems requires that accurate models of the various components exist or can be easily obtained. However, most LTCC passives are electrically long and have very complex field patterns due to their full three-dimensional geometries. Thus, standard modeling methods for microstrip- or stripline-based structures cannot apply for these components. In order to design LTCC

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structures for high frequencies successfully, the behavior of the passive components that comprise the structure must be characterized accurately at those frequencies. Therefore, the extraction of an optimum set of device model parameter values is crucial for characterizing the relationship between the model and the measured data.

Recently, design and modeling issues for embedded passive devices has been investigated by many researchers. Building-block-based modeling of integrated passives was presented by Poddar and others [7]. Yun and colleagues presented accurate device model parameter optimization for embedded passive devices using genetic algorithms and studied statistical modeling of embedded capacitors [8], [9]. Zhang and others studied the modeling of embedded passives using a neural network [10]. Finally, Choi and others presented the circuit parameter extraction of embedded passive devices for network synthesis [11].

In this paper, the modeling of an embedded two-dimensional interdigitated capacitor is performed using the capacitor test structures fabricated by LTCC technology. Test structures are divided into appropriate building blocks related to their geometries based on a partial element equivalent circuit (PEEC), and the device model parameters of each building block are extracted using an HSPICE circuit simulator. After the extraction of the device model parameters, the optimum set of device model parameters are statistically verified through Monte Carlo analysis. Predictive modeling is then performed, and the crucial parameters are extracted through a sensitivity analysis.

II. Test Structure Description

A schematic diagram of the test structures for interdigitated capacitors is shown in Fig. 1. The test structures were fabricated in a 16-layer LTCC process. All of the test structures are embedded into layer 2 of the fabricated test structure.

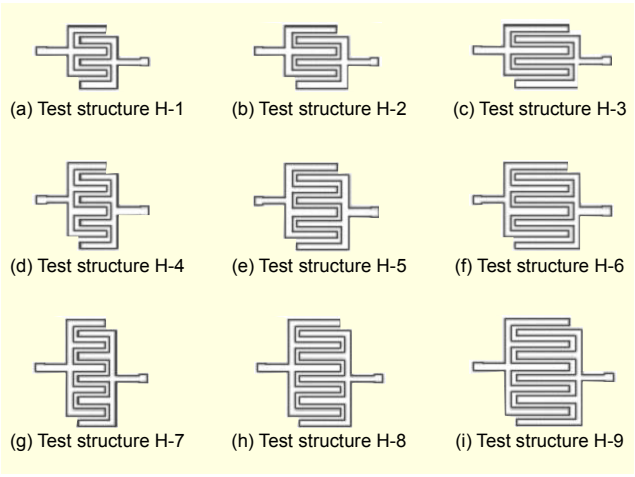

Fig. 1. Schematic diagram of interdigitated capacitors.

The interdigitated capacitors are classified by geometries such as the number and lengths of the fingers. As shown in Fig. 1, nine test structures are used for modeling. Test structures H-1, H-4, and H-7 have finger lengths of 480 μm, test structures H-2, H-5, and H-8 have finger lengths of 720 μm, and test structures H-3, H-6, and H-9 have finger lengths of 960 μm. In addition, the test structures H-1, H-2, and H-3 have six fingers, test structures H-4, H-5, and H-6 have eight fingers, and test structures H-7, H-8, and H-9 have ten fingers. In all of the test structures, the width of the metal lines is 120 μm, and the spacing between the metal lines is 80 μm. Test structures H-1, H-5, and H-9 are used for modeling, and the others are used for predictive modeling for verification.

III. Processing and Measurement

The test structure was physically designed using a commercial MyCAD design tool. LTCC sheets with a dielectric constant of 17.8 were used for fabricating the test structure. The design was fabricated at the TEMEN corporation LTCC fabrication facility. Silver, 10 μm, was deposited and used as a conductor material on 80 μm sheets. Interconnectivity between layers was achieved using stacked vias. The embedded structures had interface access using ground-signal-ground probe pads on the exposed top layer, with signals reaching the embedded layers through vias. The complete manufactured test structure is shown in Fig. 2.

The s-parameters for the test structures were measured using an Agilent 8722 network analyzer with ground-signal-ground configuration coplanar probes. DC resistance measurements were unreliable and were not used. Calibration was accomplished using a thru-reflect-match (TRM) calibration method with a calibration substrate. The s-parameters of each test structure were measured at 201 frequency points from 50 MHz to 10 GHz and stored with the aid of data acquisition software. The device model parameter extraction was accomplished using only the S- parameter data up to the first self-resonance frequency where the test

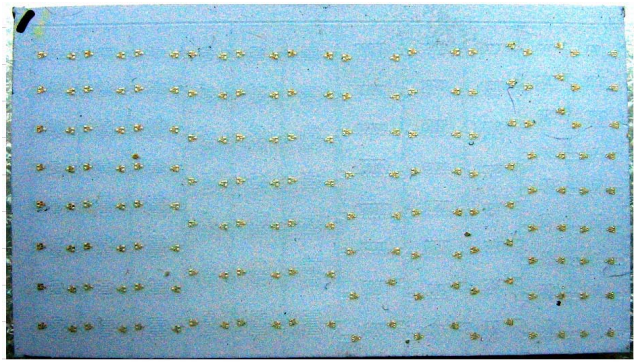

Fig. 2. LTCC test structure (only exposed top layer is visible).

structure has capacitive behavior.

IV. Modeling Scheme

A novel method of interdigitated capacitor modeling and simulation has been investigated. This modeling methodology is based on the generation of passive circuit element models. This approach first determines a set of fundamental circuit building blocks for the interdigitated capacitors. Then, test structures are designed, fabricated, and their S-parameters measured up to a desired frequency. Afterwards, the electrical contribution to the overall capacitor response by individual building block is determined. Equivalent circuit models of each building block are then extracted. These building block equivalent circuits are then used to construct an interdigitated capacitor circuit that is geometrically comprised of the building blocks. Simulation of the constructed circuit using HSPICE provides an accurate prediction of the behavior of the test structure in a fraction of the time and using far fewer resources than the traditional electromagnetic/radio frequency solution methodology. The circuit model of the test structure is then experimentally verified by comparing the predicted response with the measured response.

Due to the geometry of an interdigitated capacitor, it was estimated that fringing fields and coupling effects can exist. Therefore, parasitic elements for these non-ideal behaviors should be considered [13].

The equivalent circuit of each building block in the test structure is shown in Fig. 3. Note that each building block can be represented as the equivalent circuit of the same configuration shown in Fig. 3. However, the extracted circuit parameters are different for each building block. Also note that the capacitor indexed as C_gnd in Fig. 3 represents the capacitance between metal and grounded metal plane.

After S-parameters for the test structures were measured, circuit model parameters were extracted for the various building blocks. The overall equivalent circuits are comprised of a combination of these building blocks with modifications to take into account the building block topology and various coupling effects. The extraction of the circuit model parameters was achieved by optimization with respect to the measured S-parameter data. The optimization is completed until the residual sum of error is less than the tolerance value. The Levenberg-Marquardt (LM) method is used as the optimization algorithm. The LM method consists of the steepest descent method and the Gauss-Newton method. The steepest descent method is used for initially searching the optimization value, and the Gauss Newton method is used for searching the accurate solution. The objective function of the LM algorithm is defined as follows:

$$F_o(X)\big|_{X=(x_1,x_2,\ldots,x_n)} = \sum_{i=1}^{m}\left[\omega_i \frac{f_i(X)-F_{meas}^i}{F_{meas}^i}\right]^2. \qquad (1)$$

In (1), $X=(x_1, x_2, \cdots, x_n)$ are the component values to be extracted, n is the total number of parameters, F^i_{meas} is the measured value of the i-th model parameter, m is the total number of measurements, $f_i(X)$ is the simulated value of the i-th point, and ω_i is a weight factor for the i-th measured data point. Using the LM algorithm, the HSPICE circuit simulator finds the vector X of the device model parameters that minimizes $F_o(X)$ [14].

As mentioned above, each test structure is divided into appropriate building blocks. Based on the geometry and electrical contribution, a total of six types of building blocks are assigned. These building blocks are a pad block (pad), a sequential block 1 (seq1) representing the coupled strip line, a sequential block 2 (seq2) for the connection between pad and the body of the capacitor, a sequential block 3 (seq3) representing the coupling with edge and line, a curve block (cur) of the body, and a joint block (joi) connecting the strip line. The determined building block is shown in Fig. 4. All types of the building blocks have a cascade connection with the adjacent building blocks.

In addition, mutual inductance and coupling capacitance are also considered between fingers. Mutual inductance and coupling capacitance are inserted between the facing sequential 1 blocks. Only coupling capacitance is inserted at the spacing of the edge of sequential 1 block and the other blocks such as

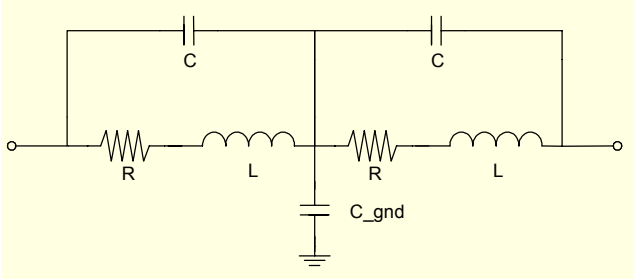

Fig. 3. The equivalent circuit of the building block.

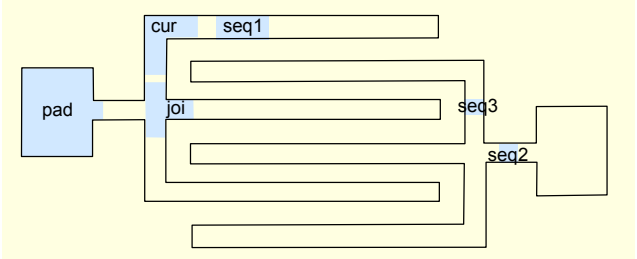

Fig. 4. The definition of building blocks in the interdigitated capacitor.

the curve block and joint block. The overall connection of the building blocks is shown in Fig. 5.

V. Results and Discussion

1. Circuit Modeling Results

Using an HSPICE circuit simulator, test structures H-1, H-5, and H-9 are modeled up to the first self-resonance frequency where the test structure behaves as a capacitor. The magnitude and phase of input admittance are calculated from the modeled s-parameters and compared with measured S-parameter data.

As shown in Fig. 5, the modeled data are well matched with the measured data. The important characteristics of the capacitors are the capacitance value and self-resonance frequency. Since it is hard to observe the capacitance value and self-resonance frequency using s-parameters, the modeled and measured data are plotted in the input admittance (Y11) parameters.

The extracted parameters are listed in Table 1. As shown in Table 1, the capitalized symbol means the passive elements in each building block, and the symbol in a subscript represents the building block itself. Parasitic element 1 represents the parasitic effects between the sequential 1 blocks, and parasitic element 2 denotes the parasitic element between sequential blocks 1 and 3. Parasitic element 3 shows the parasitic elements between sequential block 1 and the curve block, or sequential block 1 and the joint block. The statistics of the extracted parameters are also listed. The mean and mean-absolute deviation of the extracted parameters are calculated from (2) and (3). These parameters are used to perform a Monte Carlo analysis in order to determine the statistical validity of the extracted parameters.

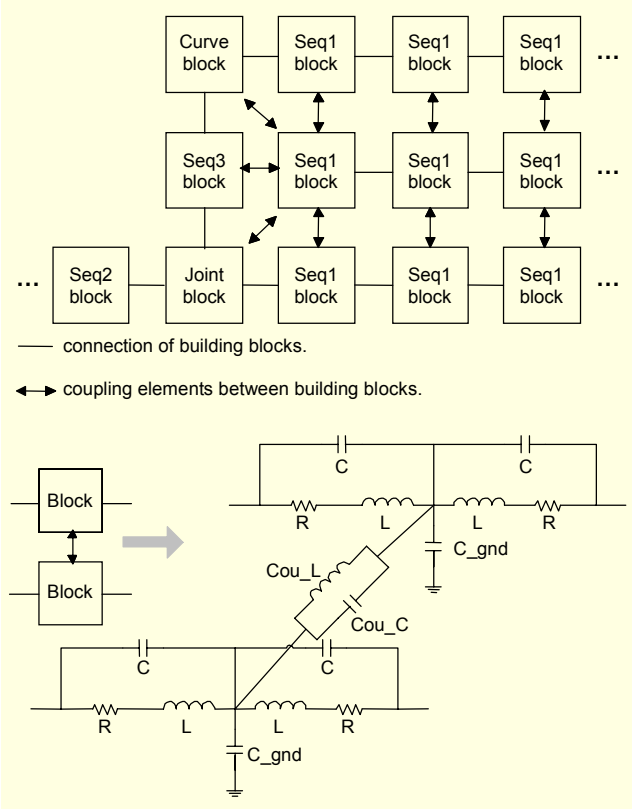

Fig. 5. Equivalent circuits associated with building blocks for test structures.

Table 1. The modeled circuit parameters of the test structures H-1, H-5, and H-9 in the interdigitated capacitor.

Parameters	H-1	H-5	H-9	Mean	MAD
Lcou1 (H)	7.85E-03	3.48E-03	1.60E-03	4.31E-03	2.36E-03
Ccou1 (F)	2.65E-14	3.06E-14	3.05E-14	2.92E-14	1.80E-15
Ccou2 (F)	1.32E-17	1.00E-17	1.00E-17	1.11E-17	1.42E-18
Ccou3 (F)	1.56E-17	1.02E-17	1.55E-17	1.38E-17	2.37E-18
Rcur (Ω)	1.83E-03	1.73E-03	1.90E-03	1.82E-03	6.16E-05
Lcur (H)	1.48E-09	2.65E-09	4.17E-09	2.77E-09	9.37E-10
Ccur (F)	3.57E-17	3.55E-17	4.14E-17	3.76E-17	2.58E-18
Rjnt (Ω)	9.00E-01	8.98E-01	7.48E-01	8.49E-01	6.74E-02
Ljnt (H)	1.00E-08	7.05E-09	7.25E-09	8.10E-09	1.27E-09
Cjnt (F)	1.47E-17	1.41E-17	1.36E-17	1.41E-17	4.02E-19
Rpad (Ω)	5.00E-02	2.29E-02	2.05E-02	3.11E-02	1.26E-02
Lpad (H)	1.51E-10	1.64E-10	1.65E-10	1.60E-10	6.11E-12
Cpad (F)	2.06E-10	3.84E-10	3.80E-10	3.23E-10	7.85E-11
Rseq1 (Ω)	9.00E-01	6.99E-01	4.18E-01	6.73E-01	1.69E-01
Lseq1 (H)	3.88E-13	3.70E-13	5.00E-14	2.69E-13	1.46E-13
Cseq1 (F)	5.00E-11	1.13E-10	1.57E-10	1.07E-10	3.79E-11
Rseq2 (Ω)	1.98E-03	1.11E-03	1.01E-03	1.36E-03	4.11E-04
Lseq2 (H)	1.47E-14	1.19E-14	5.00E-14	2.55E-14	1.63E-14
Cseq2 (F)	1.17E-10	1.62E-10	5.00E-11	1.09E-10	3.96E-11
Rseq3 (Ω)	1.75E-02	1.21E-02	2.48E-02	1.81E-02	4.45E-03
Lseq3 (H)	5.19E-15	5.00E-15	9.16E-15	6.45E-15	1.81E-15
Cseq3 (F)	1.29E-10	1.28E-10	4.56E-10	2.38E-10	1.46E-10

$$\text{Mean} : \frac{\sum_{i=1}^{n} x_i}{n} \tag{2}$$

$$\text{Mean Absolute Deviation (MAD)} : \frac{\sum_{i=1}^{n} |\mu - x_i|}{n} \tag{3}$$

2. Predictive Modeling

Since the modeling data are in good agreement with the measured data of the test structures, the validity of the extracted

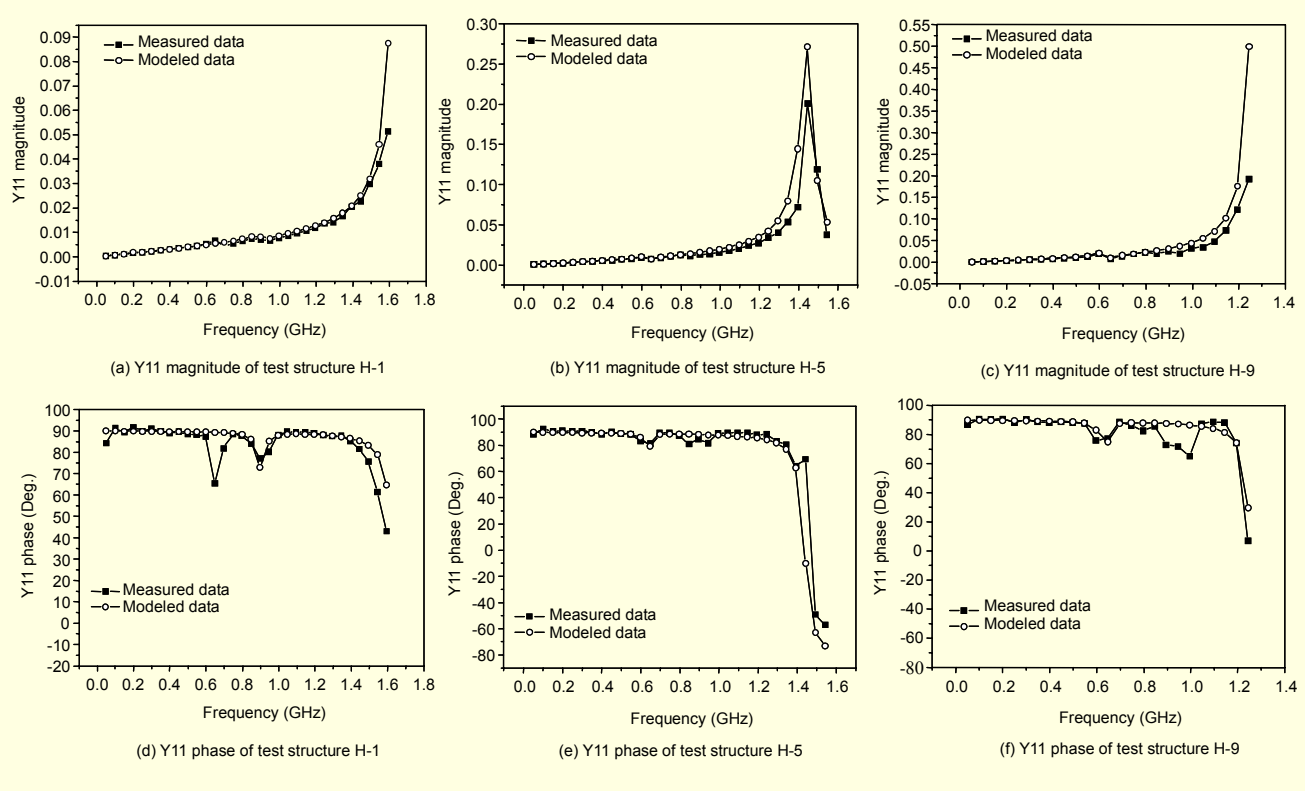

Fig. 6. Modeling results of the test structures H-1, H-5, and H-9.

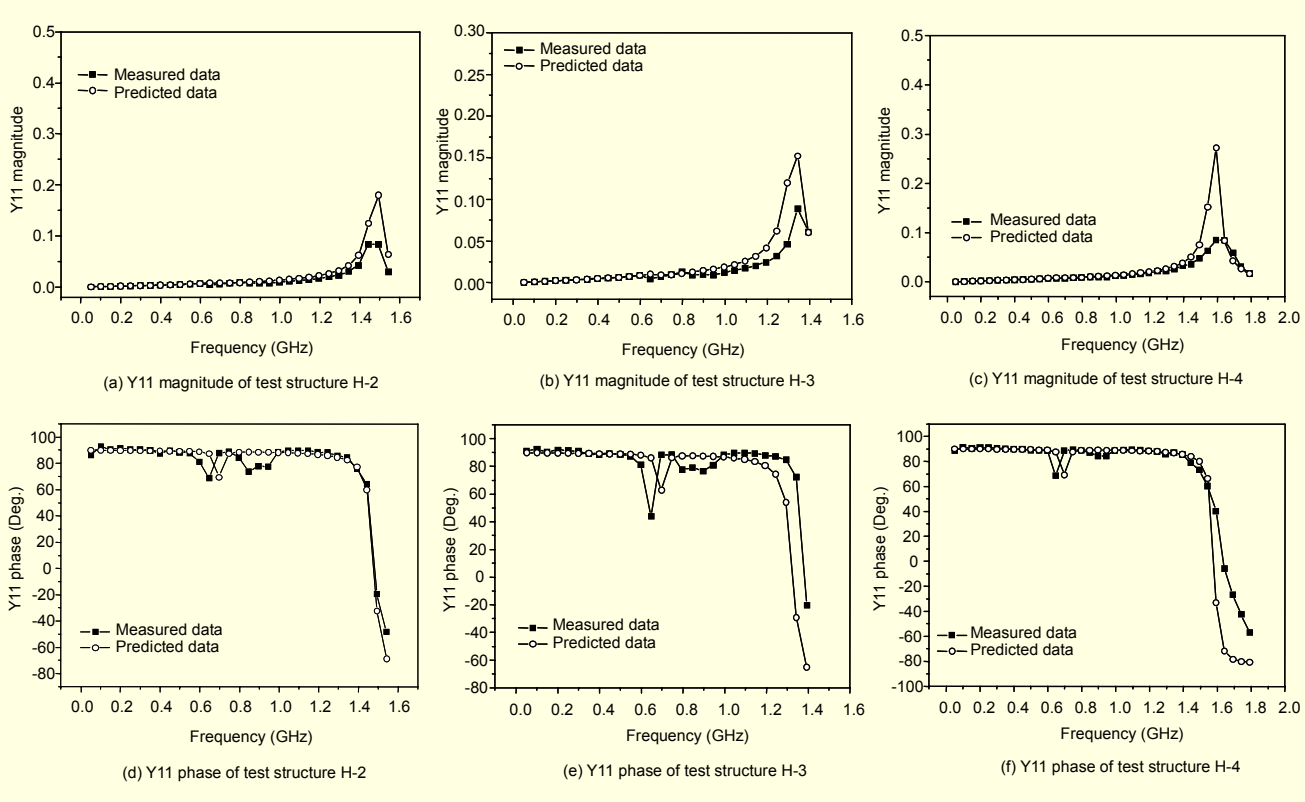

Fig. 7. Predictive modeling results of the test structures H-2, H-3, and H-4.

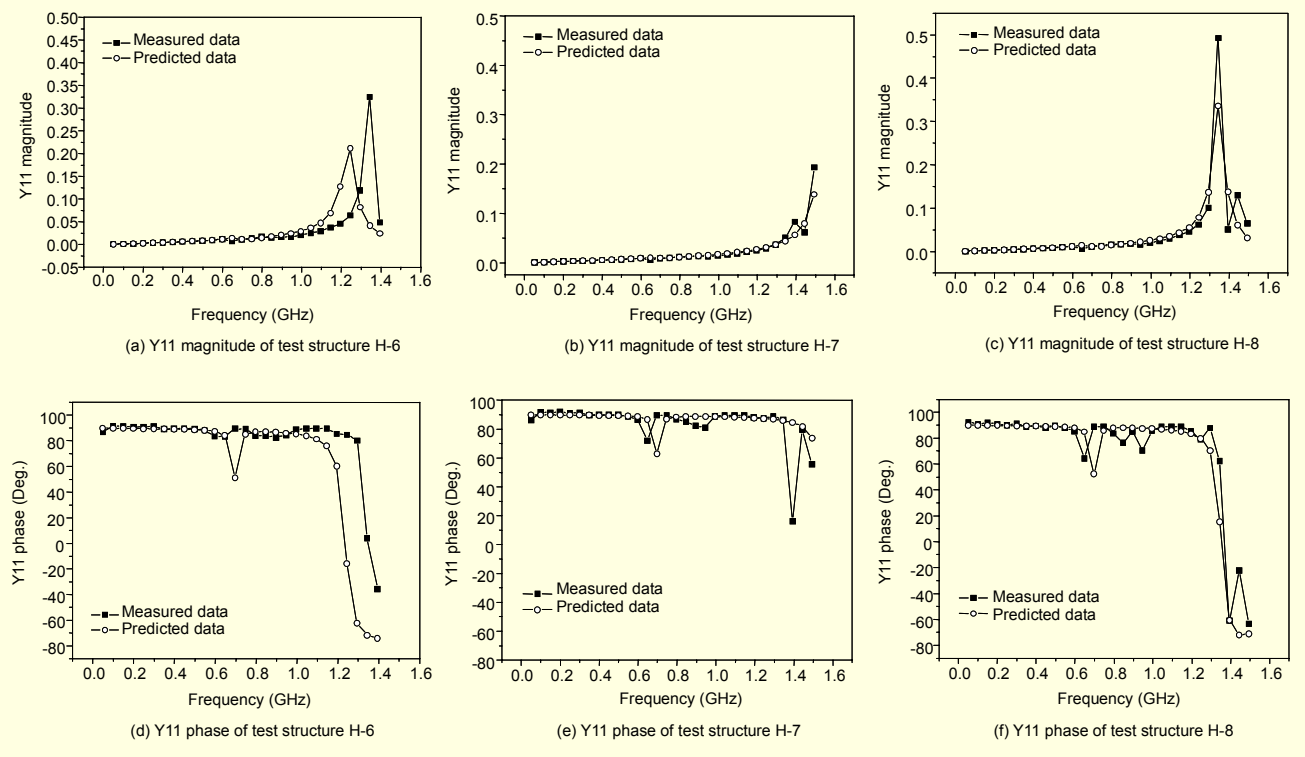

Fig. 8. Predictive modeling results of the test structures H-6, H-7, and H-8.

parameters cannot be confirmed. Here, predictive modeling is performed to verify the extracted parameters. Test structures H-2, H-3, H-4, H-6, H-7, and H-8 are used for the predictive modeling. As the starting procedure of the predictive modeling, the equivalent circuit model for each building block including parasitic building block is extracted from the test structures H-1, H-5, and H-9. The equivalent circuits of the test structures H-2, H-3, H-4, H-6, H-7, and H-8 are then constructed using the extracted building block circuits. Finally, Y11 parameters of the test structures from 50 MHz to each first self-resonant frequency are extracted and compared with the measured data.

The results of predictive modeling are shown in Figs. 6 through 8. Observe that the predicted data are well matched with the measured data. The "■" symbols represent the measured data, and the "○" symbols represent the predicted modeled data. Based on the predictive modeling results, the validity of the extracted circuit parameters is confirmed, and the extracted circuit parameters can be applied to any test structure with a combination of extracted building blocks.

3. Monte Carlo Analysis

After extracting the modeled parameters, to predict the statistical variations in actual fabricated devices, a Monte Carlo simulation is performed using HSPICE. To improve the recurrence of the parameters, the statistics are extracted from all

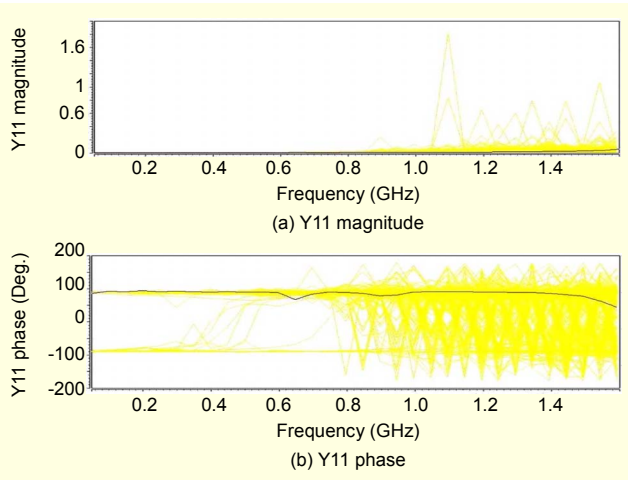

Fig. 9. Monte Carlo analysis results of the test structure H-1.

of the test structures. All of the test structures are modeled, and the mean and the mean-absolute deviations for each extracted circuit parameter are extracted from the modeled data. The Monte Carlo simulation is performed under the Gaussian distribution of each circuit parameter. Initially, 500 sets of input admittance curves are generated using the information of the mean and mean-absolute deviation, which is assumed to be a Gaussian distribution. Afterwards, the output response (that is, Y11 parameters) for each test structure was obtained and compared with measurement data to determine if the statistical

variation of circuit model parameter values was in the range of the Monte Carlo output.

The results of the Monte Carlo simulations for the test structures H-1, H-5, and H-9 are illustrated in Figs. 9 through 11. The sets of the curves represent Monte Carlo outputs, and the two black lines are the measured Y11-parameter. Measured data reside in the curves generated by Monte Carlo analysis. From these results, the extracted parameters have sufficient statistical confidence. Based on the Monte Carlo analysis results, it has been demonstrated that the variations in the complete equivalent circuit models for the test structures based only on the circuit building blocks can be used to predict such variations in actual fabricated devices. Also, these results reveal that even a small number of test structures provide sufficient statistical variation of component values to allow for the prediction of performance variation of a larger population.

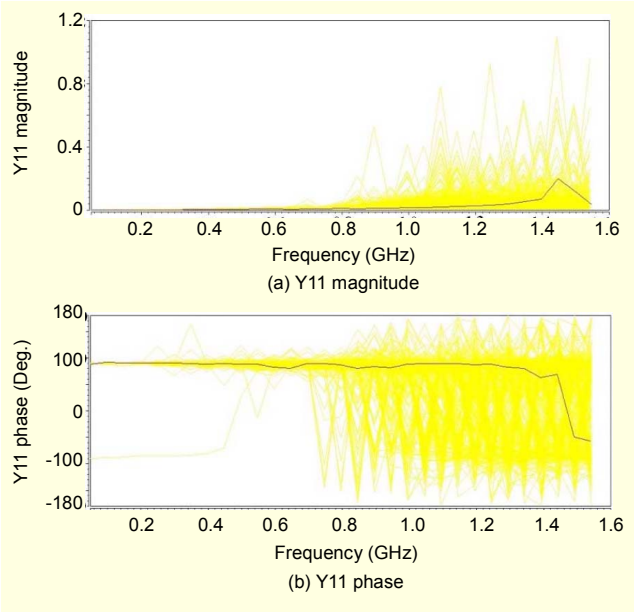

Fig. 10. Monte Carlo analysis results of the test structure H-5.

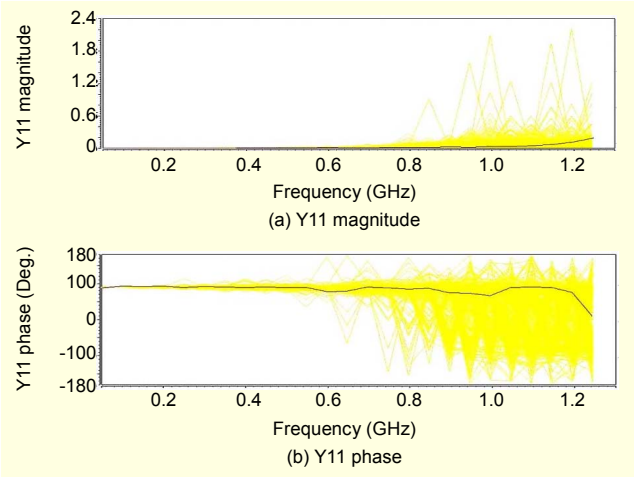

Fig. 11. Monte Carlo analysis results of the test structure H-9.

4. Sensitivity Analysis

In order to determine the impact of the circuit parameters on the performance metrics, a sensitivity analysis is performed. The important performance metrics of the capacitors are the capacitance and self resonance frequency (SRF). Through the sensitivity analysis, the influence of the most effective parameters for each performance metric is verified. As an illustration, the sensitivity analysis of the test structure H-9 is performed. The capacitance and SRF by the 10% variation of inductance value in the link block and the coupling capacitance between sequential 1 blocks are shown in Fig. 12.

From the results of the sensitivity analysis, most effective parameters are clarified as the inductance element of the joint block and the coupling capacitance element between sequential 1 blocks. Therefore, the design of the joint block and coupling effect can be carefully determined to maintain the desired

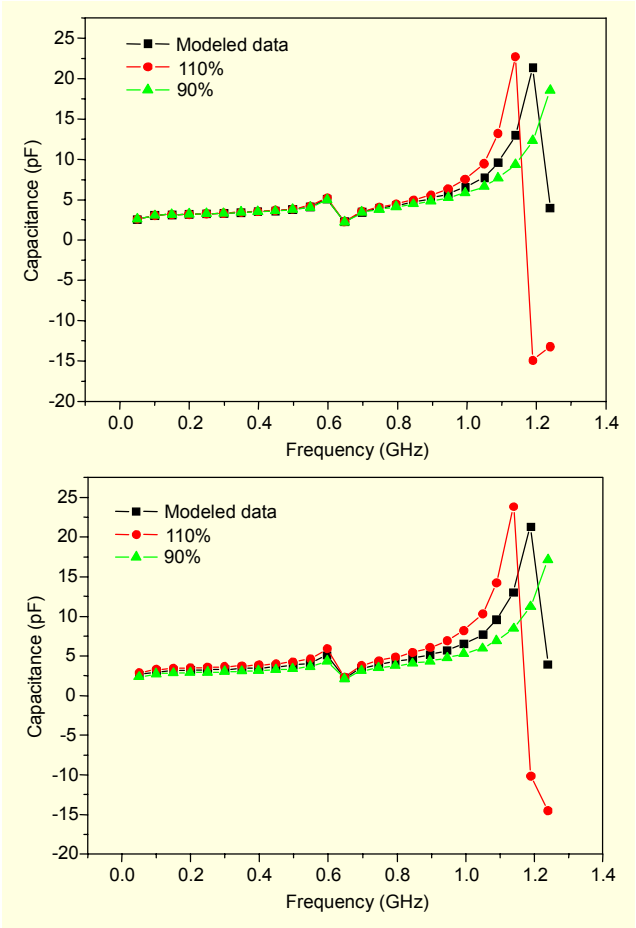

Fig. 12. The characteristic variation of the test structure H-9 (a) due to the inductance of the joint block and (b) due to the coupling capacitance between sequential 1 blocks.

performance metrics of the interdigitated capacitors.

VI. Conclusion

In this paper, the design, fabrication, modeling, and simulation of interdigitated capacitors were investigated. An accurate model of the test structures fabricated by LTCC technology can be achieved based on the partial equivalent building block method. The parameters of equivalent circuits were extracted using an HSPICE circuit simulator. Afterward, predictive modeling was performed to verify the validity of the modeled parameters. The variations in actual fabricated devices were predicted by Monte Carlo analysis, and a sensitivity analysis was studied to verify the most crucial parameters on the performance metrics of the test structures.

This modeling methodology can potentially give many advantages to device designers. At first, performance metrics can be predicted for any test structures composed of extracted building blocks without the fabrication of the given devices. Secondly, a parametric yield and performance variations of the given devices can be predicted with a small number of test structures. Finally, this modeling methodology gives the opportunity to improve the performance metrics of the given devices to analyze the crucial circuit parameters on the performance metrics through the sensitivity analysis. Therefore, this modeling methodology can allow device designers to improve the parametric yield and to provide cost-effective manufacturing of devices.

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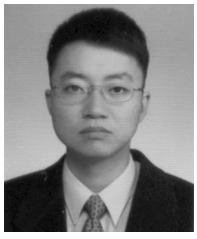

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