: IP Catalog

SIPAC

2006년 2월부터 4월 초까지 50개의 IP가 SIPAC에 새로 등록되었습니다. 지면관계상 18개의 IP의 정보를 제공해 드리며, SIPAC 홈페이지(http://www.sipac.org)를 방문하시면 그 외 IP에 대한 보다 다양하고 자세한 정보를 보실 수 있습니다. (Total: 1977 개)

No.	IP Name (Type/Format)	Seller	Category	Description
1	LC Quadrature VCO using the 2nd harmonic freq (Hard IP/GDS II)	ICU (www.icu.ac.kr)	Analog & Mixed Signal	LC Quadrature VCO using the 2nd harmonic freq
2	1Gb/s Ethernet PON MAC Chipset (EPMC & EPSC) (Soft IP, Firm IP / VHDL, Verilog)	ETRI (www.etri.re.kr)	Wireline Communication	The DCM 802.11 MAC is a high performance, interoperable, and easy to configure solution for 802.11 products
3	24 Channel GPS L1-CA correlator (Soft IP / VHDL)	Konkuk University (www.konkuk.ac.kr)	Digital Signal Processing	The general structure of GNSS receiver consists of RF front end, DA-converter, multi channel correlator, and μ-processor. Correlator performs tracking under control of μ-processor, and μ-processor get navigation solution using tracking information from correlator. This IP is 24 channel GPS L1-CA correlator.
4	802.11i AES-CCM Core (Soft IP, Firm IP / VHDL, Verilog)	Elliptic Semiconductor (www.ellipticsemi.com)	Peripheral Core	AES-CCM Core for 802.11a/b/g/n applications. Two core sizes - 11,000 gates for 300 Mbps, 27,000 gates for 802.11n Provides AES-CTR mode for encryption Provides AES-CTR with CBC MAC for message authentication
5	I2C (Soft IP / VHDL)	Microtronix Datacom (www.microtronix.com)	Bus Interface	This IP Core is a complete I2C solution for the Altera Nios II soft-core processor. It supports three modes of operation: Avalon I2C Master controller, Avalon I2C Slave controller and an 8-bit PIO Slave device. Normal: 100Kbps, Fast: 400Kbps and High-Speed: 3.4Mbps transmission speeds are supported. The I2C IP Master/Slave core is Altera SOPC Builder ready and integrates easily into any SOPC Builder generated system.
6	AMBA SOC Platform- Configurable (Soft IP / Verilog)	Aurora VLSI, Inc. (www.auroravlsi.com)	Platform IP > General Purpose	The AMBA Bus SOC Platform is a configurable AMBA Bus platform with several popular peripherals and system functions. It provides a baseline SOC implementation to which designers add the ARM processor, their proprietary hardware, and other third party IP of their choice.
7	USB 2.0 OnTheGo (OTG) Type A AMBA Subsystem Core (Soft IP / Verilog)	Aurora VLSI, Inc. (www.auroravlsi.com)	Bus Interface > USB > USB OTG	It contains a USB 2.0 Device and Host Controller that connects seamlessly to the AMBA AHB Bus. It is a type A dual mode USB 2.0 Controller and therefore, begins each session as the USB host that then, when requested, will relinquish its host status to become a USB device/hub. When operating as a host, it supports up to eight downstream ports.
8	High Performance Java/ SPARC Bilingual Processor Core (Soft IP / Verilog)	Aurora VLSI, Inc. (www.auroravlsi.com)	General Processor & Microcontroller > Microprocessor	The AU-J1200 Java Bilingual Processor Core is a Java plus 32 bit SPARC processor core targeted at efficient high performance Java execution. It directly executes both Java code and 32 bit SPARC code, thus providing software compatibility for existing applications, as well as fast, efficient Java execution.
9	SDRAM/DDR Controller AMBA Subsystem Core (Soft IP / Verilog)	Aurora VLSI, Inc. (www.auroravlsi.com)	Peripheral Core > Controller > Memory Controller	The AU-MB2200 SDRAM/DDR Controller AMBA Subsystem provides an SDRAM/DDR Controller peripheral subsystem for AMBA based SOCs. It contains an SDRAM/DDR Controller that connects seamlessly to the AMBA AHB Bus as an AMBA Bus slave.

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10	XD Controller AMBA Subsystem Core (Soft IP / Verilog)	Aurora VLSI, Inc. (www.auroravlsi.com)	Peripheral Core > Controller > Peripheral Controller	The AU-MB5000 XD Controller AMBA Subsystem provides an XD Controller peripheral subsystem for AMBA based SOCs. It contains an XD Controller that connects seamlessly to the AMBA AHB Bus as an AMBA Bus slave.
11	Serial Peripheral Interface (SPI) with AMBA Interface Core (Soft IP / Verilog)	Aurora VLSI, Inc. (www.auroravlsi.com)	Peripheral Core > Controller > Peripheral Controller	It supports master (including multi master) and slave SPI modes with SPI word lengths up to 32 bits. Either the most significant bit or least significant bit of each SPI word may be transferred first. All four combinations of SPI clock idle polarity and SPI clock data transfer phase are implemented.
12	General Purpose I/Os (GPIOs) with AMBA APB Interface Core (Soft IP / Verilog)	Aurora VLSI, Inc. (www.auroravlsi.com)	Peripheral Core > Controller > Peripheral Controller	AMBA based SOCs. It contains 32 General Purpose I/Os (GPIOs) that connect seamlessly to the AMBA APB Bus as an AMBA Bus slave. The General Purpose I/Os AMBA APB Core is available as a synthesizable Verilog model.
13	Interrupt Controller with AMBA APB Interface Core (Soft IP / Verilog)	Aurora VLSI, Inc. (www.auroravlsi.com)	Peripheral Core > Controller > Peripheral Controller	The AU-G0100 Interrupt Controller AMBA APB Core provides an interrupt controller peripheral for AMBA based SOCs. It aggregates 32 interrupt requests into 8 interrupt outputs. It connects seamlessly to the AMBA APB Bus as an AMBA Bus slave.
14	Dual-Band Transceiver with 802.11.a and 802.15.4 (Hard IP/ GDSII)	ICU (www.icu.ac.kr)	Analog & Mixed Signal	2.4GHz 의 zigbee와 5 GHz 대역의 WLAN 표준을 동시에 하나의 Tranceiver 로 구현 하였다. 1. RF Front-end- 잡음지수 : 12.5 dB / 전압이득 : 14 dB / 입력 3차 intercept point (IIP3) : -12 dBm 2. 수신기 Baseband- 이득제어 : 0~40 dB / Cutoff : 13 MHz 3. VCO core frequency : 3.4~3.6 GHz / VCO Gain : 160 MHz/V / Image suppression : 28 dBc
15	JPEG Encoder(Soft IP / VHDL, Verilog)	Chonnam National University (www.chonnam.ac.kr)	Video / Image / Audio > Image Coder/Decoder > JPEG	JPEG encoder converts YCbCr video signal into the JPEG file stream of byte level in realtime. The encoder compresses sequential DCT-based mode. IP can be verified by connecting the board that has the JPEG file on their NAND Flash Memory.
16	AES Algorithm for Wireless LAN 802.11 (Soft IP / VHDL)	Chonbuk National University (www.chonbuk.ac.kr)	Wireless Communication > 802.11	This IP is AES algorithm for Wireless LAN. it is tested by FPGA board level test.
17	DI2CMS - I2C Bus Interface - Master/Slave (Soft IP, Firm IP / VHDL, Verilog, EDIF)	Digital Core Design (www.dcd.pl)	Bus Interface> 12C (Inter Interg ateed Circuit)	The DI2CMS core provides an interface between a microprocessor / microcontroller and an I2C bus. It can work as a master or slave transmitter/receiver depending on working mode determined by microprocessor/microcontroller. The DI2CMS core incorporates all features required by the latest I2C specification including clock synchronization, arbitration, multi-master systems and High-speed transmission mode.
18	DP80C51 - Pipelined High Performance Microcontroller (Soft IP, Firm IP / VHDL, Verilog, EDIF)	Digital Core Design (www.dcd.pl)	General Processor & Microcontroller	DP80C51 is an ultra high performance, speed optimized soft core of a single-chip 8-bit embedded controller dedicated for operation with fast (typically on-chip) and slow (off-chip) memories. The core has been designed with a special concern for performance to power consumption ratio.