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A Simple ZVZCS Sustain Driver for a Plasma Display Panel

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ABSTRACT

A high efficiency and low cost sustain driver for a plasma display panel (PDP) utilizing a current pumping method is proposed. The main concept of the proposed circuit is using the current source to charge and discharge the panel. As a result, all power switches can achieve zero voltage switching (ZVS) and every auxiliary switch can also achieve zero current switching (ZCS). Since the inductor current can compensate for the discharge current, the current stress of all the power switches can be reduced considerably. Furthermore, it has features such as a simpler structure, less mass, lower cost and lower electromagnetic interference than in previous circuits.

Keywords: Plasma Display Panel, Sustain Driver, Current Pumping Method

1. Introduction

Plasma displays panels (PDPs), invented at the University of Illinois in 1946 by Prof. Bitzer and Prof. Slottow, have been praised for their large screen size, wide viewing angle, long life, high contrast ratio and thinness. Therefore, it is obvious that PDPs are the best candidate for high-definition televisions (HDTVs) with high resolution. Fig. 1 shows the simplified structure of a PDP with three electrodes. It consists of two glass plates filled with chemically stable rare gases, helium (He) or xenon (Xe) and it is comprised of transparent X and Y sustain electrodes covered with a dielectric layer on the face plate and address electrodes perpendicular to the sustain electrodes on the back plate. A desired color can be realized by exciting the phosphors on the addressing electrode to emit visible light with the ultraviolet photons generated by the gas discharge [1].

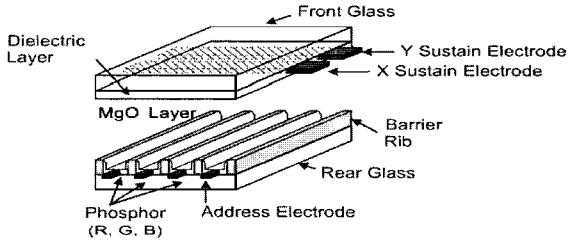

Fig. 1 Simplified structure of PDP with three electrodes

Generally, PDPs have been driven by the address display separation (ADS) method. The driving operation is divided into three periods: reset, addressing, and sustaining periods, as shown Fig 2. During the reset period a high voltage (usually larger than 340V) is forced between electrode X and electrode Y to initialize all the cells in order to obtain the same conditions for all the cells In the addressing period, wall charges are accumulated in

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the cells which display the image. In the last period, sustaining, the discharges occur in the cells addressed previously and the desired image can be obtained on the panel.

During the sustaining period of Fig. 2, the panel voltage waveform is a rectangular pulse from V_S to $-V_S$ between electrode X and Y. Due to the existence of the dielectric layer, the PDP is purely a capacitive load (C_P) with respect to circuit operation. As a result, during charging and discharging transients, $2C_PVs^2$ of energy is consumed in one cycle where C_P and V_S are the panel capacitance and the power supply voltage, respectively. If the operating frequency is defined by f, then the total consumed energy becomes $2fC_PV_S^2$ [2]. If the operating frequency f and V_S is increased, there will be considerable unusable energy which causes serious problems in driving the PDP. In addition, the surge current for charging and discharging the transient intervals causes electromagnetic interference (EMI) noise. To solve these problems, the sustain driver with an energy-recovery-circuit (ERC) is essential in the sustaining period to display the desired image effectively in the PDP.

Many energy recovery circuits have been proposed [3-9]. Among them, the energy recovery circuit using the LC resonant concept [3-4] features high efficiency and good circuit flexibility to cope with various driving methods. Therefore, a number of leading PDP makers have adopted this type of circuit. In addition, several researchers have investigated various new circuits to improve performance and reduce circuit volumes. However, there are some drawbacks such as low efficiency, bulk size, manufacturing or limitation of high frequency driving.

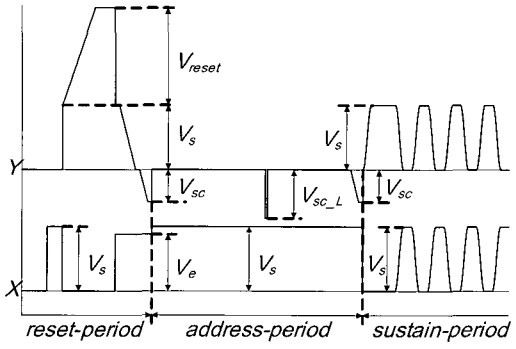


Fig. 2 Voltage waveforms applied to X and Y electrodes in ADS driving method

Therefore, in this paper, a new sustain driver with an energy recover circuit PDP is proposed to solve the drawbacks of the prior circuits with a new driving concept: a current pumping method. The proposed circuit builds up the inductor current before inverting the polarity of the panel. As a result, the main power switches are turned on under a zero voltage condition and the auxiliary switches are turned off under a zero current condition. Furthermore, since the inductor current compensates for the discharging current, the current stress of the main power switches can be considerably reduced. In addition, the proposed sustain driver shows high efficiency and EMI noise resulting from no surge current. Since the transient time can be shortened, PDPs can be driven in high frequencies to obtain high luminance efficiency.

2. PRIOR CIRCUITS

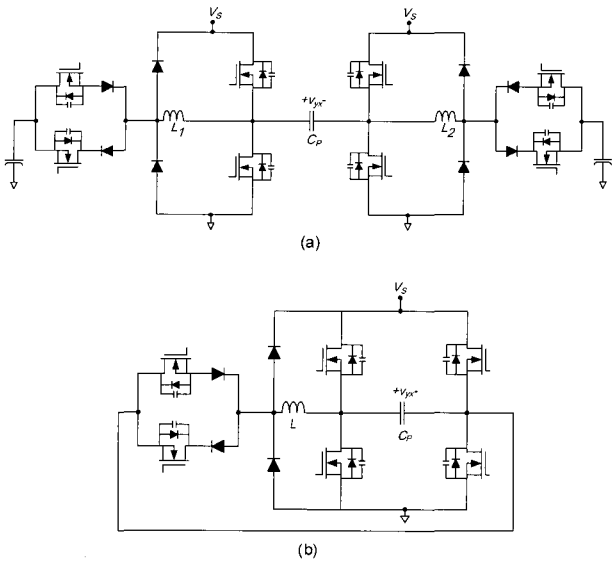


Fig. 3 LC resonant-type PDP driving circuit
(a) Series resonance (b) Parallel resonance

Fig. 3 shows the two representative circuits suggested by Webber and Ohba using series or parallel LC resonance. During charging or discharging the panel, the equivalent circuit of the prior two circuits and panel voltage waveforms of each are shown in Fig. 4. The panel voltages are changed by the LC resonance to the desired voltage level. However, the desired sustain voltage is acquired by hard switching the main inverter switching.

Therefore, a large surge current occurs, as a result of parasitic component effects such as parasitic resistance, on-state resistance of switches, and the forward voltage drop Von as shown in Fig. 4. Considering the parasitic component effects, the equation of panel voltage v_{yx} can be obtained as follows from the equivalent circuit:

Series resonant type

$$v_{yx}=(V_s/2-V_{on})\left[1-e^{-t/\tau}\left(\cos\omega t+(R/\omega L)\sin\omega t\right)\right] \quad (1)$$

Parallel resonant type

$$v_{yx}=-(V_s-V_{on})e^{-t/\tau}\left(\cos\omega t+(R/\omega L)\sin\omega t\right)-V_{on} \quad (2)$$

where $\tau=2L/R$ and $\omega=\sqrt{(1/LC_p)-(R/2L)^2}$. The peak value of two equations can be obtained as follows [10].

Series resonant type

$$V_{yx,pk}=(V_s/2-V_{on})\left(1+e^{(\pi R/2)\sqrt{Cp/L}}\right) \quad (3)$$

Parallel resonant type

$$V_{yx,pk}=(V_s-V_{on})e^{(\pi R/2)\sqrt{Cp/L}}-V_{on} \quad (4)$$

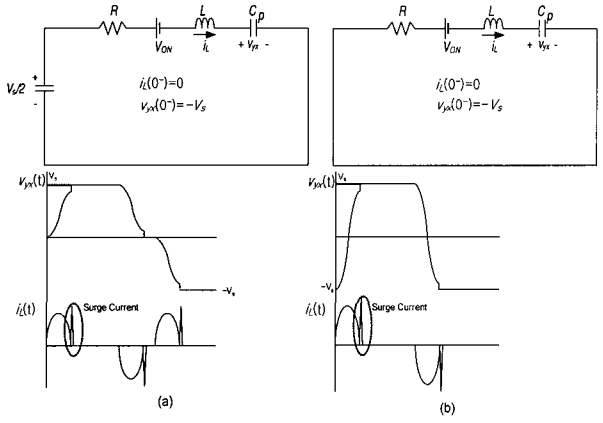


Fig. 4 Equivalent circuit for LC resonant-type PDP driving circuit
(a) Series resonance (b) Parallel resonance

As shown in the above equations, as the parasitic components increase, the peak voltage by LC resonance decreases. This means that an increase in the parasitic resistance or diode forward voltage drop causes a large surge current and reduced recovery efficiency. The parasitic components can be reduced by designing the circuit board optimally and selecting good semiconductor devices. However, since the parasitic effects cannot be removed completely, surge current, EMI and power loss by hard switching are inevitable. In addition, since the transition time, duration of the inversion of panel voltage from $-V_S$ to V_S, is fixed when the inductance is selected, a very small inductance value is needed to obtain a faster transition time. However, this small inductance is hard to implement due to the parasitic components of the circuits. This is a distinct limitation of the conventional LC resonant method.

3. OPERATIONAL PRINCIPLE AND FEATURES OF THE PROPOSED SUSTAIN DRIVER

3.1 Operational Principles of the Proposed Sustain Driver Circuit

Fig. 5 shows the circuit diagram and key waveforms of the proposed sustain driver for the PDP. The proposed sustain driver features a simpler structure, less mass and lower production cost because it has only two auxiliary power switches and two inductors as shown Fig 5 (a) instead of a bulky additional circuit for the ERC. The operation of the proposed sustain driver can be divided into two half cycles, t_0~t_5 and t_5~$t_{0'}$, and mode diagrams are shown in Fig. 6. Because the operation of the two half cycles are symmetric, only the first half cycle is considered.

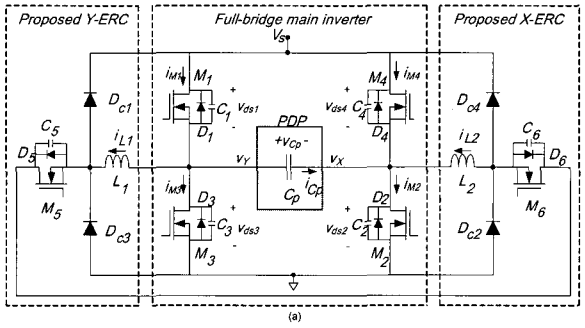
Mode 1($t_0 \le t \le t_1$):Mode 1($t_0 \le t \le t_1$): In this mode, since switches, M_3 and M_4, are turned on and other switches are turned off, the panel voltage, v_{Cp}, is sustained to $-V_S$.

Mode 2($t_1 \le t \le t_2$): When auxiliary switch M_5 is turned on at t_1, mode 2 begins. During t_1 and t_2, both

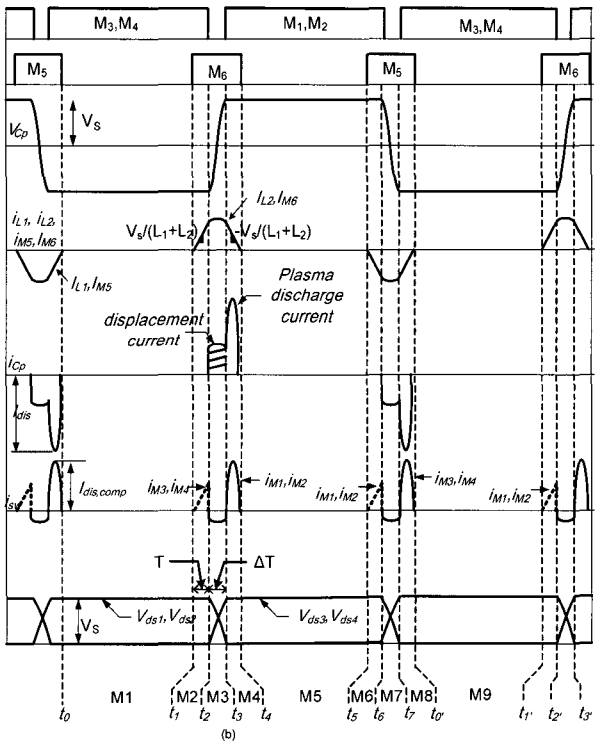
inductor-current, i_{L1} and i_{L2}, are built up linearly with a slope of $V_s / (L_1+L_2)$ through M_3, M_4, M_5 and body diode D_6 of M_6. But the panel voltage is still maintained at $-V_s$. The current is expressed as:

$$i_{L1}(t) = i_{L2}(t) = \frac{V_s}{2L}(t - t_1) \tag{5}$$

During this mode, the energy-recovery inductor can have sufficient energy to make panel voltage, V_x and V_y, go up to sustain voltage $+V_S$ or go down to $-V_S$.



(a) Circuit diagram of the proposed circuit



(b) Key waveforms

Fig. 5 The proposed circuit diagram and its key waveforms

Mode 3($t_2 \le t \le t_3$): When M_3 and M_4 are turned off with M_5 on state, mode 3 begins at t_2. Since the series resonant circuit is formed by $L_1=L_2=L$ and C_P with initial conditions of $v_{ds1}(t_2)=v_{ds2}(t_2)=V_s$, $v_{ds3}(t_2)=v_{ds4}(t_2)=0V$, $v_{Cp}(t_2)=-V_s$ and $i_{L1}(t_2) = i_{L2}(t_2) = (V_s / 2L)\delta T$, panel voltage, v_{Cp}(t), and displacement current C_P , i_{Cp}(t) are given by

$$v_{Cp}(t) = -V_s \cos \omega_c(t - t_2) + \sqrt{\frac{2L}{Cp}}\left(\frac{V_s}{2L}\delta T\right)\sin w_c(t - t_2) \tag{6}$$

$$i_{Cp}(t) = (\frac{V_s}{2L}\delta T)\cos w_c(t - t_2) + \sqrt{\frac{C_p}{2L}}(V_s)\sin w_c(t - t_2) \tag{7}$$

where $\delta T = t_2 - t_1$ and $\omega_c = 1/\sqrt{2LC_p}$. Before t_3, v_{Cp} is clamped to V_S, the output capacitors of switches, M_1 and M_2, are discharged. Therefore, the voltage across M_1 and M_2 falls to zero.

Mode 4($t_3 \le t \le t_4$): When switches, M_1 and M_2, are turned on at t_3 under zero voltage condition, mode 4 begins and t i_{L1} flows to the input source through body diode D_1 of M_1. Additionally, i_{L2} flows through body diode D_2 of M_2 and the inductor current is decreased with a slope of $-V_s / (L_1+L_2)$. The inductor current is given by:

$$i_{L1} = i_{L2} = i_{L2}(t_3) - \frac{V_s}{2L}(t - t_3) \tag{8}$$

This resulted in the canceling of panel discharge currents M_1 and M_2 simultaneously. By compensating the panel discharge current in the main power switches, the current stresses on power switches M_1 and M_2 can be greatly reduced as shown Fig. 5 (b). During this mode, the compensated current of the main inverter switches can be expressed as:

$$i_{M1}(t) = i_{M2}(t) = i_{dis,comp}(t) = i_{dis}(t) - i_{L1}(t) \tag{9}$$

During mode 4, panel voltage V_y is sustained at V_S.

Mode 5($t_4 \le t \le t_5$): When the inductor current is zero, mode 5 begins. This means that the auxiliary switches are turned off under zero current condition t4. However, panel voltage V_y is maintained at V_S as mode 4.

The circuit operation of t_5~t_0' is similar to that of t_0~t_5. Therefore, the operation is repeated. In the circuit diagram, diodes D_{C1}~D_{C4}, are used to clamp the voltage of auxiliary switches to V_S when they are turned off.

As shown in the previous modal analysis, the conduction losses of the main inverter switches can also be reduced significantly and the current stresses of the main inverter switches can be reduced due to the inductor current compensating discharge current. In addition, switches M_1, M_2, M_3 and M_4 are turned on in a zero voltage condition. And auxiliary switches M_5 and M_6 are turned off in a zero current condition. Therefore, high efficiency can be obtained with the simple ERC method because of the canceling discharge current and soft switching of the power switches.

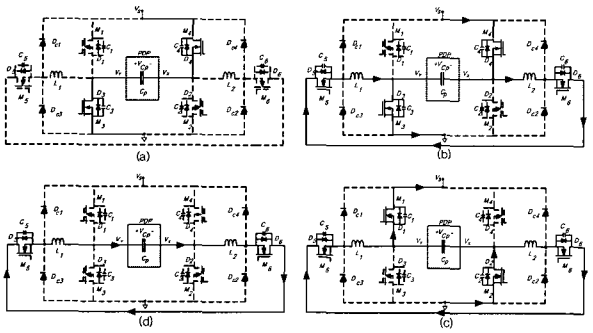


Fig. 6 Operational modes of the proposed sustain driver
(a) Mode 1 (t_0~t_1) (b) Mode 2 (t_1~t_2)
(c) Mode 3 (t_2~t_3) (d) Mode 4 (t_3~t_4)

3.2 Features of the proposed sustain driver

The proposed sustain driver can be applied to drive the industrial and the large screen size PDPs with a fast transition time and high frequency. To obtain these features,

Table 1 Inductance value to obtain desired transition time in the prior circuit and the proposed circuit where Cp=80nF (42-inch PDP)

	Series resonant type	Parallel resonant type	Proposed sustain driver
Transition time ΔT	$2\pi\sqrt{LC_P}$	$\pi\sqrt{LC_P}$	$\sqrt{2LC_P}\left[\sin^{-1}\left(1/\sqrt{(\delta T/\sqrt{2LC_P})^2+1}\right)+\theta\right]$ [1]
Inductor for $\Delta T = 600ns$	$0.227\mu H$	$0.455\mu H$	$1\ \mu H$ when built-time, $\delta T = 200ns$
Inductor for $\Delta T = 500ns$	$0.158\mu H$	$0.306\mu H$	$1\ \mu H$ when built-time, $\delta T = 300ns$
Inductor for $\Delta T = 400ns$	$0.100\mu H$	$0.200\mu H$	$0.7\ \mu H$ when built-time, $\delta T = 300ns$

[1] refer to next section IV

it is very important to select the appropriate inductance value for the energy recovery operation. In section Ⅱ, two prior circuits using resonance between panel capacitance Cp, and resonant inductor L, are studied. As shown in Table 1, if the two prior circuits are applied to a 42-inch PDP (Cp=80nF), the series resonant type circuit [3] needs two inductors with an inductance of 0.227uH. The parallel resonant type [4] needs an inductor with a value of 0.445uH to obtain the transition time of ΔT=600ns. If the board has a parasitic inductor, the two prior circuits cannot achieve the desired fast transition time. Therefore, the faster the transition time is, the harder it is to design an inductor, as shown in Table 1. However, the proposed sustain driver with two inductors of value 1uH can be applied to a 42-inch PDP and can obtain a sufficient transition time. In other words, it is insensitive to the effects of the parasitic components.

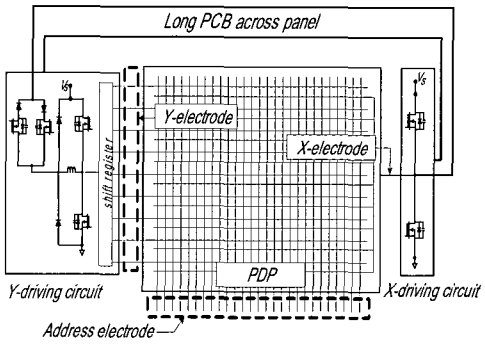


Fig. 7 Long PCB across panel to apply the parallel resonant type in industrial PDP

The parallel resonant type needs a long wire across the panel for the sustain driver of a PDP, as shown in Fig.7. This means that it is hard to obtain normal operation due to the parasitic inductor on the long wire. Therefore, it is hard to use the parallel resonant type for industrial PDPs. Although the proposed driver seems to be similar to the parallel resonant type, it can be applied to industrial PDPs. The improved sustain driver can be obtained without additional circuits as shown in Fig. 8. By replacing auxiliary switches with two inductors, the inductors can absorb the parasitic inductance with the same operation of the proposed sustain driver.

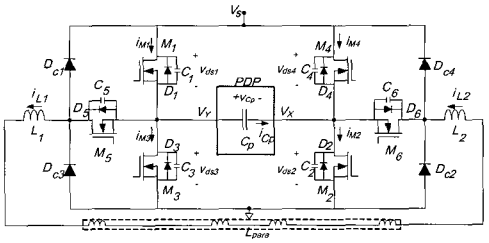


Fig. 8 Circuit diagram of the improved sustain driver to overcome problem of the parasitic inductor on wire across panel

4. DESIGN CONSIDERATION

4.1 Relationship of Transition Time ΔT, Inductor L, and built-up time δT

It is assumed that parasitic components, such as resistor, inductor, etc are neglected because normal operation is not affected by parasitic components. Transition time ΔT is defined as the time duration during which the panel voltage is changed from V_S to $-V_S$. By replacing t-t_1 to ΔT and $V_{Cp}(t)$ to V_S, the equation (6) becomes:

$$V_s = -V_s \cos w_c(\Delta T) + \sqrt{\frac{2L}{C_p}}\left(\frac{V_s}{2L}\delta T\right)\sin w_c(\Delta T) \tag{10}$$

By solving this equation, ΔT can be obtained when δT is defined as the time duration in which the inductor current is built up before the inversion of the panel polarity. As a result, transition time ΔT can be given by

$$\Delta T = \sqrt{2LCp}\left[\sin^{-1}\left(1/\sqrt{(\delta T/\sqrt{2LCp})^2+1}\right)+\theta\right] \tag{11}$$

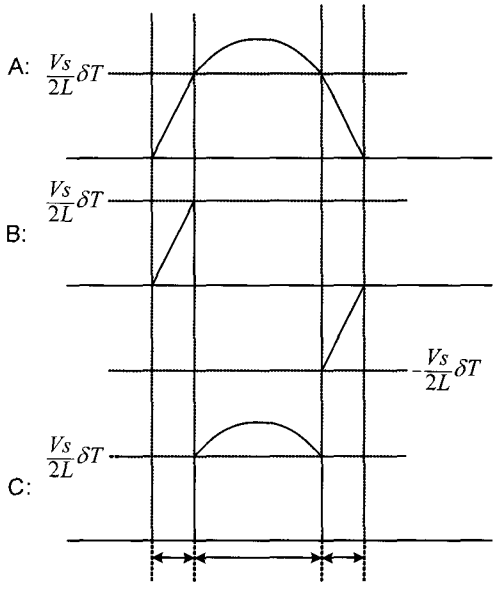
where $\theta = \tan^{-1}(\sqrt{2LC_p}/\delta T)$. Transition time, ΔT, is decreased as the current build-up time, δT, is longer with a fixed value of $L_1 = L_2 = L$. This means that another design factor is considered in designing inductor L. This means that if a faster transient time with a fixed inductance is required the inductor current should be built up more before transition.

4.2 Power Losses according to Built-up time δT and Inductance of L

Until now, many sustain drivers for PDPs have been proposed, but have not been applied to PDP products, because power consumption is an important application factor. In this section, the power loss equation of the proposed circuit is shown to predict power consumption and considers power loss according to the design parameters of previous section. By considering the mode analysis in Fig. 8, the power consumption in the main inverter switch and auxiliary switches can be obtained in one switching period T as follows:

$$P_{sus-sw} = \frac{4}{T}\left[\int_0^{\delta T}\left(\frac{V_s}{2L}t\right)^2 R_{ds-sus}dt + \int_0^{\delta T}\left(\frac{V_s}{2L}t\right)V_{on-body}dt\right] \tag{12}$$

$$P_{ER-sw} = \frac{2}{T}\left[\int_0^{\delta T}\left(\frac{V_S}{2L}t\right)^2 R_{ds-on}dt\right] + \frac{2}{T}\left[\int_0^{\delta T}\left(\frac{V_S}{2L}t\right)V_{on-body}dt\right] \tag{13}$$
$$+\frac{2}{T}\left[\int_{\delta T}^{\delta T+\Delta T}\left(\frac{V_S}{2L}\delta T\cos(t-\delta T)-\sqrt{\frac{C_P}{2L}}V_S\sin(t-\delta T)\right)^2 R_{ds-on}dt\right]$$
$$+\frac{2}{T}\left[\int_{\delta T}^{\delta T+\Delta T}\left(\frac{V_S}{2L}\delta T\cos(t-\delta T)-\sqrt{\frac{C_P}{2L}}V_S\sin(t-\delta T)\right)V_{on-body}dt\right]$$



A: Current waveforms of auxliary switches for ERC
B: Current waveforms of main inverter switches
C: Current waveforms of panel capacitor

Fig. 9 Current waveforms of the main inverter switches and auxiliary switches

where R_{ds-sus} and R_{ds-er} are the on-resistance of the main inverter switches and auxiliary switch and $V_{on-body}$ is the forward voltage drop in the body diode of the auxiliary and main switches. This is not considered a power loss of

the clamping diode. This power loss is considered as a conduction loss of the inductor current because a large amount of surge current of the main inverter switches must be removed by adapting the proposed sustain driver using the current-pumping method. By using (12) and (13), the power loss according to variations of the built-up time and inductor value can be calculated with parameters used in the prototype PDP driver, as shown in Fig. 9. The transition time is decreased as the current build-up time, δT, is increased with a fixed inductance value, but the conduction losses are increased. Thus, the value of the build-up time, δT, can be carefully selected to obtain a desirable transition time and high efficiency.

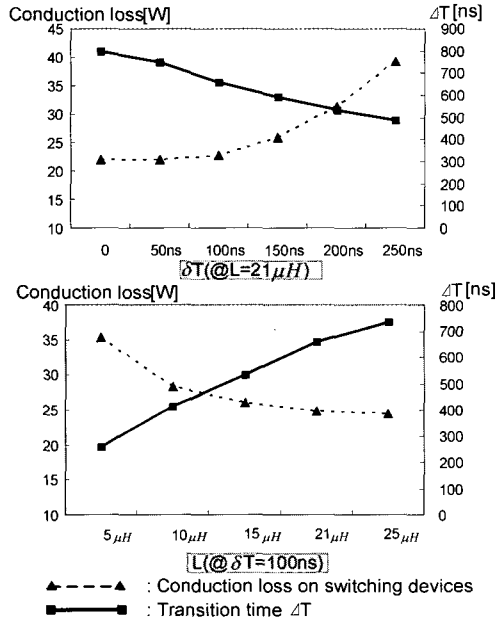


Fig. 10 Calculated conduction loss under δT and L variations without discharging current

5. EXPERIMENTAL RESULTS

A prototype sustain driver for a PDP is implemented with specifications as follows:, $L_1 = L_2 = 21\mu H$, C_p=2nF (6 inch panel), M_1-M_6=2SK2995, clamp diodes=S20LC30, gate driver IC=IR2110, switching frequency=50KHz, transition time $\Delta T \leq 800ns$, and V_S =141V. Fig. 11 shows the experimental results of the proposed circuit. Panel voltages V_x and V_y are charged and discharged from V_S to 0V and from 0 to V_S respectively, without voltage notches. In Fig.11 (a), during the built-up interval, v_{Cp} is sustained and the auxiliary switch current (inductor current) increases linearly. After reversing the polarity of the panel, they are recovered. Fig.11 (b) shows the output capacitors of the switches are discharged fully when the power switches are turned on. This means that all main inverter switches are turned on in a zero voltage condition. In addition, the auxiliary switches are turned off in a zero current condition. As it can be shown in experimental waveforms, the proposed circuit employed a current pumping method which has the advantages of full charging and discharging of the panel. Therefore, it enables soft-switching of the power switches. Furthermore it requires fewer devices and the structure of the circuit is simpler than those of the prior circuits.

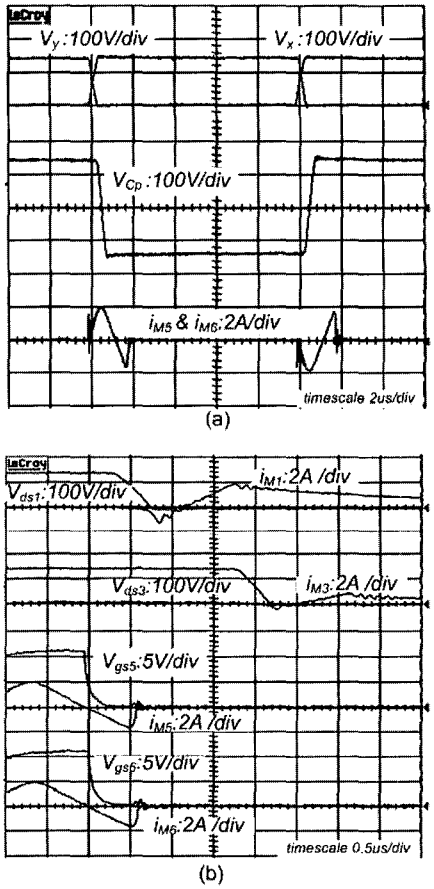


Fig. 11 Experimental waveforms of the proposed sustain driver
(a)Voltage Waveforms of X,Y node, V_{Cp} and current waveforms of i_{M5} and i_{M6}
(b)Turn on transient waveforms of M_1 and M_3 and turn off transient waveforms of M_5 and M_6

6. Conclusion

A new current-pumping PDP sustain driver circuit has been proposed to overcome the drawbacks of the prior circuits. This circuit features a simpler structure and lower production cost. Moreover, the main power switches are turned on under a zero voltage condition and the auxiliary switches are turned off under a zero current condition. Therefore, it demonstrates higher efficiency and lower EMI noise. Furthermore, since the panel discharge current is compensated, it shows a low current stress and low conduction loss. In addition, it enables light for the panel without having to consider parasitic component effects. Lastly, the proposed sustain driver can be designed easily without consideration of the parasitic components and can promise fast transient time ΔT according to the values designed. Therefore, the proposed circuit is expected to be very suitable for energy recovery circuits for high-definition PDP TVs.

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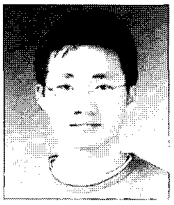

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