논문 2006-43SD-9-2

PHS 어플리케이션에서의 빠른 스위칭 주파수 합성기를 위한 효율적인 Coarse Tuning 방법

(An Efficient Coarse Tuning Scheme for Fast Switching Frequency Synthesizer in PHS Applications)

박 도 진*, 정 성 규*, 김 진 경*, 부 영 건*, 정 지 훈*, 이 강 윤**

(Do Jin Park, Sung Kyu Jung, Jin Kyung Kim, Young Gun Pu, Ji Hoon Jung, and Kang-Yoon Lee)

요 약

본 논문에서는 PHS 어플리케이션에서 새로운 Coarse Tuning 기법을 사용한 빠른 스위칭의 CMOS 주파수 합성기를 기술하였다. 제안한 Coarse Tuning 방법은 Phase Noise와 Lock-Time을 최적화하기 위해 LC-VCO의 적절한 Tuning Capacitances를 선택하는 것이다. 이를 바탕으로 측정된 Lock-Time은 약 20μs 이고, Phase Noise는 600kHz의 offset에서 -121dBc/Hz 이다. 칩은 0.25μm CMOS 공정으로 제작하였고, 면적은 0.7mm x 2.1mm 이다. 소비전력은 2.7V 공급 전압 하에서 54mW 이다.

Abstract

This paper presents a fast switching CMOS frequency synthesizer with a new coarse tuning scheme for PHS applications. The proposed coarse tuning method selects the optimal tuning capacitances of the LC-VCO to optimize the phase noise and the lock-time. The measured lock-time is about 20μs and the phase noise is -121dBc/Hz at 600kHz offset. This chip is fabricated with 0.25μm CMOS technology, and the die area is 0.7mm x 2.1mm. The power consumption is 54mW at 2.7V supply voltage.

Keywords : Coarse Tuning, Frequency Synthesizer, Phase Noise, Lock time, Weighted Capacitance

Ⅰ. 서 론

A frequency synthesizer has stringent performance requirements of low phase noise, fast switching time, and low spurious tone. To meet the channel switching time of 30μs in PHS, the efficient coarse tuning method are proposed in this paper.

* 학생회원, ** 정회원, 건국대학교 전자공학부
(Konkuk University)
(Konkuk University)
※ 본 연구는 IT SoC 핵심설계인력양성 사업과 학술진흥재단의 지원에 의하여 수행되었고, IDEC을 통해 Chip 제작을 지원받았음.
접수일자: 2006년7월1일, 수정완료일: 2006년8월18일

Ⅱ. 본 론

1. Frequency Synthesizer Architecture

Fig. 1 shows the block diagram of the proposed frequency synthesizer. The proposed frequency synthesizer is composed of a reference clock doubler (RCD), phase frequency detector (PFD), charge pump (CP) with current mismatch compensation circuit, voltage controlled oscillator (VCO), prescaler, and modulator. The frequency of the REF_CLK is 19.2MHz. Reference Clock Doubler (RCD) generates the 38.4MHz clock by doubling the REF_CLK to reduce the quantization noise of the modulator[2].

The coarse tuning controller sets the optimum

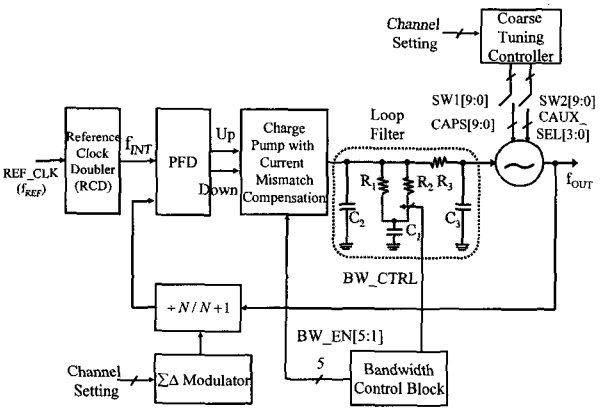


그림 1. 제안한 주파수 합성기의 구조
Fig. 1. Block diagram of the proposed frequency synthesizer.

coarse tuning capacitance for VCO. Because there is no time for coarse tuning at every channel switching and the overall frequency range of PHS cannot be covered by one VCO curve, a new coarse tuning method using auxiliary capacitor arrays, CAUX_SEL[3:0], is proposed.

2. Proposed Coarse Tuning Method

The LC-type VCO is used to meet the phase noise specification. The LC-type VCO shown in Fig. 2 is composed of a fixed capacitance, coarse tuning capacitances, auxiliary capacitances, and variable capacitance (varactor). Switches, SW_CAPS[9:0], are inserted between the CAPS[9:0] from coarse tuning and those to VCO to reduce the spur after coarse tuning process. The coarse tuning controller determines the optimal coarse tuning capacitances, CAPS[9:0]. To cover the overall PHS frequency band of 50MHz, the VCO gain should be greater than 50MHz/V. However, if the VCO gain is too large, the phase noise specification cannot be satisfied, so the frequency band cannot be covered by one VCO curve. To cover the overall frequency range with small VCO gain, many numbers of VCO curves are implemented using the capacitor arrays[4][5].

The frequency range that can be covered by CAUX_SEL[3:0] is 36MHz. CAUX_SEL[0] and CAUX_SEL[2] cover the frequency range of 6MHz, and CAUX_SEL[1] and CAUX_SEL[3] cover the frequency range of 12MHz.

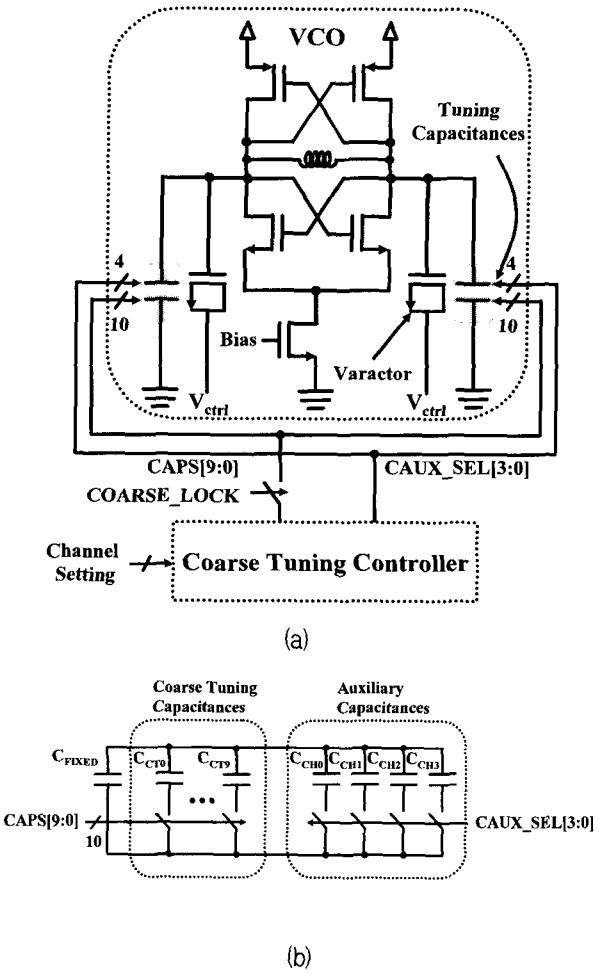


그림 2. (a) voltage controlled oscillator 의 구조
(b) VCO의 튜닝 캐패시턴스
Fig. 2. (a) Block diagram of voltage controlled oscillator
(b) Tuning capacitances of VCO.

To optimally select the VCO curve, the new coarse tuning method is proposed. Unfortunately, there is no time for coarse tuning in every channel switching in PHS protocol. Only fine tuning is possible at every channel switching, so auxiliary capacitances, CAUX_SEL[3:0], are used for the fast channel switching in the proposed coarse tuning method. Coarse tuning is done for the center frequency (1902MHz). Based on the target switching frequency, the auxiliary capacitances, CAUX_SEL[3:0], are adjusted as shown in Fig. 3. After the main coarse tuning, the CAPS[9:0] is determined, and these values are valid until next power up.

When the auxiliary coarse tuning is done at every channel switching, CAUX_SEL[3:0] is selected statically based on the target frequency. The basic

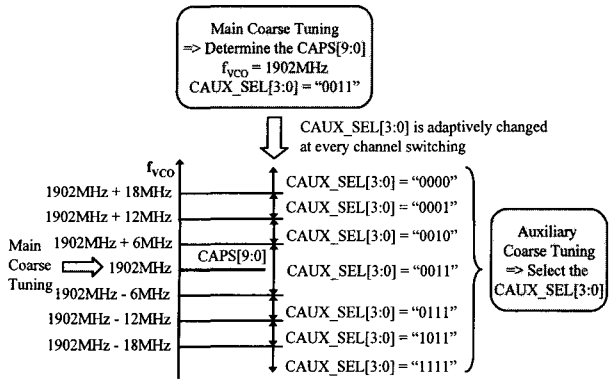


그림 3. 주 coarse tuning과 보조 coarse tuning 간의 관계

Fig. 3. Relationship between main coarse tuning and auxiliary coarse tuning.

algorithm is shown in Fig. 3. The optimum VCO curve can be selected with this auxiliary coarse tuning without extra main coarse tuning. As the coarse tuning time is shorter, the average power consumption can be reduced. The new coarse tuning method that can reduce the coarse tuning time is proposed.

Fig. 4(a) shows the block diagram of the proposed coarse tuning method and Fig. 4(b) shows the timing diagram of the proposed coarse tuning process.

When the frequency synthesizer receives the channel information, the coarse tuning controller converts the channel information to the appropriate timing parameter for the coarse tuning. The coarse tuning controller works with 19.2MHz reference clock signal to generate RST_CNT, EN_CNT, DES_CLK, and COMP_CLK signals. Since the coarse tuning process is a kind of frequency tracking, the digital accumulator is used to estimate the period of the VCO. This result is compared with the channel reference number, CH_REF_NUM[N-1:0], generated from Channel Reference Number Generator based on the Channel Setting. In the timing diagram shown in Fig. 4(b), the digital accumulator or the counter are periodically reset by the RST_CNT signal generated by the En_Counter Generator block. This counting operation is masked by the EN_CNT signal. Only when the EN_CNT is high, the operation of the counter is enabled. When the output of the counter is larger than the channel reference number, the DOWN

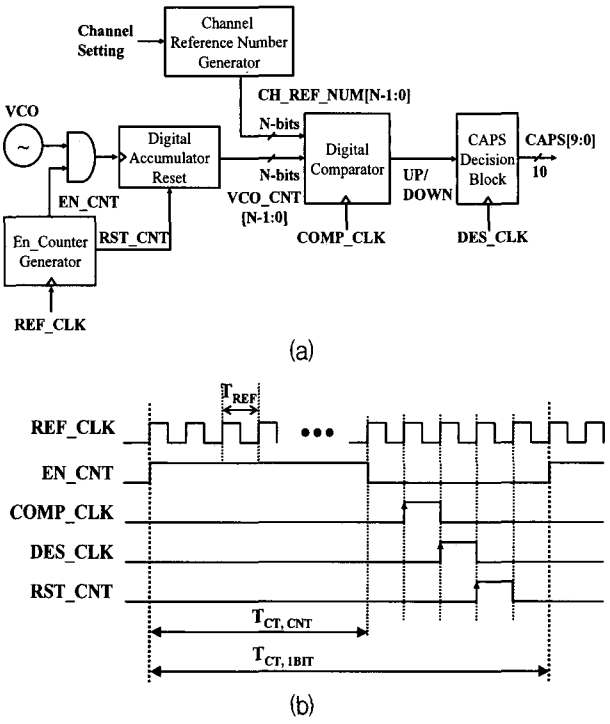


그림 4. (a) 제안한 coarse tuning 기법의 구조
(b) 제안한 coarse tuning 기법의 타이밍도

Fig. 4. (a) Block diagram (b) Timing diagram of the proposed coarse tuning method.

signal is asserted at the rising edge of COMP_CLK to make the frequency of the VCO lower. When the output of the counter is smaller than the channel reference number, the UP signal is asserted at the rising edge of COMP_CLK to make the frequency of the VCO higher. The UP/DOWN signals will be used to decide the CAPS[i] which is the polarity of the switch connected to the i-th capacitor in the VCO.

The accuracy of the coarse tuning process is mainly determined by the EN_CNT signal. In Fig. 4(b), the TCT, 1BIT means the total cycle time for the switch on and off of the one bit in the coarse tuning, which is mainly determined by operating time of the counter, TC, CNT. The way to improve the accuracy is to increase the reference number or the duration of the EN_CNT. However, the penalty for the improvement in coarse tuning is the increase of the comparison time or the time required for the coarse tuning. If the number of bits that should be determined is 10 bits, then the time required to finish the coarse tuning will be 10 times for the 1bit decision case. Thus, as the number of the bits or the

accuracy for the coarse tuning is increased, it results in the increase of the coarse tuning time.

After finishing the coarse tuning, the frequency synthesizer enters into the phase lock operation. Since the total lock time of the frequency synthesizer includes the time required for the coarse tuning, the accurate coarse tuning works as a disadvantage for the lock time. The coarse tuning should be done very fast both for good phase noise performance and small lock time.

The proposed coarse tuning method discloses the way to reduce the total bit-comparison time of the coarse tuning period. In the proposed coarse tuning method, the trade-off between the coarse tuning time and the accuracy of the coarse tuning is resolved by adopting weighted comparison time for the coarse tuning of the each bit decision. The bit-comparison time for each coarse tuning bit is set differently according to its comparison resolution.

Fig. 5(a) shows the simplified timing diagram of the coarse tuning process in the conventional method [4]. Since the final resolution of the coarse tuning should be made to be small enough, the coarse tuning time for each bit is set to large enough to cover all of the variation in decision process. Those variations might come from the uncertainty of the digital accumulator, the other logic delay, the noise like the power supply noise, and the start-up time of each component. When the number of the coarse tuning bits increases, the total time required for the coarse tuning increases linearly.

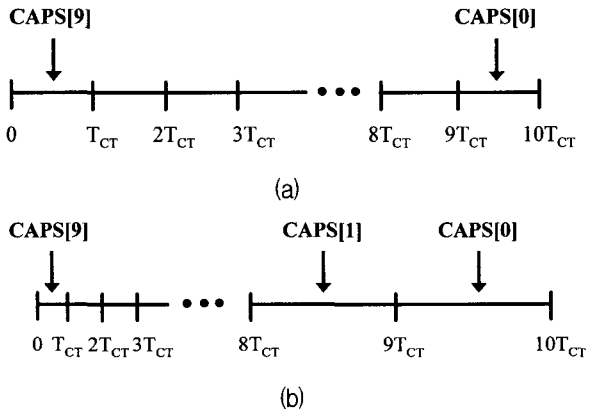


그림 5. (a) 기존 coarse tuning 기법의 타이밍
(b) 제안한 coarse tuning 기법의 타이밍
Fig. 5. Timing of (a) the conventional coarse tuning method (b) the proposed coarse tuning method.

Fig. 5(b) shows the simplified timing diagram of the proposed coarse tuning process. Unlike the conventional method in Fig. 5(a), the decision for each bit is set differently. The last bit has the longest decision time, meanwhile the first bit has the shortest decision time. The duration of each bit can be optimized according to the specific implementation of the coarse tuning algorithm. The main purpose of the weighting on the decision time is to provide an accurate coarse tuning result, while also guaranteeing the short coarse tuning time.

The unequal time regulation for the coarse tuning in this proposed method is guaranteed by the design incorporating redundant weighting in the discrete capacitor arrays for the coarse tuning. Table 1 shows the implementation of the capacitor array for the coarse tuning. CAP[i] corresponds to the i-th capacitor used to tune the frequency of the VCO and the CAP[0] is the last capacitor to be selected through the coarse tuning process.

In Table 1, only relative weighting factors for capacitance value are shown. Since the frequency of the LC VCO is determined by the equation of $1/2\pi\sqrt{LC}$, the relative weighting of the capacitance is sufficient to indicate the variation of the frequency. The redundancy R[i] in Table 1 is obtained by Eq. 3.

표 1. coarse tuning 처리를 위한 가중 캐패시턴스
Table 1. Weighted capacitance for the coarse tuning process.

Capacitor CAPS[N]	Weighting W[N]	Redundancy Amount R[N]
CAPS[0]	1	0
CAPS[1]	2	0
CAPS[2]	3	0
CAPS[3]	4	2
CAPS[4]	6	4
CAPS[5]	10	6
CAPS[6]	16	10
CAPS[7]	32	10
CAPS[8]	64	10
CAPS[9]	128	10

W[i] is the weighting factor for CAPS[i] in Eq. 3.

$$R[i]=W[i]-\sum_{i=0}^{i-1}W[i] \quad (1\le i\le 9) \tag{3}$$

Since the capacitance value has correspondence with the frequency, the above equation indicates that the redundancy can be used to compensate the error in the decision process. In an ideal situation, if the decision process is perfect and the redundancy is all set to zero, then the result of the coarse tuning will also be ideal and the resulting accuracy will be determined by the smallest weighting factor. However, in practical implementation of the capacitor array, there is some mismatch between two binary-weighted capacitors. If there is no redundancy for the lower bits, this mismatch at certain stages cannot be restored. Since the amount of the mismatch is proportional to the weighting factor, the frequency error caused by the mismatch will be less severe for the cases with smaller weighting factor. Thus, the redundancy is given to the high index value rather than the low index as described in Table 1.

Although those redundancies in an array of capacitors are made intentionally to compensate fabrication mismatch of the capacitor array, this property can be used to reduce the coarse tuning time effectively. Even though some uncertainty or error happens to exist in the decision process of the coarse tuning, those errors or uncertainties will be corrected if amount of the error is smaller than the redundancy amount at that specific index.

Therefore, the duration of the coarse tuning can be reduced in the case where there is large redundancy. Since the extension of the duration of comparison time in Fig. 5(b) can reduce the effect from the decision process, the most accurate decision or the longest comparison time should be made when the redundancy is zero. In Table 1, the coarse tuning controller should have the most accurate decision when it decides the switching polarity of CAPS[2:0]. The comparison for other bits can be relaxed and thus a smaller comparison time will be allowed.

As stated before, when the comparison time is doubled, the accuracy of the coarse tuning process is doubled. Assuming that Tmin is the minimum 1-bit comparison time required for CAPS[0], the comparison time for CAPS[4] can have the value of Tmin/2 to give correct coarse tuning result. The comparison time of Tmin/10 for CAPS[9] will have same probability of error with that of Tmin for CAPS[0]. When the same comparison cycle time is applied for the coarse tuning, the total time for the coarse tuning will be 10*Tmin. However, when the adaptive optimization for the comparison time is made, the total coarse tuning time will be calculated as shown in Eq. 4.

$$\frac{T_{min}}{10}\times 4+\frac{T_{min}}{6}+\frac{T_{min}}{4}+\frac{T_{min}}{2}+T_{min}\times 3=\frac{259}{60}T_{min} \tag{4}$$

The total coarse tuning is reduced by more than two times with the same accuracy in the proposed coarse tuning method. The accurate coarse tuning can be done by adopting the unequal time interval for the comparison time as done in the proposed coarse tuning method. This accurate coarse tuning enables the smaller size of the analog varactor for better phase noise performance.

III. 실 험

This chip is fabricated in CMOS process with a feature size of 0.25μm technology, a single poly layer, five layers of metal, and options of metal-insulator-metal (MIM) capacitors, and high sheet resistance poly resistors. The die area of the frequency synthesizer is 0.7mm x 2.1mm. The area is about one-third of the reference[1], which is 2.29mm x 2.32mm. Because it is implemented in CMOS technology, it has merits in the area over the reference[1], which is implemented in BiCMOS technology.

Fig. 6 shows the measured lock-time. It is about 18μs when the target frequency is switched from 1884.65MHz to 1915.68MHz.

The frequency span is 8kHz and the frequency resolution is 1kHz/div in Fig. 6. The frequency step

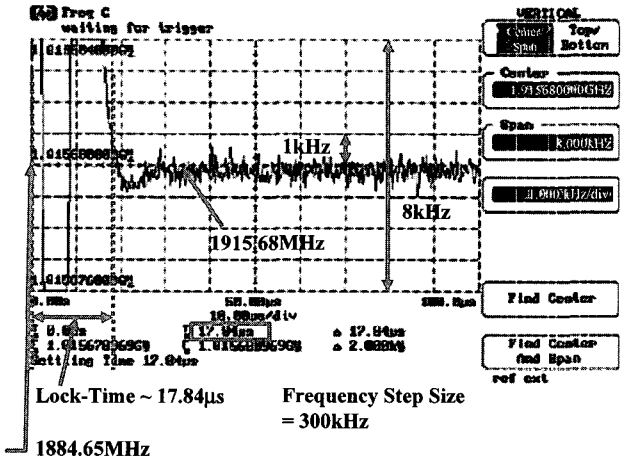


그림 6. 측정된 lock-time
Fig. 6. Measured lock-time.

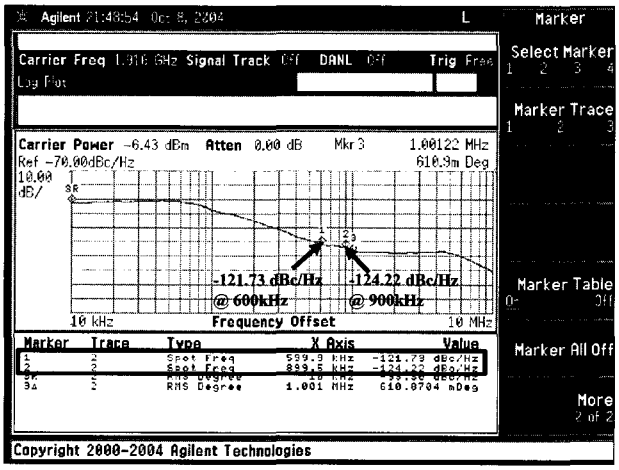


그림 7. 측정된 phase noise
Fig. 7. Measured phase noise.

표 2. 측정된 성능 요약
Table 2. Summary of measured performance.

Supply Voltage	2.7V
Power Consumption	53mW
Lock Time	< 20μs
Phase Noise	-121.73 dBc/Hz @ 600kHz
Die area	0.7mm x 2.1mm

size is designed as 300kHz to support the channel spacing of 300kHz. The lock-time is measured by the time within which time the output frequency of the frequency synthesizer settles into the range of 1kHz of the target frequency.

Fig. 7 shows the measured phase noise. The phase noise is -121dBc/Hz and -124dBc/Hz at 600kHz and 900kHz offset, respectively. The power consumed only in the frequency synthesizer is 54mW at 2.7V supply voltage.

Table 2 is the summary of measured performance and comparison results with references [1] and [6].

IV. 결 론

The proposed coarse tuning method for a fast switching frequency synthesizer selects the optimal tuning capacitances of the LC-VCO to optimize the phase noise and the lock-time. The measured lock-time is about 20μs and the phase noise is -121dBc/Hz at 600kHz offset. This chip is fabricated with 0.25μm CMOS technology, and the die area is 0.7mm x 2.1mm. The power consumption is 54mW at 2.7V supply voltage.

참 고 문 헌

[1] Mike Keaveney, Patrick Walsh, Mike Tuthill, Colin Lyden, Bill Hunt, "A 10us Fast Switching PLL Synthesizer for a GSM/EDGE Base-Station," 2004 IEEE International Solid-State Circuits Conference, pp. 192-193, Feb. 2004.

[2] Hyungki Huh, Yido Koo, Kang-Yoon Lee, Yeonkyeong Ok, Sungho Lee, Daehyun Kwon, Jeongwoo Lee, Joonbae Park, Kyeongho Lee, Deong-Kyoon Jeong, Wonchan Kim, "A CMOS Dual-Band Fractional-N Synthesizer with Reference Doubler and Compensated Charge Pump," 2004 IEEE International Solid-State Circuits Conference, pp. 100-101, Feb. 2004.

[3] Hisayasu Sato, Kenichi Kashiwagi, Kazuhito Niwano, Tetsuya Iga, Tatsuhiko Ikeda, Koichiro Mashiko, Tadashi Sumi, and Koji Tsuchihashi, "A 1.9-GHz Single Chip IF Transceiver for Digital Cordless Phones," IEEE J. Solid-State Circuits, vol. 31, no. 12, pp. 1974-1980, December 1996.

[4] Yido Koo, Hyungki Huh, Yongsik Cho, Jeongwoo Lee, Joonbae Park, Kyeongho Lee, Deog-Kyoon Jeong, and Wonchan Kim, "A fully integrated CMOS Frequency Synthesizer with charge-averaging charge pump and dual-path loop filter for PCS and Cellular-CDMA wireless systems," IEEE J. Solid-State Circuits, vol. 37, no. 5, pp. 536-542, May 2002.

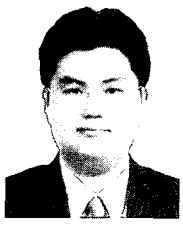
[5] J. Craninckx and M. Steyaert, "A fully integrated CMOS DCS-1800 frequency

synthesizer," IEEE J. Solid-State Circuits, vol. 33, no. 12, pp. 2054 - 2065, Dec. 1998.
[6] Mohamed A. I. Mostafa, Chee K. Quck, Abdellatif El Moznine, William Roberts, Matt Romney, David Walker, Dave Stegmeir, Kien Tran, Nathaniel King, Shayan Farahvash, and Robert Koupal, "A 1.9GHz SiGe BiCMOS PHS Transceiver with an Integrated PA and a Fast Settling PLL," 2005 IEEE Radio Frequency Integrated Circuits Symposium, pp. 277-280, June 2005.

저 자 소 개

박 도 진(학생회원)
2006년 건국대학교 전자공학부 학사 졸업.
2006년~현재 건국대학교 전자정보통신 공학과 석사과정
<주관심분야 : RF/아날로그 집적회로설계>

김 진 경(학생회원)
2006년 건국대학교 전자공학부 학사 졸업.
2006년~현재 건국대학교 전자정보통신 공학과 석사과정
<주관심분야 : RF/아날로그 집적회로설계>



정 지 훈(학생회원)
2006년 건국대학교 전자공학부 학사 졸업.
2006년~현재 건국대학교 전자정보통신 공학과 석사과정
<주관심분야 : RF/아날로그 집적회로설계>

정 성 규(학생회원)
2006년 건국대학교 전자공학부 학사 졸업.
2006년~현재 건국대학교 전자정보통신 공학과 석사과정
<주관심분야 : RF/아날로그 집적회로설계>

부 영 건(학생회원)
2006년 건국대학교 전자공학부 학사 졸업.
2006년~현재 건국대학교 전자정보통신 공학과 석사과정
<주관심분야 : RF/아날로그 집적회로설계>

이 강 윤(정회원)
2003년 서울대학교 전기공학부 박사 졸업.
2003년~2005년 (주)지씨티리써치 책임연구원.
2005년~현재 건국대학교 전자공학부 조교수.
<주관심분야 : RF/아날로그 집적회로설계, 아날로그/디지털 Mixed Mode 설계>