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SLS Technology for High Performance Poly-Si TFTs and Its Application to Advanced LCD and SOG

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Abstract

SLS crystallization and CMOS LTPS process have been developed for high performance and uniform characteristics. By strictly optimizing SLS optics in conventional 2 shot SLS process, threshold voltage variation of 720 pixel TFTs in 2.2-inch QVGA panel (240xRGB) was remarkably decreased from 1.89 V to 0.56 V of 3sigma value. Mobility of the channel doped NTFT and PTFT for circuits were 146 and 38 cm^2/Vs, respectively. Functional unit circuits for SOG were also fabricated and properly operated.

1. Introduction

Polycrystalline Si (poly-Si) TFT has been widely used as pixel switching- and circuit-device for advanced mobile liquid crystal display (LCD) and system-on-glass (SOG) or system-on-panel (SOP). Higher carrier mobility of poly-Si TFT compared with that of a-Si TFT, makes it possible to integrate external driver ICs, other peripheral circuits, memory and ultimately CPU on the glass[1]. High performance poly-Si TFT is required to enhance circuit integration level and improve the quality of displays. In order to enhance the performances of poly-Si TFT, so many crystallization technologies for high quality poly-Si film have been developed. Among various crystallization technologies, Sequential Lateral Solidification (SLS)[2-4] has attracted many attentions because of its productivity, superior crystalline quality, flexibility for obtaining various microstructure and wide process range. Previous reports demonstrated that SLS crystallization is attractive for high performance TFT[5] and SOG[6], compared with conventional excimer laser annealing (ELA) method. In this article, we report our recent development results of SLS crystallization and SLS-based LTPS technology for advanced LCD

and SOG. We have focused on the mobility enhancement, threshold voltage (Vth) adjustment for CMOS circuit TFT and uniformity improvement for pixel TFTs in display area.

2. SLS crystallization technology

2.1 Process design

An SLS equipment with XeCl pulsed laser is used. Its wavelength is 308 nm, repetition rate is 300 Hz and extended pulse duration time is 240 nsec. Laser beam was patterned by an SLS mask and irradiated onto the substrate with 5x demagnification. An irradiated area on the substrate is 2 mm x 15 mm per shot.

SLS process is conducted at a laser energy density for complete melting of the a-Si film prepared on buffer layer/substrate. Depending on the SLS mask design and process method, various microstructures of poly-Si are obtained as shown in Fig. 1. Material properties of buffer layer[7] and pretreatment for a-Si also affect the final

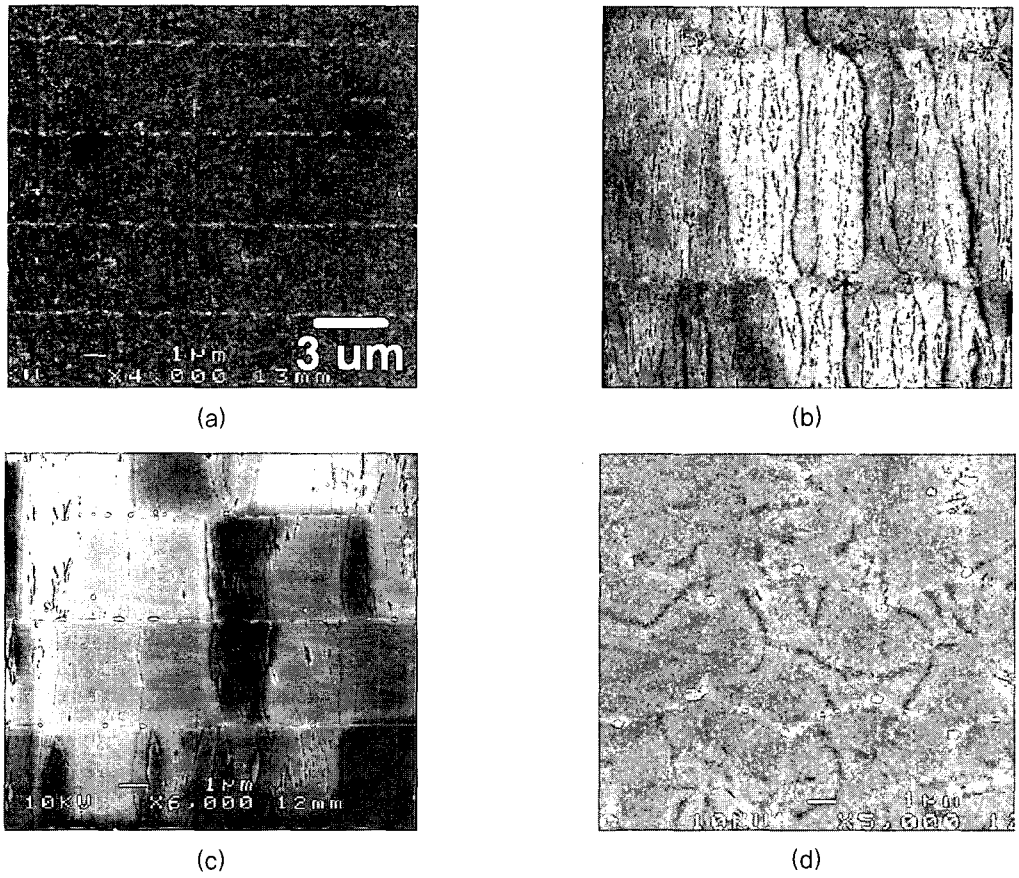


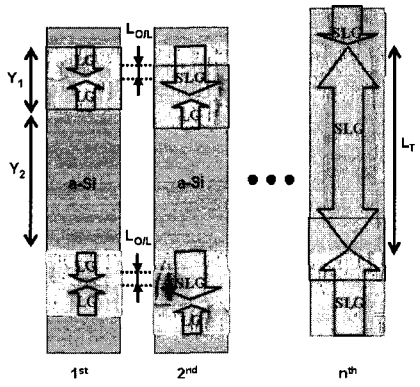
Fig. 1. Microstructures of various types of SLS. (a) 2 shot SLS (b) 4 shot SLS (c) Cross SLS (d) Dot SLS.

microstructure of poly-Si. Among many kinds of SLS methods, n-shot SLS with slit-shape beam arrays [Fig. 1(a) and (b)] is the most practical since it is easily applied to get the high quality poly-Si. In n-shot process, we derived the correlation between SLS mask design parameter and a targeted grain size (L_T) for a given architecture of SOG display[8] with the relation as follows;

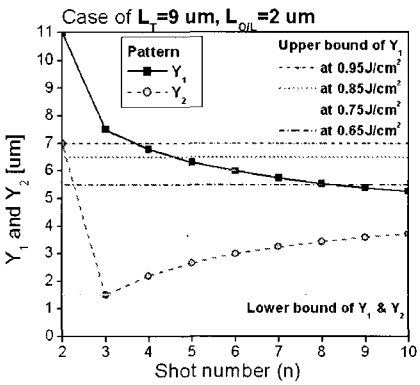
For n = 2,

$$Y_1 = L_T + L_{O/L} \quad (1)$$

$$Y_2 = L_T - L_{O/L} \quad (2)$$



(a)



(b)

Fig. 2. n-shot SLS. (a) Evolution of microstruc-ture (b) Diagram for correlation among parameters.

For n ≥ 3,

$$Y_1 = 2(L_T + n \times L_{O/L})/(n+1) \quad (3)$$

$$Y_2 = \{(n-1) \times L_T - 2n \times L_{O/L}\}/(n+1) \quad (4)$$

where Y_1 and Y_2 is the demagnified width of transparent and opaque region, respectively. $L_{O/L}$ is the overlap length. In order to avoid the nucleation phenomenon Y_1 is limited below lateral growth length (LGL) at a given laser energy density, and Y_2 is limited above the optical resolution of SLS equipment[8]. Fig. 2(a) shows the evolution of microstructure in the n-shot process and (b) is the diagram for the correlation among targeted grain size, process- and mask design-parameters. For example, if the microstructure requirement for the architecture of an SOG displays is a poly-Si with 9 um grain-size and an overlap length as 2.0 um, n-shot SLS with n≥4 is applicable to obtain the poly-Si grains of 9.0 um. Increasing shot number (n) enlarges the grain size of poly-Si while it decreases throughput. Therefore, n=4 is most desirable for L_T=9 um and $L_{O/L}$=2 um. Based on the derived equations and experimentally measured lateral growth length (LGL) with laser energy density, we can design SLS process and mask for a given targeted grain length. On the consideration of grain size and throughput, 2 shot SLS has been developed for this work.

2.2 SLS uniformity improvement

SLS beam of this work has the dimension of 2 mm x 15 mm compared with the larger area of glass substrate. In addition, there is a laser energy variation in shot-to-shot and the energy profile within each shot is not perfectly flat. Occasionally, one can see shot marks, corresponding to the SLS beam dimension, in the display panel. It is thought that those are related with the difference of poly-Si microstructure originated from the non-uniformity in SLS process, which increases the variation of

pixel TFT characteristics[9]. As an approaching method for the non-uniformity in SLS process, "smearing technique" or "shot mixing method"[10] was proposed. However, that method needs complicated SLS mask design and may decrease throughput. Our approach is to improve SLS laser beam uniformity by strictly optimizing the optics (lens, mirror, etc) of the SLS system. We used a conventional 2 shot SLS mask and thereby there is no decrease in throughput. Additionally, anti-reflective (AR) coating on the SLS mask is also helpful for more uniform energy profile in the SLS beam dimension. The improvement of beam uniformity was confirmed by comparing the Vth variation in whole pixel TFTs along the panel horizontal direction (gate line direction) before and after SLS process tuning.

3. Process and TFT characteristics

Conventional 8 mask CMOS LTPS process was applied to fabricate poly-Si TFT on 370 mm x 470 mm x 0.5 t-size glass substrate. Detailed process was described in elsewhere[11]. In order to enhance the mobility, low sheet resistance (Rs) of doped poly-Si film of S/D region is important as well as high quality poly-Si and gate oxide. As for the dopant activation method, it is well known that laser annealing is more advantageous for lower Rs and thereby higher mobility compared with furnace annealing. In this work, however, we adopted a furnace activation method because we considered that the furnace annealing is more cost-effective and advantageous for the uniformity than laser annealing. By optimizing acceleration energy and minimizing out-gassing issue of photo resist during the doping process, we have obtained Rs of 1~3 kohm/sq after 500 C-activation annealing. For the CMOS circuit operation scheme, symmetric characteristics of N-channel TFT (NTFT) and P-channel TFT (PTFT) are required for proper CMOS circuit operation. In order to adjust Vth for the symmetric characteristics, channel doping was applied with the dose below 5e11 /cm^2.

3.1 Circuit TFT

Id-Vg characteristics of NTFT and PTFT are shown in Fig. 3 and device parameters for both devices are summarized in Table. 1. Channel length (L) and width (W) for circuit TFT were 10 and 4 um. For NTFT, lightly doped drain (LDD) region with 1.5 um-length was adopted. Mobility of NTFT and PTFT were 187 and 59 cm^2/Vs for non-channel doping case, 146 and 38 cm^2/Vs for channel doping case, respectively. Vth of NTFT and PTFT without

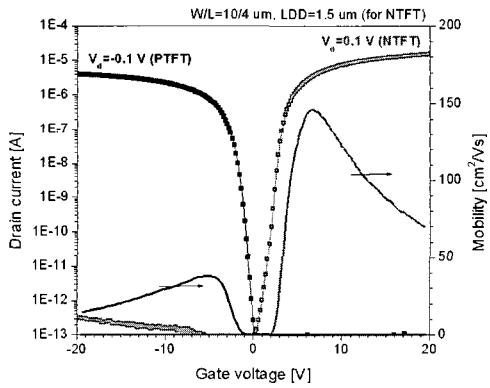


Fig. 3. Id-Vg characteristics of NTFT and PTFT. W/L=10/4 um and LDD length is 1.5 um for NTFT.

Table 1. Device parameters of NTFT and PTFT in Fig.3.

	w/o channel doping		w/ channel doping	
	NTFT	PTFT	NTFT	PTFT
Vth [V]	0.49	-4.17	3.86	-2.79
Mobility [cm2/Vs]	187	59	146	38
Slope [V/dec]	0.35	0.42	0.36	0.40

channel doping were 0.49 and -4.17 V and adjusted to 3.86 and -2.79 V by channel doping, respectively.

3.2 Pixel TFT

Pixel TFT has a dual gate NTFT structure with W/L/LDD=4/(4+4)/1.5 um. Fig. 4(a) and (c) shows Id-Vg characteristics and their Vth measured for 370 pixel TFTs in a 2.2-inch QVGA panel along a gate line. Average value and 3sigma of Vth are 3.81 V and 1.89 V, respectively. Wide range of Vth like this increases the variation of feed through voltage (ΔVp) among pixel TFTs and cause the non-uniformity in display image. The non-uniformity emerged as the SLS shot marks, which are perceived especially in gray-scale display images.

As we previously commented in section 2.2, the non-uniformity is related with SLS process. Thus, we have improved the SLS beam uniformity by strictly optimizing the optics of SLS system. Fig. 4(b) and (d) are I-V characteristics and their Vth variation for whole 720 pixel (240xRGB) TFTs along a gate line measured in a 2.2-inch QVGA panel

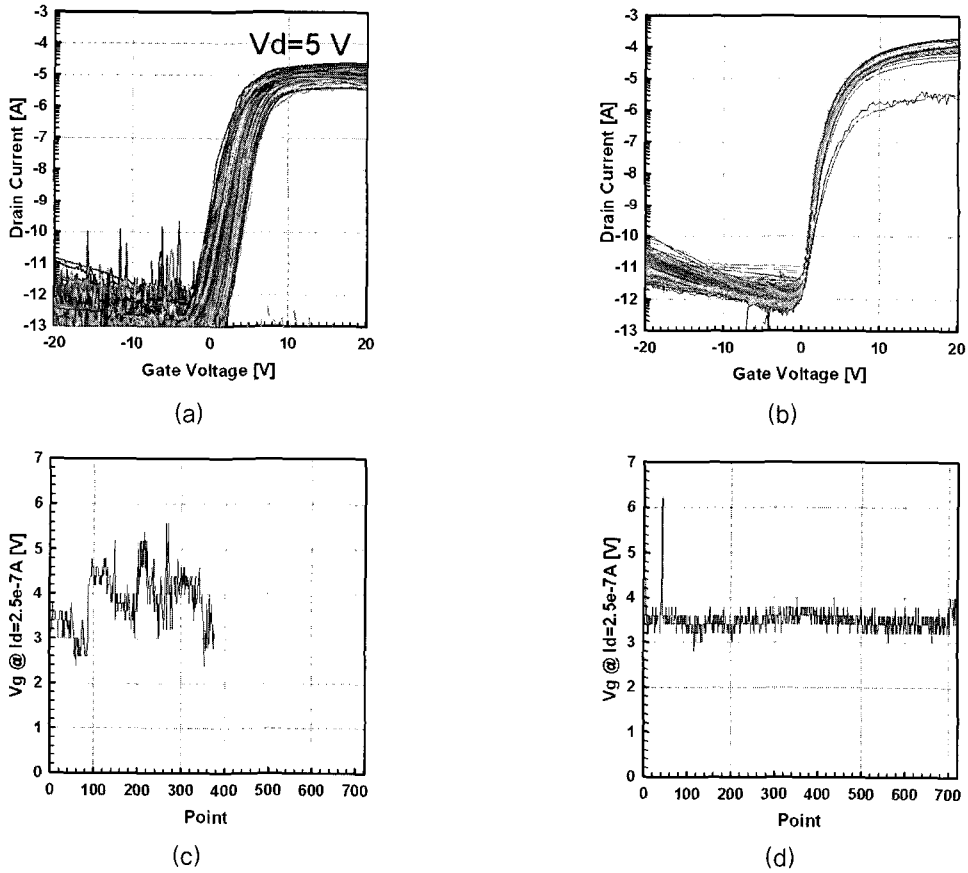


Fig. 4. Id-Vg characteristics and Vth [defined as Vg for Id=2.5x e^{-7} A] of pixel TFTs. (a) and (c) for 370 pixel TFTs fabricated by SLS process before improved. (b) and (d) for 720 pixel TFTs fabricated by improved SLS process.

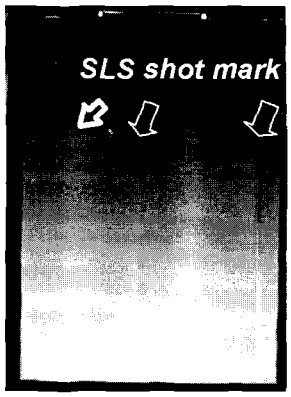
fabricated by an improved SLS process. Average value and 3sigma of Vth for this case are 3.48 V and 0.56 V, respectively. Consequently, the uniformity of pixel TFT characteristics was remarkably improved.

4. Panel

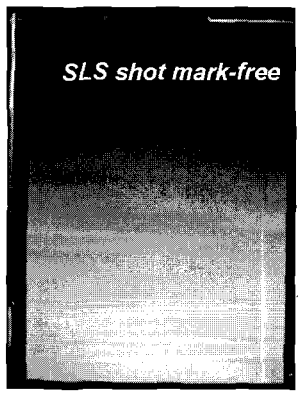
Fig. 5(a) is a gray scale images of a panel fabricated by a conventional 2 shot SLS. Sharp boundaries and white columns are observed. Particularly, the distance between these boundaries and columns is 15 mm, exactly fitted to the SLS beam dimension. According to our simulation, a wide variation of Vth in pixel TFTs causes the variation of feed through voltage (Δ Vp) of pixel TFTs and finally emerges as the non-uniformity of transmittance in the display. Therefore, these results indicate that the features in Fig. 5(a) should be originated from the non-uniformity of pixel TFT characteristics, which is closely related with the SLS process and called as "SLS shot mark". After SLS optics tuning, we have improved the uniformity of SLS process and successfully fabricated the SLS shot mark-free panel as shown in Fig. 5(b). A color display image and panel specification of 2.2-inch QVGA LTPS panel with integrated gate driver and 3:1 DeMUX switching circuits are shown in Fig. 5(c) and Table.2, respectively.

5. SOG unit circuits

The gate driver circuits are composed of D-latches (delay- latches), NAND gates, level shifters, and output buffers. The D-latch circuit might malfunction because of non-uniform characteristics of TFTs or the clock overlapping due to the rather long clock delay times. Therefore, the non-



(a)



(b)

(c)

Fig. 5. Photograph of 2.2-inch QVGA display image.

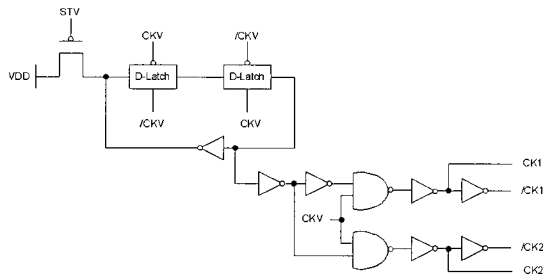
Table 2. Panel specification.

Parameter	Specifications
Glass	0.5t glass
Display size	2.2 inch (TN)
Resolution	qVGA (180 ppi)
Pixel number	240 x RGB x 320
Pixel pitch	46.5 ㎛ x 139.5 ㎛
Brightness [cd/m2]	250 (typ.)
Contrast ratio	300:1
Viewing angle (R/L/U/D)	45/45/15/30
Gray scale	64 gray (262k colors)
Color gamut	45 %
Driving voltage	(10 V / -5 V) / 4 V / 4 V (Vgate)/Vdata/Vcom
Driving method	Line inversion
Integrated circuit	Gate driver Source 3:1 DeMUX

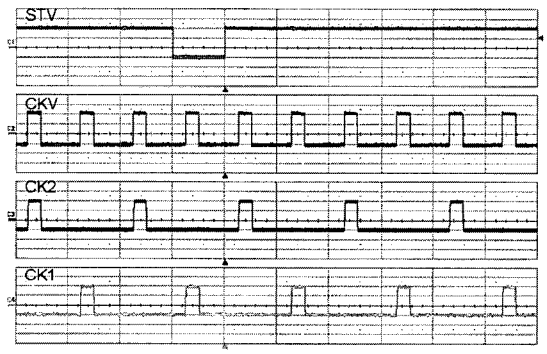
overlapped 2-phase clock system is employed in our shift register circuits [12]. Fig. 6 (a) and (b) show the schematic diagram of the circuit which generates the non-overlapped clocks and the measured output waveforms, respectively.

In order to implement the SOG, it is essential to integrate an efficient DC-DC converter circuit for generating the power supplies of the gate driver circuits. Well-known switched-capacitor circuit is employed[13] and the measured output voltages as a function of load currents are shown in Fig. 7. Although the output voltages drop slightly as the load currents increase, the voltage drop can be made negligible by optimizing TFT sizes and capacitors.

It is well known that the implementation of an area-efficient digital-to-analog converter (DAC) is an obstacle to source driver integration. Figure 8 shows the measured output voltage of a 6-bit cyclic DAC[14] and a source follower unit circuit. Additional 2 bits were used in order to correct gamma curves. The simple cyclic DAC scheme might be a candidate for area-efficient DACs even though the switching accuracy of it and the accuracy of the source follower should be improved.



(a)



(b)

Fig. 6. (a) The schematic diagram of the circuit which generates the non-overlapped clocks, and (b) the measured output waveforms.

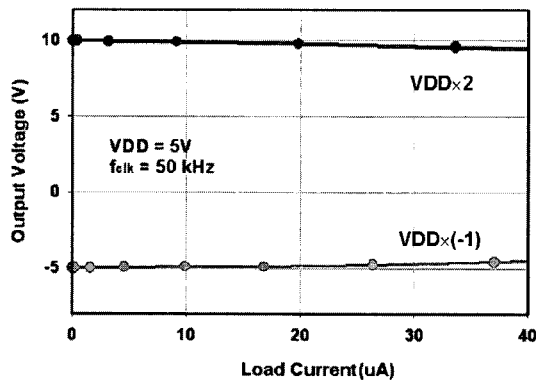


Fig. 7. The measured output voltages of the DC-DC converter as a function of load currents.

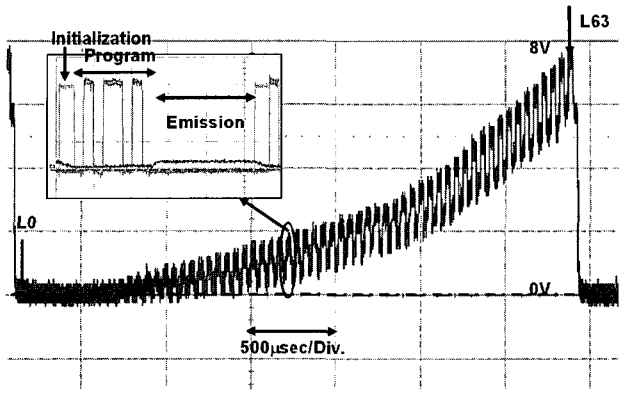


Fig. 8. The measured output voltage of a 6-bit cyclic DAC and a source follower unit circuit.

6. Conclusion

We have developed SLS technology for high performance and uniform display. For CMOS circuit TFT, Vth was adjusted by channel doping and mobility was enhanced by decreasing sheet resistance of doped poly-Si film. By strictly optimizing the conventional 2 shot SLS process, remarkably improved uniformity in display area was achieved, which was confirmed by comparing the Vth variation of pixel TFTs in 2.2-inch QVGA panel before and after SLS process tuning. Unit circuits for SOG were also fabricated and evaluated.

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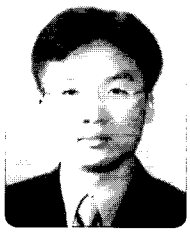

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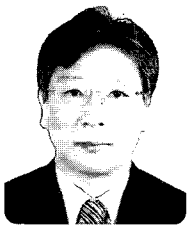

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